Microelectronics & VLSI at IIT Bombay

Department of Electrical Engineering
Indian Institute of Technology, Bombay
2003

IIT Bombay

- IIT Bombay is one of 7 IITs in India, and the oldest but one
- Located on a 250 hectare campus on the shores of Powai lake
- About 400 faculty and 5000 students
- More than half of the students are post-graduate students
- 26 major Departments, Schools and Centres, plus 6 inter-disciplinary programmes

Department of Electrical Engineering

- The largest Department at IIT Bombay
- About 40 faculty and 600 students
- Major research and teaching areas
  - Communications & Signal Processing
  - Power Electronics & Power Systems
  - Electronic Systems
  - Control & Computing
  - Microelectronics & VLSI

Microelectronics & VLSI

- Microelectronics & VLSI is the largest group in EE Department at IIT Bombay
- Started in 1984; Group activity emphasized
- Main thrust in silicon CMOS devices, technology and design
- Group consists of 12 core faculty and 110 post-graduate students

Faculty

- P. R. Apte
- A. N. Chandorkar
- M. P. Desai
- S. Duttagupta
- B. Gadepally*
- R. Lal
- S. Mahapatra
- H. Narayanan
- R. Parekhji*
- M. B. Patil
- R. Pinto
- V. Ramgopal Rao
- D. K. Sharma
- S. D. Sherlekar*
- J. Vasi

*Adjunct

Associated Faculty From EE Department

• A. Karandikar	Communications
• D. Manjunath	Communications
• V. Gadre	Communications
• Girish Kumar	Communications
• Girish Saraph	Communications
• R.K. Shevgaonkar	Communications
• P.C. Pandey	Electronic Systems

Associated Faculty From Other Departments

• S. S. S. P. Rao	Comp. Sci. & Engg.
• S. Chakrabarty	Comp. Sci. & Engg.
• M. Sohoni	Comp. Sci. & Engg.
• S. Patkar	Maths
• R. O. Dusane	Met. Eng. & Mat. Sci.
• R. Srinivasa	Met. Eng. & Mat. Sci.
• A. Contractor	Chemistry
• M. Ravikanth	Chemistry
• S. Mukherji	Bio-medical

Teaching Programs

- Ph.D. (graduating ~ 3 - 5 / year)
- M.Tech. with specialization in Microelectronics (~ 35 / year)
- Dual Degree (B.Tech. + M.Tech.) with specialization in Microelectronics (~ 20 / year)
- B.Tech. (~ 50 / year, ~ 15 / year with projects in Micro-electronics)

Areas of R & D

- Silicon CMOS physics and technology
- MEMS, BioMEMS
- New materials
- Device modeling and simulation
- VLSI design (digital, analog, mixed-mode, RF)
- VLSI CAD tool development
- Interaction between VLSI technology and design

Facilities

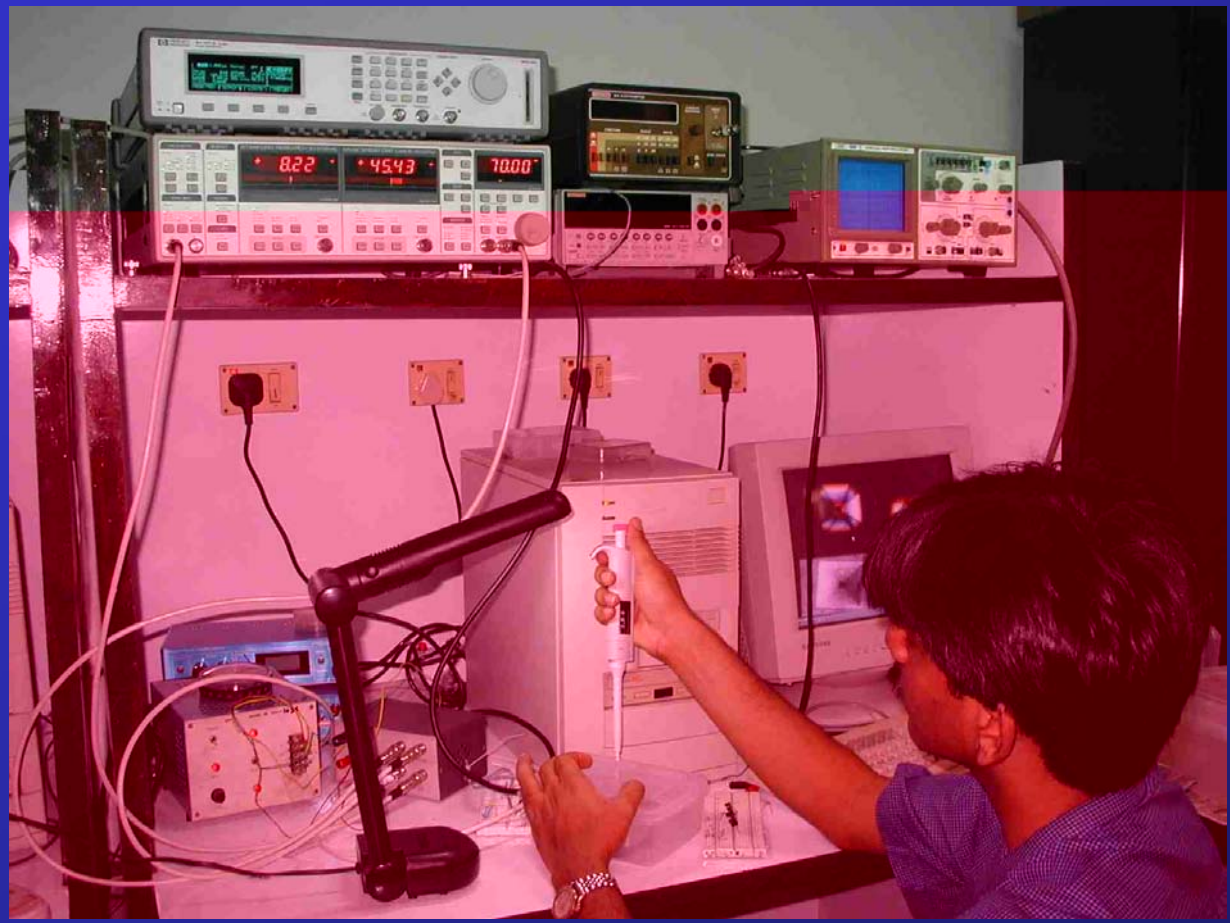
- Class 1000 Clean Room (class 100 work areas) with facilities for complete IC manufacturing (optical & EB lithography, RIE, Deposition, Sputter, RTP, Furnace facilities)
- MEMS fabrication
- Excellent characterization facility
- SEM; photoluminescence
- VLSI design workstations
- VLSI design tools
  - Cadence, Mentor, Synopsys, Tanner, Xilinx, plus many public domain tools
- Simulation workstations
- Simulation software
  - Medici, TSuprem, ISE-TCAD, SMC (Monte Carlo)
- Gaitonde Integrated Systems Laboratory
- Intel Microelectronics Lab
- TCS VLSI Design Lab

Facilities: Clean Room

Facilities: Photolithography

Facilities: SEM

Facilities: Characterization



Facilities: Intel Lab

Facilities: TCS Lab

Facilities: TCS Lab

Sponsored Projects

- Over 60 projects since 1985 totaling US$ 8 Million
- Projects cover all areas of Microelectronics & VLSI
- Projects from major government agencies, and leading Indian & international companies

Some Recent & Ongoing Projects:
Physics & Technology

- Silicon sensors for electroporation (Praman Technology)
- BioMEMS sensors for cardiac applications (ADA)
- Silicon Locket (TCS)
- Channel engineering for 100 nm CMOS devices (DST)
- Characterization of vertical MOS transistors (Siemens)
- Design and characterization of Flash memories (Hitachi)

Some Ongoing Projects:
Modeling & Simulation

- Development of a hot-carrier simulator (Motorola)
- Look-up table modeling for circuit simulation (DST)
- Modeling of power semiconductor devices (GE)
- Macromodels for circuit simulation (National)
- RF MOSFET models (IME, Singapore)
- Oxide scaling effects on design issues (Intel)
- CMOS device design and optimization for mixed-signal applications (Intel)

Some Ongoing Projects:
VLSI CAD Tools

- Interconnect capacitance extraction by Monte Carlo (Intel)
- Eigenvalues for large scale systems (NRB)
- Math programming & electrical networks (DST)
- General purpose systems partitioners (NRB)
- Design issues with high-k dielectrics (Intel)

Some Ongoing Projects:
VLSI Design

- Analog PHY interface chip (ControlNet)
- Data Conversion & RF Circuits (Texas Instruments India)
- High-speed comparator design (TII)
- Communication VLSI Design (SASKEN)
- Packet classifier (Switch-on Networks)
- FSM-based packet router (DST)
- On-chip coupling capacitance measurement (MHRD)
- VLSI Design training (MIT, TCS)

Recent Work in RF Design

- Design of RF Tuner for Cable Modem Applications: V.Babu, S. Seth and A.N. Chandorkar – won the best paper award at VLSI-2004
- A new Approach to Model Nonquasi-static (NQS) Effects For MOSFETS – A.S. Roy, J.M. Vasi and M.B. Patil, IEEE transactions on Electron Devices, ED-50, 2401 (2003)
- Dual Channel RF receiver design – A Krishnakanth, D. K. Sharma – 6th International Symposium on Wireless Multimedia communications WPMC '03, Yokosuka, Kanagawa, Japan, Dec 2003
- Linearization of RF Power Amplifiers – A. Kotwal, A.N. Chandorkar (M.Tech. Project)
- Power optimal RF data transfer for mobile heart monitoring – N. Nagaraju, S. Gupta, R. Lal, D.K. Sharma (3 M.Tech. Projects in progress)

Some Recent and Ongoing Ph. D. Theses

- S. Vaidya: Neutron radiation effects in MOS systems
- J. Meckie: Asynchronous design issues
- G. Trivedi: Parallel algorithms for VLSI optimization
- N. Mahapatra: High-k dielectrics for 100 nm CMOS
- A. Shastry: Microcapillary electrophoresis on silicon
- C.A. Betty: Capacitive immunosensor on porous Si
- B. Anand: Digital design with dynamic threshold CMOS
- D. Nair: Flash memory design and reliability
- D.V.Kumar: Look-up table approach for CMOS circuits
- K. Narasimhulu: CMOS devices for mixed-signal design

Industry Collaborations

- Sponsored, Consultancy & Collaborative Projects
  - Indian industry: SCL, BEL, ITI, TCS, Sasken, TII, Cypress, ControlNet, National, etc
  - International industry: Intel, Motorola, GE, Siemens, Hitachi, National, IME, Agere
- Industry sponsorship of students
  - M.Tech. & Dual Degree students
  - Ph.D. students
- Endowed Laboratories
  - Gaitonde Integrated Systems Laboratory
  - Intel Microelectronics Laboratory
  - TCS VLSI Design & Characterization Laboratory
- Continuing Education Programs for industry

University Collaborations

- Research Collaborations
  - Other IITs, IISc, Universities of Bombay, Pune
  - International universities like
    - UCLA, UCSB, Yale University (USA)
    - Hong Kong University of Science & Tech. (HK)
    - Delft University (The Netherlands)
    - University of Bundeswehr (Germany)
    - Griffith University (Australia)
    - NUS, NTU (Singapore)
- Student Exchanges

Mode of Interaction with Intel

- Intel Laboratory
- Intel Sponsored Research
- Intel Sponsorship for Students

Intel Sponsored Ph.D. Students

- Nihar Mohapatra: "Device and Circuit Performance Trade-offs with the Use of High-K Dielectrics in Sub-100 nm CMOS Technologies" (Graduated in Jan 2004)
- D. Vinay Kumar: "Gate Oxide thickness Scaling in Sub-100 nm MOSFETS and its Effect on Circuit Performance"
- K. Narasimhulu + 1 student: "Impact of Device Scaling on Mixed-Signal CMOS Circuits"

Publications by Intel Sponsored Ph.D. Students

International Journals:

- Nihar.R.Mohapatra, A.Dutta, G.Sridhar, M.P.Desai and V.Ramgopal Rao “Sub 100 nm CMOS Circuit Performance with High-K Gate Dielectrics” Microelectronics Reliability, Vol. 41, p.1045-1048, 2001
- Nihar R. Mohapatra, Madhav P. Desai, Siva G. Narendra, V. Ramgopal Rao, "The Effect of High-K Gate Dielectrics on Deep Sub-micrometer CMOS Device and Circuit Performance", IEEE Transactions on Electron Devices, p. 826-831, Vol. 5, 2002.
- Nihar R. Mohapatra, Madhav P. Desai, Siva.G.Narendra, V. Ramgopal Rao, “Modeling of Parasitic Capacitances in Deep Sub-micrometer Conventional and High-K dielectric MOS Transistors” IEEE Transactions on Electron Devices, vol. 50, No.4, pp. 959-966, 2003
- Nihar .R.Mohapatra, D.R.Nair, S.Mahapatra, V.Ramgopal Rao, S.Shukuri, J.D.Bude, "CHISEL programming Operation of Scaled NOR Flash EEPROMs-Effect of Voltage Scaling, Device Scaling, and Technological Parameters", IEEE Transactions on Electron Devices, vol. 50, pp.2104-2111, October 2003
- K.Narasimhulu, D.K.Sharma and V.Ramgopal Rao, "Impact of Lateral Asymmetric Channel Doping on Deep Sub-Micrometer Mixed-Signal Device and Circuit Performance", IEEE Transactions on Electron Devices vol. 50, pp.2481-2489, December 2003
- V.Ramgopal Rao, Nihar R. Mohapatra, "Device and Circuit Performance issues with Deeply Scaled High-K MOS Transistors", Journal of Semiconductor Technology and Science (JSTS), Korea, Special issue on Device Reliability, September 2003. (Invited)
- K. Narasimhulu, Madhav P. Desai, Siva G. Narendra and V. Ramgopal Rao, "The Effect of Lateral Asymmetric Channel (LAC) Doping on Deep Sub-micron Transistor Capacitances and its Influence on Device RF Performance", Accepted, IEEE Transactions on Electron Devices, 2004

International Conferences:

1. Nihar.R.Mohapatra, A.Dutta, M.P.Desai and V. Ramgopal Rao, “Effect of Fringing Capacitances in Sub 100 nm MOSFET's with High-K Gate Dielectrics” Proceedings of the 14th International Conference on VLSI Design, January 2001, Bangalore, INDIA
2. Nihar.R.Mohapatra, A.Dutta, G.Sridhar, M.P.Desai and V.Ramgopal Rao “Sub 100 nm CMOS Circuit Performance with High-K Gate Dielectrics” Proceedings of the 11th Workshop on Dielectrics in Microelectronics (WoDiM), November 13-15, 2000, Munich, Germany
3. Nihar. R. Mohapatra, M. P. Desai, Narendra Siva, V. Ramgopal Rao, “The Impact of High-K Gate Dielectrics on Sub 100nm CMOS Circuit Performance”, Proceedings of the 31 st European Solid-State Device Research Conference (ESSDERC), 11 - 13 September 2001, Nuremberg, Germany, September, 2001
4. Nihar Mohapatra, Souvik Mahapatra, V.Ramgopal Rao, “"Study of Degradation in Channel Initiated Secondary Electron Injection Regime", Proceedings of the 31 st European Solid-State Device Research Conference (ESSDERC), 11 - 13 September 2001, Nuremberg, Germany, September, 2001.
5. Nihar. R. Mohapatra, Souvik Mahapatra and V. Ramgopal Rao, “A Comparative Study of Degradation for NMOSFET's in CHE and CHISEL Injection Regime”, Proceedings of the 11 th International Workshop on The Physics of Semiconductor Devices, December 11-15, 2001, Delhi, India
6. Nihar. R. Mohapatra, M. P. Desai, V. Ramgopal Rao, “Effect of Technology Scaling on MOS Transistors with High-K Gate Dielectrics”, Proceedings of the 2002 MRS Spring Meeting, San Francisco, California (April 1-5, 2002)
7. Krishna K. Bhuwalka, Nihar. R. Mohapatra, Siva G.Narendra, V. Ramgopal Rao, “Effective dielectric thickness Scaling for High-K Gate Dielectric MOSFETs”, Proceedings of the 2002 MRS Spring Meeting, San Francisco, California (April 1-5, 2002)
8. Nihar. R. Mohapatra, Souvik Mahapatra and V. Ramgopal Rao, “Device Scaling Effects on Substrate Enhanced Degradation in MOS Transistors”, Proceedings of the 2002 MRS Spring Meeting, San Francisco, California (April 1-5, 2002)

9. N.R Mohapatra, S. Mahapatra and V. Ramgopal Rao, “Bias and Time Dependene of Damage Generation in n-Channel MOS Transistors Operating in the Substrate Enhanced Gate Current Regime” Proceedings of the 9 th IEEE International Symposium on Physical and Failure Analysis of Integrated Circuits, 8-12 July 2002, Singapore
10. Nihar. R. Mohapatra, S. Mahapatra, V. Ramgopal Rao, S. Shukuri and J. Bude, “Effect of Programming Biases on the Reliability of CHE and CHISEL Flash EEPROMs”, Proceedings of the International Reliability Physics Symposium (IRPS) 2003, March 30 - April 3, 2003, Dallas, Texas, USA
11. Nihar Mohapatra, Deleep Nair, Souvik Mahapatra, V. Ramgopal Rao, Shoji Shukuri, "The Impact of Channel Engineering on the Performance Reliability and Scaling of CHISEL NOR Flash EEPROMs", 33rd European Solid-State Device Research Conference (ESSDERC) 2003: 16 - 18 September 2003, pp. 541-544, Lisbon, Portugal
12. D. Vinay Kumar, N. R.Mohapatra, V. Ramgopal Rao, and M. B. Patil, "Application of the look-up table approach to high-K dielectric MOS transistor circuits," Proceedings of the 16th IEEE International Conference on VLSI Design, January 4-8, 2003, New Delhi, India
13. N.R Mohapatra, M.P.Desai, and V. Ramgopal Rao “Detailed Analysis of FIBL in MOS Transistors with High-K Gate Dielectrics”, Proceedings of the 16th IEEE International Conference on VLSI Design, January 4-8, 2003, New Delhi, India
14. D. Vinay Kumar, R. A. Thakker, M. B. Patil, and V. Ramgopal Rao, "Simulation study of non quasi static behaviour of MOS transistors," Proc. 5th International Conference on Modeling and Simulation of Microsystems, San Juan, Puerto Rico, April 22, 2002.
15. Nihar. R. Mohapatra, S. Mahapatra, V. Ramgopal Rao, S. Shukuri and J. Bude, “Effect of Programming Biases on the Reliability of CHE and CHISEL Flash EEPROMs”, Proceedings of the International Reliability Physics Symposium (IRPS) 2003, March 30 - April 3, 2003, Dallas, Texas, USA
16. K. Narasimhulu, ,Siva G.Narendra, and V. Ramgopal Rao, “Effect of Process Variations on Device and Circuit Parameters with LAC/DH MOSFETs”, proceedings of the 17 th IEEE International Conference on VLSI Design, January 7-9, 2004, Mumbai, India

Achievements

- Undertaken projects of national importance (over US $8 Million in the last 15 years) and successfully transferred technologies to industries
- Close industry interaction
- Publish over 30 research papers every year in reputed international journals and conferences

Group's publications in the area of Electron Devices in the last few months in IEEE Trans. On Electron Devices/IEEE Electron Device Letters

1. Najeeb-ud-din, et.al., "Analysis of Floating Body Effects in Thin Film Conventional and Single Pocket SOI MOSFETs using the GIDL Current Technique", *IEEE Electron Device Letters*, vol. 23, p. 209-211, April 2002
2. B. J. Daniel, et al., "Modeling of the CoolMOS transistor Part I: Device physics," IEEE Trans. Electron Devices, pp. 916-922, May 2002.
3. B. J. Daniel, et al., "Modeling of the CoolMOS transistor Part II: DC model and parameter extraction," IEEE Trans. Electron Devices, pp. 922-929, May 2002.
4. Nihar R. Mohapatra et.al., "The Effect of High-K Gate Dielectrics on Deep Sub-micrometer CMOS Device and Circuit Performance" *IEEE Transactions on Electron Devices*, vol.49, (no.5), May 2002, p.826-831
5. P.Sivaram et.al., "Silicon film thickness considerations in SOI-DTMOS", *IEEE Electron Device Letters*, vol. 23, p. 276 –278, May 2002
6. D.G.Borse, et.al., , "Optimization and Realization of Sub 100nm Channel Length Single Halo p-MOSFETs" *IEEE Transactions on Electron Devices*, vol.49, (no.6), June 2002.
7. S. Mahapatra, et.al., "CHISEL Flash EEPROM. I. Performance and scaling" *IEEE Transactions on Electron Devices*, vol.49 p.1296 –1301, July 2002
8. S. Mahapatra, et.al., "CHISEL flash EEPROM. II. Reliability", *IEEE Transactions on Electron Devices*, vol.49 p. 1302 -1307, July 2002
9. K.N.Manjularani, et al, "A New Method to Characterize Border Traps in Sub-Micron Transistors using Hysteresis in the Drain Current", IEEE Transactions on Electron Devices, vol. 50, No.4, pp. 973-979, 2003
10. Sahoo, D.K et al., "High-field effects in silicon nitride passivated GaN MODFETs "IEEE Transactions on Electron Devices, Volume: 50 Issue: 5 , May 2003, pp.1163 -1170
11. N.R.Mohapatra, et. al., "CHISEL programming Operation of Scaled NOR Flash EEPROMs-Effect of Voltage Scaling, Device Scaling, and Technological Parameters", IEEE Transactions on Electron Devices, vol. 50, No.2104-2111, October 2003
12. K.Narasimhulu et.al., "Impact of Lateral Asymmetric Channel Doping on Deep Sub-Micrometer Mixed-Signal Device and Circuit Performance", IEEE Transactions on Electron Devices vol. 50, pp.2481-2489, December 2003
13. Ananda Sankar Roy et al., "A New Approach to model non-quasi-static (NQS) effects for MOSFETs: Part I: Large Signal Analysis, *IEEE Trans. Electron Devices*, **51**, **(**2004).
14. Ananda Sankar Roy et al., "A New Approach to model non-quasi-static (NQS) effects for MOSFETs: Part II:Small Signal Analysis, *IEEE Trans. Electron Devices* **51**, (2004).
15. B.Anand, M.P.Desai, and V.Ramgopal Rao, "Silicon Film Thickness Optimization for SOI-DTMOS from Circuit Performance considerations", Accepted for publication, IEEE Electron Device Letters, June, 2004
16. K. Narasimhulu, Madhav P. Desai, Siva G. Narendra and V. Ramgopal Rao, "The Effect of Lateral Asymmetric Channel (LAC) Doping on Deep Sub-micron Transistor Capacitances and its Influence on Device RF Performance", Accepted, IEEE Transactions on Electron Devices, 2004

The group had papers at IEDM 2002, IEDM 2003, IRPS 2003, IRPS 2004 and has had two papers on an average at ESSDERC since 1997

Publications

- Over 200 publications in the last 5 years in major journals and conferences
- Cover all areas of interest
- Details at www.ee.iitb.ac.in/ ~microel/

Conclusions

- Most active Microelectronics & VLSI group in India (publications, sponsored projects, students, facilities)
- Excellent research facilities
- Projects of national importance
- Projects from Indian & international industry
- Major teaching programs at all levels
- High international visibility (Editorial boards, IEEE AdCom, reviews, conference committees. etc.)

Contacts

- Microelectronics Group
  Department of Electrical Engineering
  Indian Institute of Technology, Bombay
  Powai
  Mumbai 400076 India

- Phone: +91-22-2572-3655
- Fax: +91-22-2572-3480
- email: me@ee.iitb.ac.in
- website: www.iitb.ac.in/~microel/