SMDP Workshop on Mixed-Signal VLSI Design, GEC, Goa

Comparators, Gm-C Filters, SC Filters in CMOS Technology

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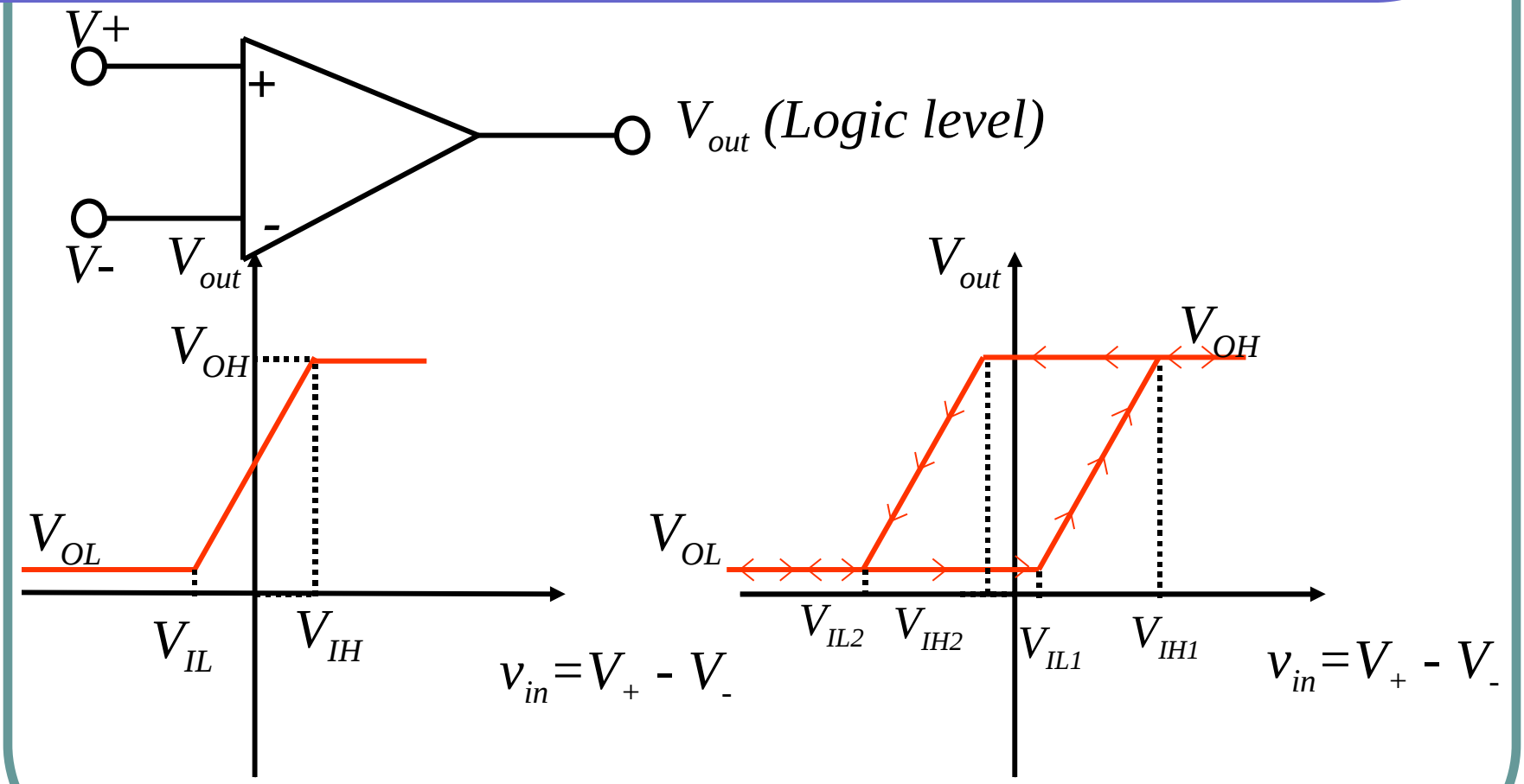
Materials presented in this workshop are partly from the following references.

- CMOS Analog Circuit Design by P. E. Allen et al. , Oxford University Press, 2002.
- CMOS Circuit Design, Layout, and Simulation by R. J. Baker et al, IEEE press, reprint 2002, edition 1998.
- CMOS Mixed-Signal Circuit Design by R. J. Baker, reprint 2008, edition 2002, Wiley.
- Analog Integrated Circuit Design by D. Johns et al. Wiley, edition 2005.

Teaching Methodology

The presented lecture is based on a combination of slide presentation, class notes and lab experiments.

Comparator – Basic Concept



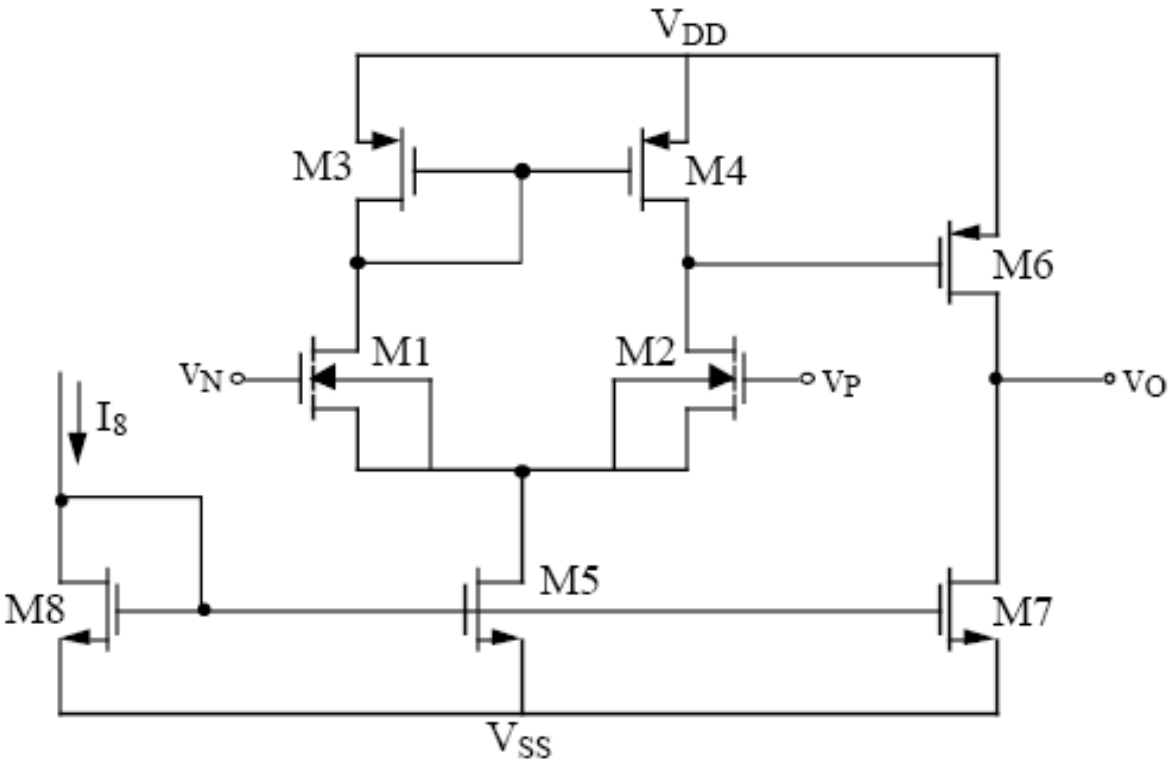
Without hysteresis

With hysteresis

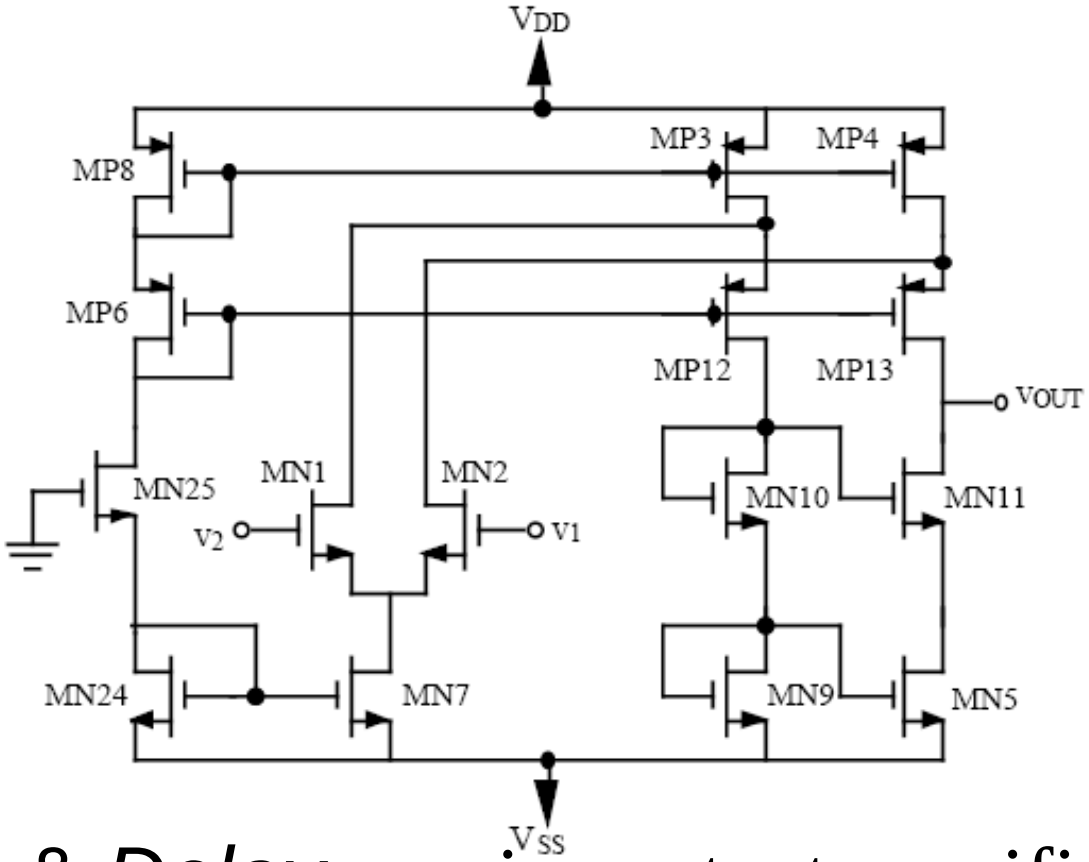
Comparator – Important specifications

- *Gain* ⟷ *Resolution*
- *Delay* ⟷ *Switching speed*
- *Power dissipation*
- *Input common-mode range*
- *Offset voltage*
- *Input noise voltage*

Two-stage op-amp as a comparator?

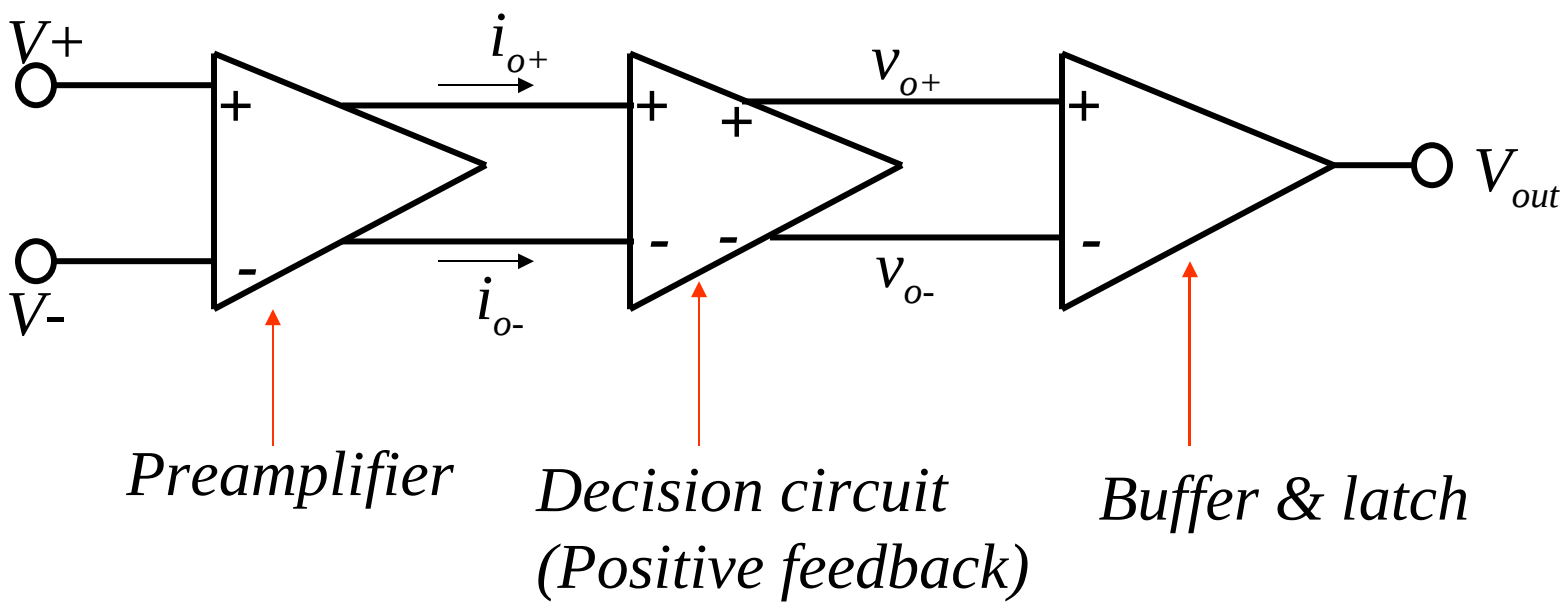


Folded cascode op-amp as a Comparator?

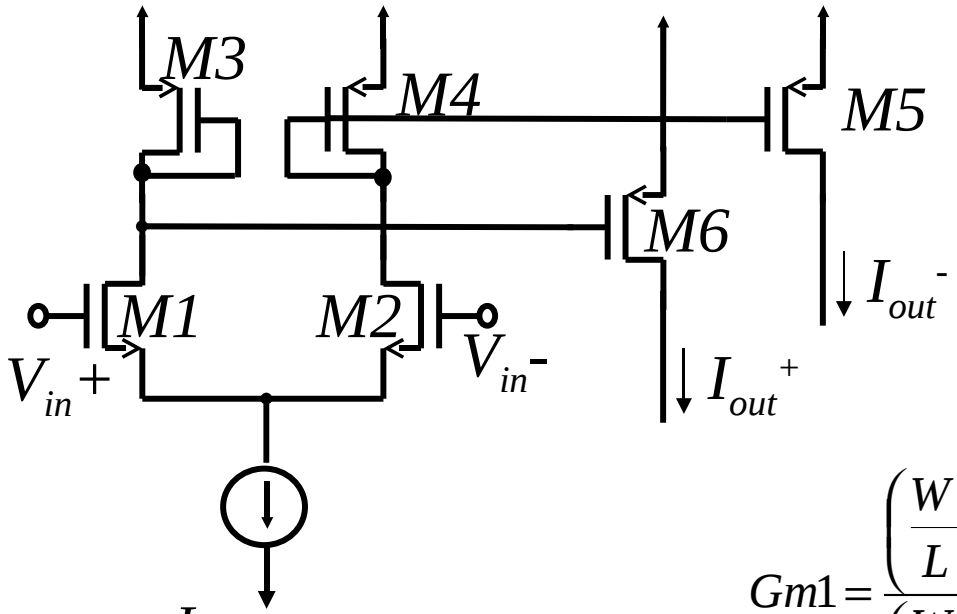


Gain & Delay are important specifications of a comparator.

Comparator - Block Diagram



Comparator – Preamplifier example



All nodes except output Node are low-impedance.

$$I_{out_+} = \frac{I_{ss}}{2} + Gm1 \cdot \left(V_{in_+} - V_{in\_}\right)$$

$$I_{out\_} = \frac{I_{ss}}{2} - Gm1 \cdot \left(V_{in_+} - V_{in\_}\right)$$

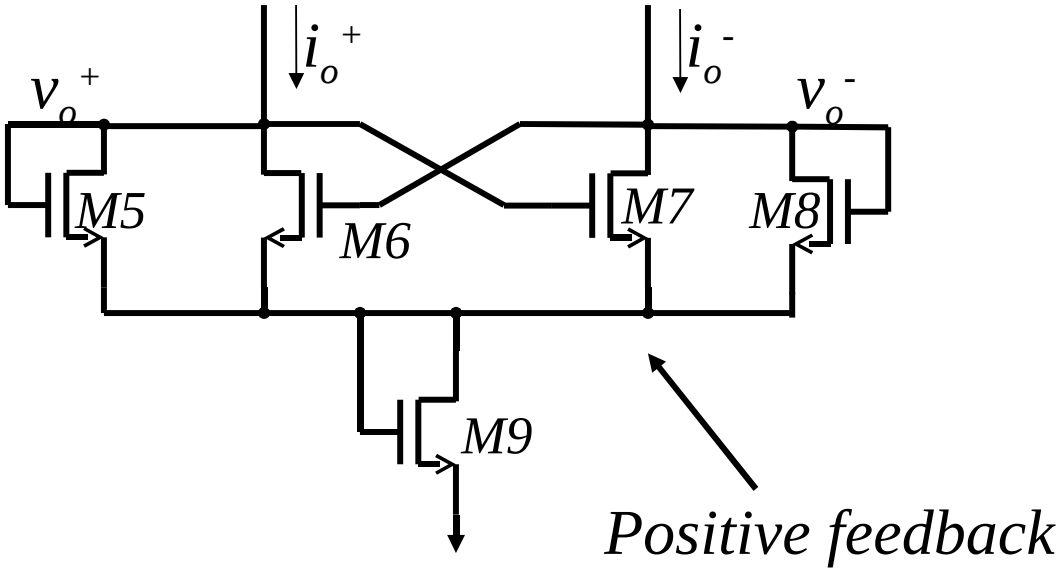
$$Gm1 = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_3} \cdot \frac{gm1}{2}$$

$$\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_5$$

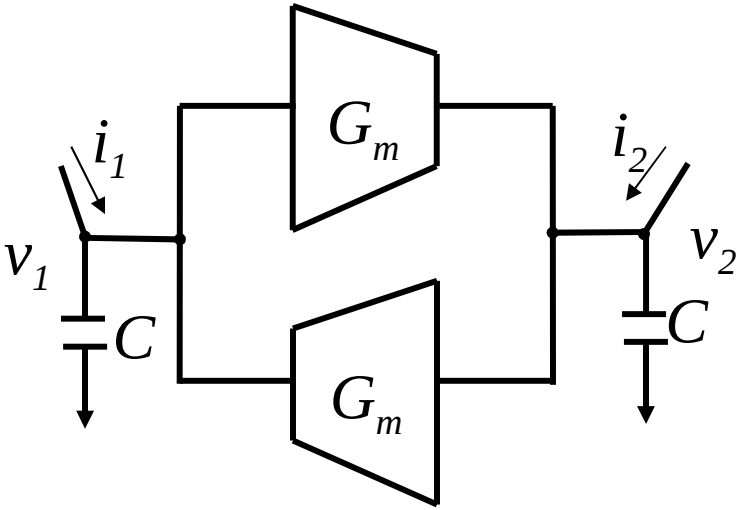
$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$$

Comparator – Decision circuit Example



Positive Feedback Concept

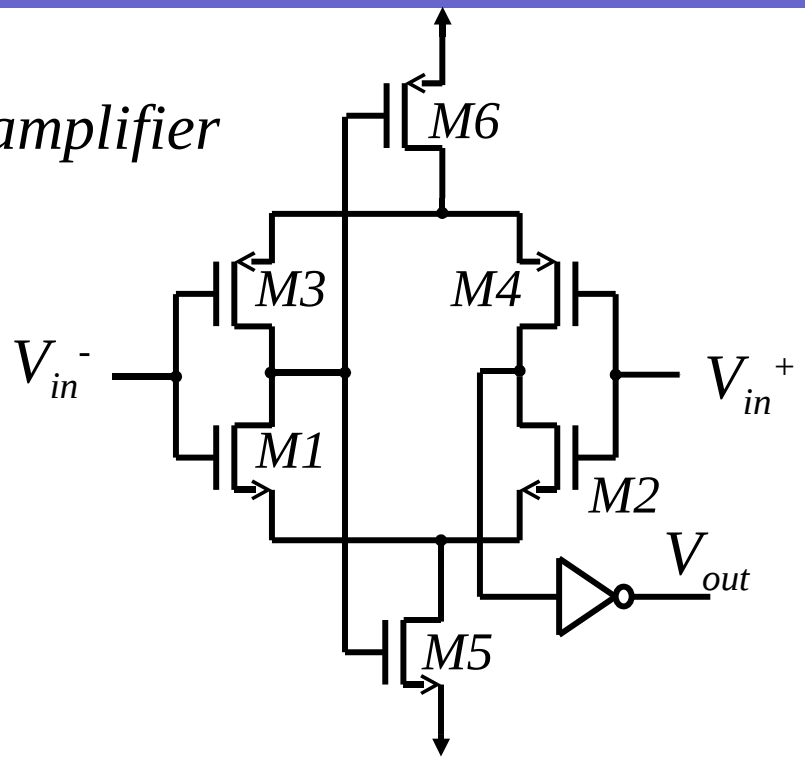


$$If\ i_1 = -i_2 \Rightarrow v_1(s) = \frac{1}{Gm} \cdot \frac{i_1(s)}{\frac{sC}{Gm} - 1}$$

RHP pole

Comparator – An example output buffer

Self-biased differential amplifier



High-speed comparators typically use track-and-latch mechanism for the stage after preamplifier.

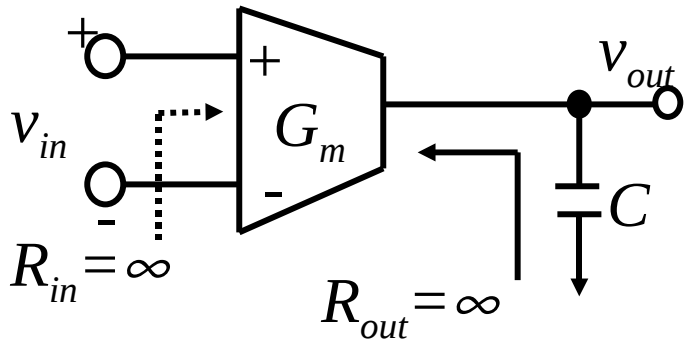
More details will be given in the lecture.

Gm-C Filters

- Application in continuous time filters (DSL/ADSL, Video applications, very low-frequency applications…)
- Need for some sort of tuning circuitry
- Linearity requirements
- Noise performance

Basic building block of Gm-C filters

Integrator is the main building block of continuous time filters.

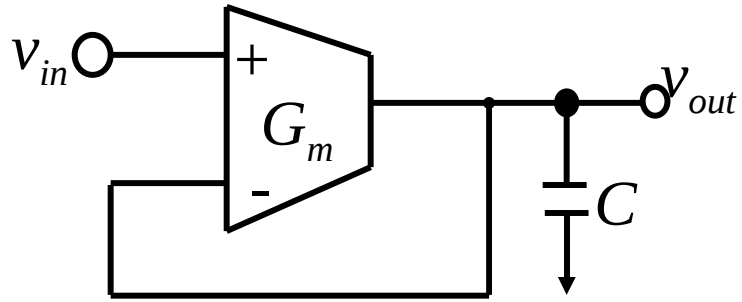


$$v_{out} = \frac{v_{in}}{s \cdot \left(C / G_m \right)}$$

G_m/C: Unity gain frequency of the integrator

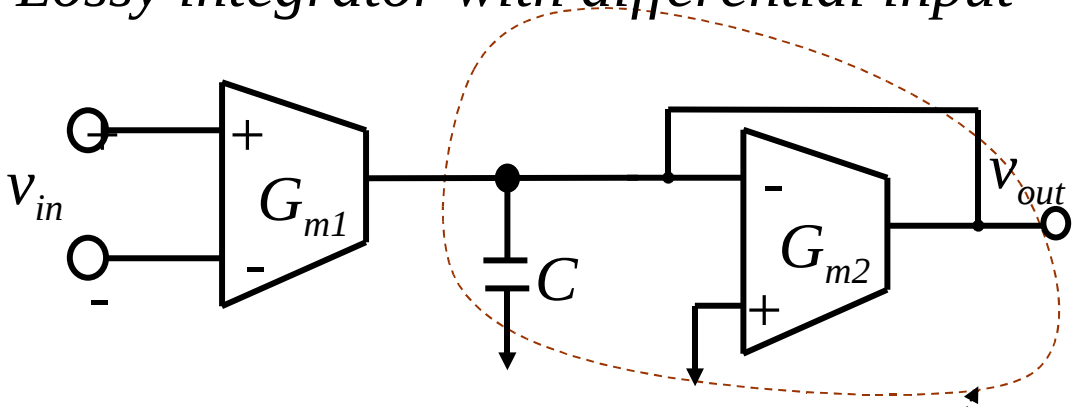
Basic building block of Gm-C filters (cont'd)

Lossy integrator with single-ended input



$$v_{out} = \frac{v_{in}}{1 + s \cdot \left(C / G_m \right)}$$

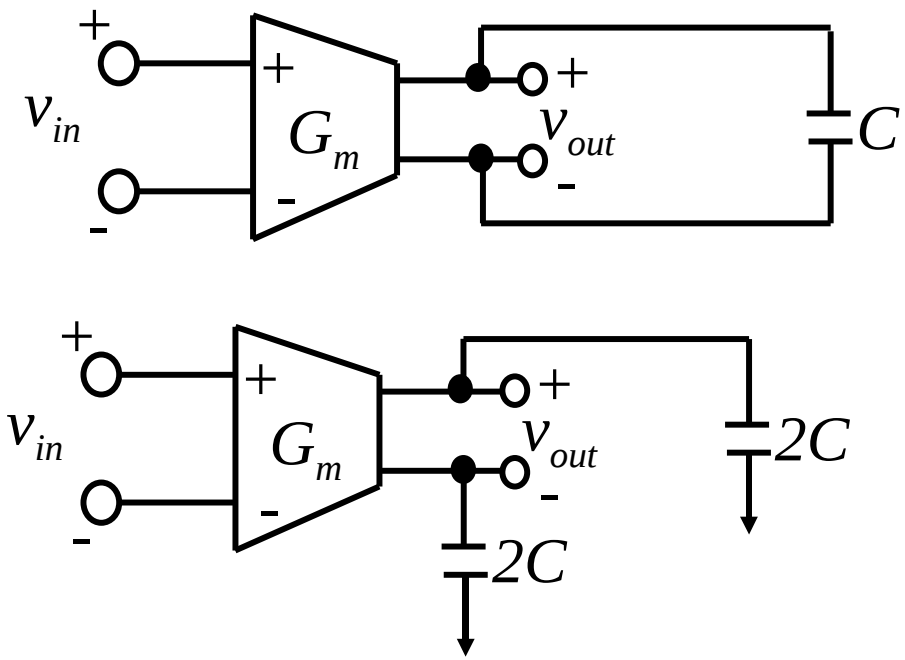
Lossy integrator with differential input



$$\frac{v_{out}}{v_{in}} = \frac{G_{m1} / G_{m2}}{1 + s \cdot \left(C / G_{m2} \right)}$$

Similar to a parallel RC

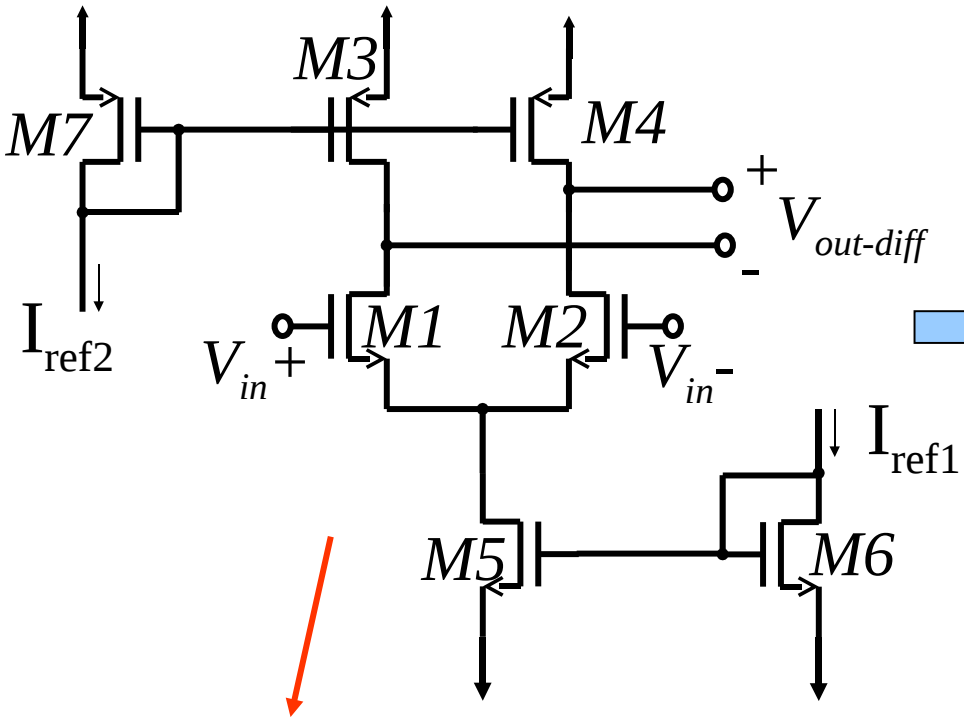
Fully differential Gm-C integrator

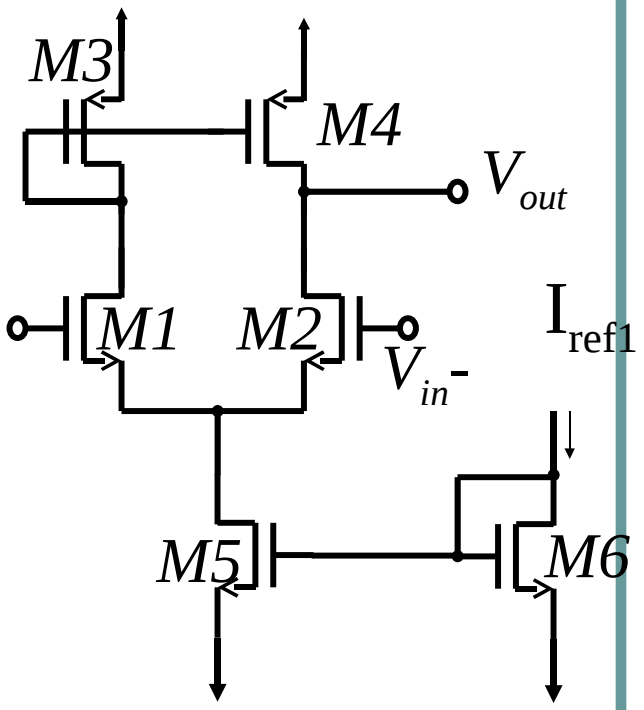


Which configuration is preferred?

Differential architecture needs common-mode feedback (CMFB)

Example

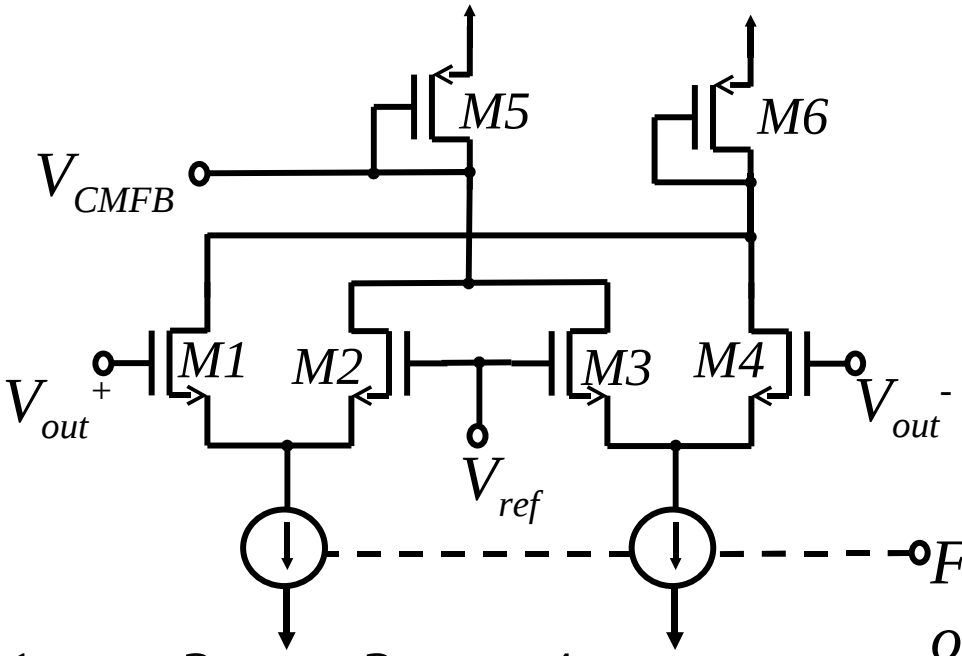




Quiescent value of CM output voltage is very sensitive to "I_{ref1}-I_{ref2}".

Internal CMFB!

CMFB - Example



From the bias voltages of the main circuit

$$gm1 = gm2 = gm3 = gm4 = gm$$

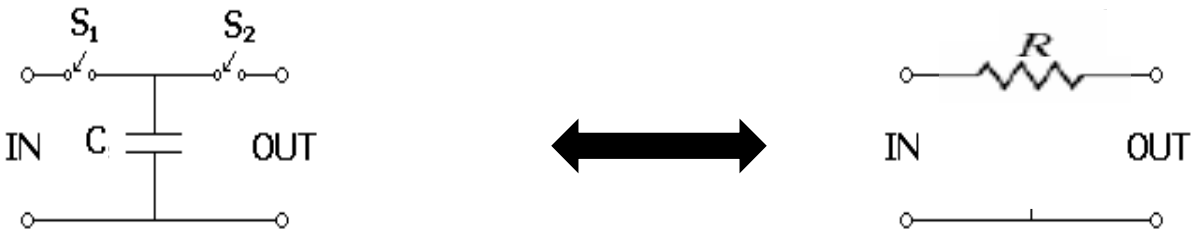
$$\Delta I_5 = gm \cdot \left[V_{ref} - \left(\frac{V_{out}^{+} + V_{out}^{-}}{2} \right) \right] \Rightarrow \frac{\Delta V_{CMFB}}{\Delta V_{out_{CM}}} = \frac{gm}{gm5}$$

More details will be given in the lecture.

Switched-Capacitor (SC) Filters

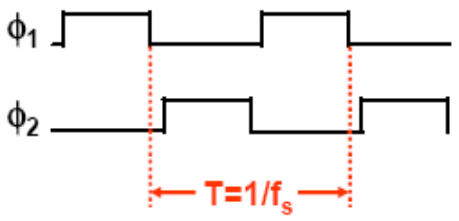
- SC filters are discrete-time or sampled-data equivalents of continuous-time filters.
- SC circuits eliminate resistors in filters by replacing them with capacitors and switches.
- Filter time constants are a function of capacitor ratios and clock frequency.

Emulating a Resistor by a Switched-Capacitor Circuit



- Two-phase non-overlapping clocks are used to control switches S1 & S2.
- Charge transferred from Vin to Vout during each clock cycle is:

$$\mathbf{Q = C(Vin - Vout)}$$



- Average current flowing from Vin to Vout is:

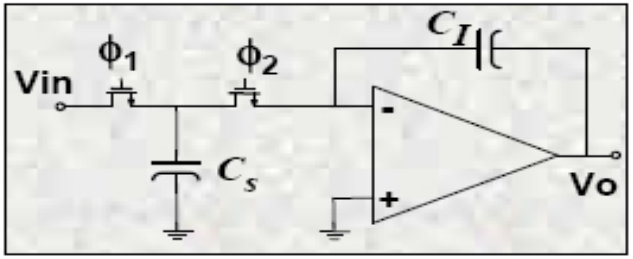
$$\mathbf{i = Q/t = Q.f_s}$$

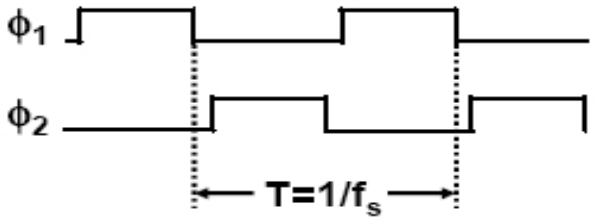
$$\mathbf{i = f_s.\ C(Vin - Vout)}$$

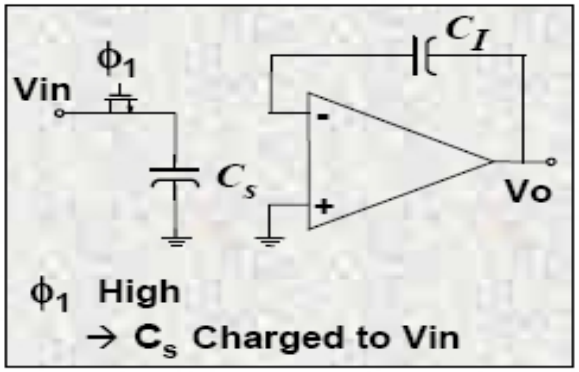
- With the current through the switched capacitor resistor proportional to the voltage across it, the equivalent "switched capacitor resistance" is:

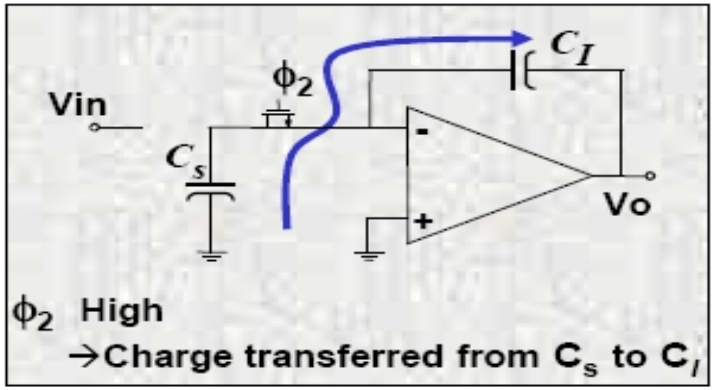
$$\mathbf{Req = 1/(f_s.C)}$$

Switched-capacitor Circuits: Integrator









EECS 247 Course slides, UCB

- For $f_{signal} << f_{sampling}$ $V_o = \frac{fs\ x\ Cs}{Ci} \int Vin\ dt$
- $\omega_o = f_s\ x\ (C_s / C_I)$

More details will be given in the lecture.