Current Mode Interconnect

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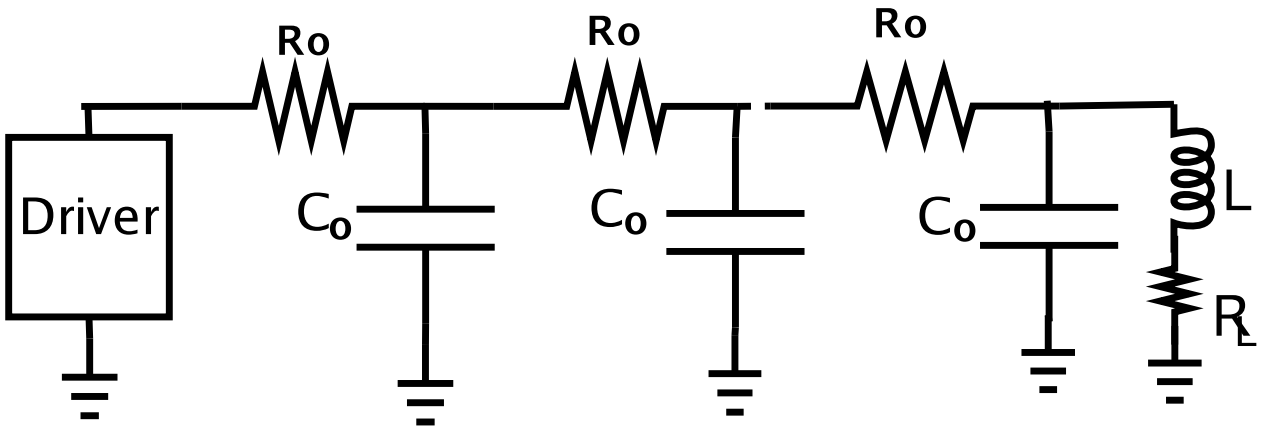
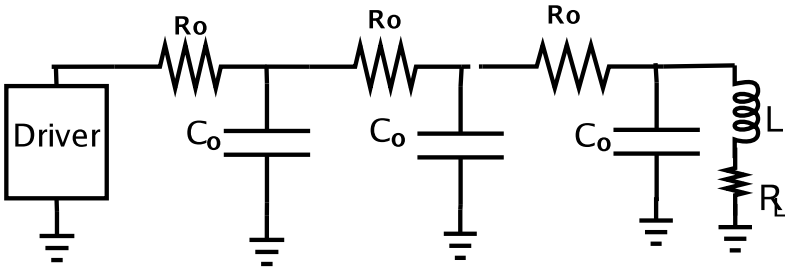
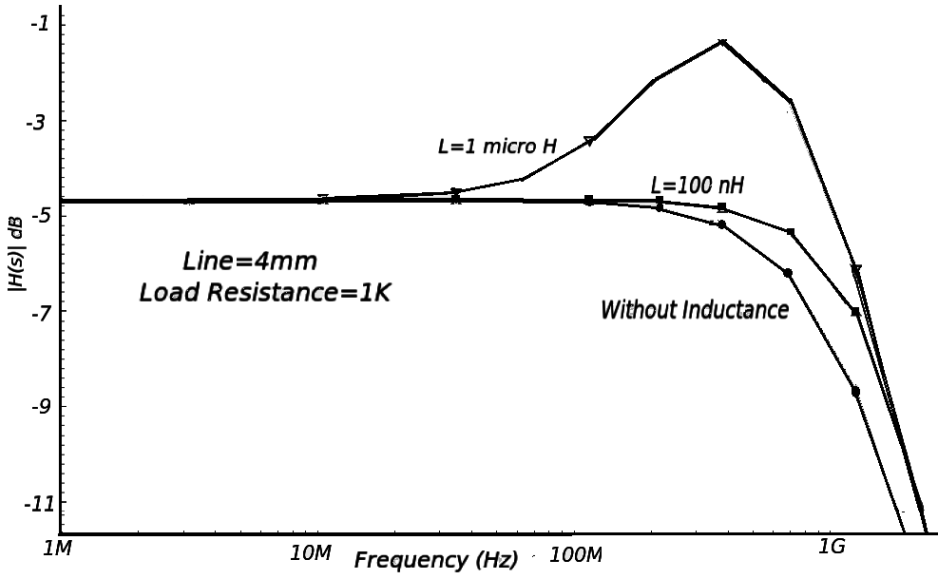
Inductive Peaking for Bandwith Enhancement



- On-chip interconnects can be modeled as distributed RC which is essentially a low pass filter
- Bandwidth Enhancement techniques employed in on-chip I/O buffers and RF amplifers can be employed for bandwidth enhancement of interconnects

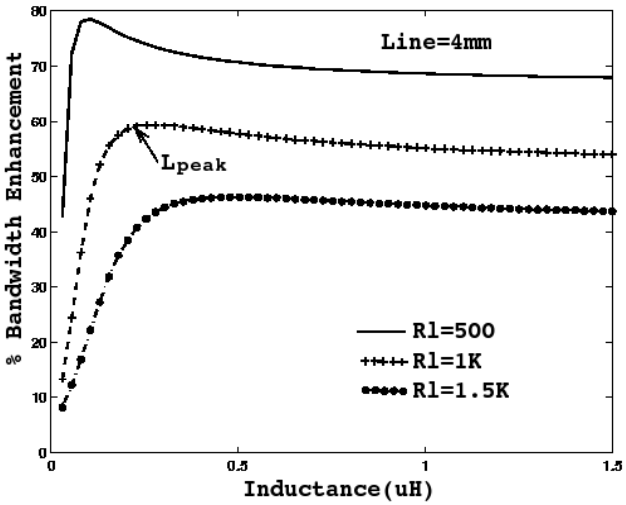
Inductive Peaking for Bandwith Enhancement





- One way of enhancing bandwidth is through Inductive Peaking.
- Inductive impedance is used as line termination.
- Output developed across the inductor has a high pass characteristic, which counters the low pass character of the wire.
- Shows enhancement of around 500MHz in 3dB bandwidth.

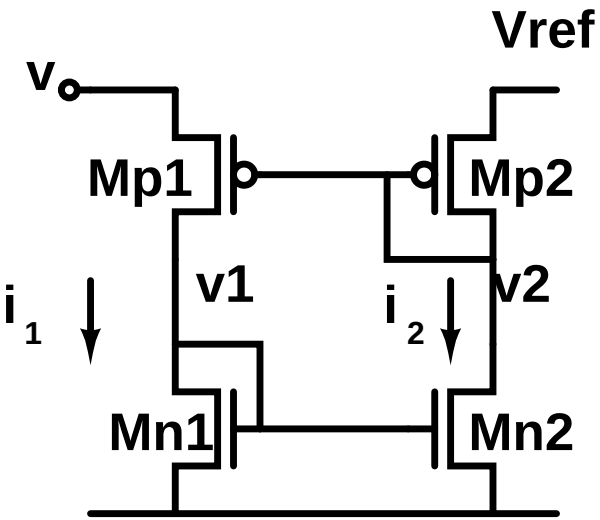
Bandwidth Enhancement Vs Load Inductance



- For a given line length, the amount of bandwidth enhancement is a function of inductance and load resistance.
- Significant bandwidth enhancement can be achieved for a wide range of inductance values greater than L_{peak}.
- Required inductance for significant enhancement in bandwidth is a few hundreds of nano Henries !!
- An active inductor is required

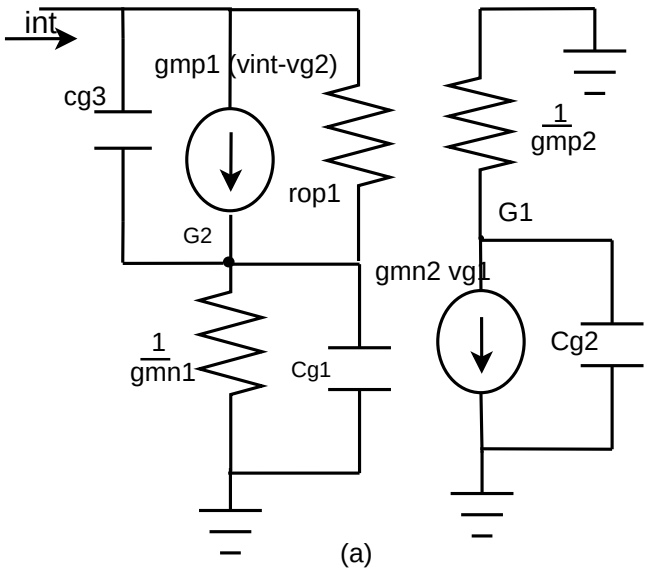
Beta Multiplier: A Gyrator

Beta Multiplier Circuits can exhibit inductive input impedance for some frequency range if designed properly.



A Beta Multiplier is essentially a gyrator circuit with two Gm elements connected back to back and parasitic capacitance of the transistors.

Beta Multiplier: Input Impedance



$$\text{Let } \tau_1 = \frac{C_{g1}}{g_{mn1}} \quad \tau_2 = \frac{C_{g2}}{g_{mp2}} \quad R_1 = \frac{1}{g_{mn1}}$$

$$\tau_3 = C_{g3} r_{op1} \quad \tau_4 = \frac{C_{g3}}{g_{mp1}} \quad R_3 = r_{op1}$$

$$\gamma = \frac{g_{mp1}/g_{mp2}}{g_{mn1}/g_{mn2}} \qquad \frac{R_1}{R_3} = k$$

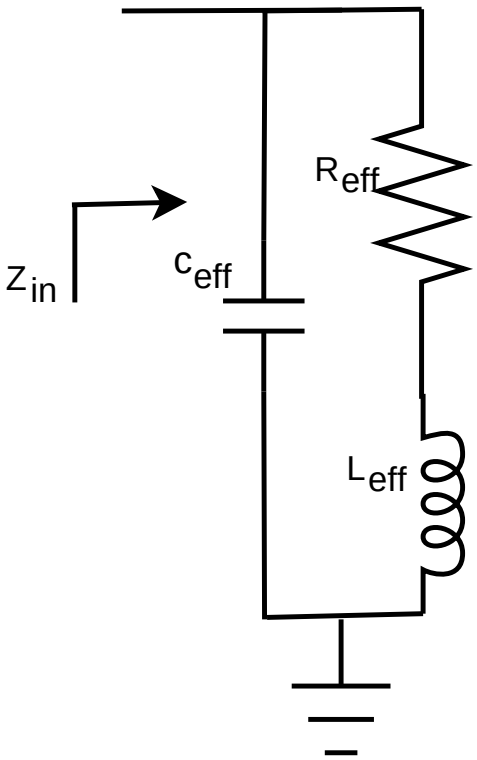
$$Z_{in} = \frac{\{(\tau_1\tau_2 + k\tau_2\tau_3)s^2 + (\tau_1 + \tau_2 + k(\tau_3 + \tau_2))s + 1 + k - \gamma\}}{\{(g_{mp1} + \frac{1}{R_3})\{(1 + \tau_1 s)(1 + \tau_2 s)(1 + \tau_4 s)\}\}}$$

$$R_{in} = \frac{(1 - \gamma) + \frac{1}{g_{mn1} r_{op1}}}{g_{mp1} + \frac{1}{r_{op1}}}$$

Beta Multiplier : Equivalent Circuit

$$Z_{in} = \frac{\{(\tau_1\tau_2 + k\tau_2\tau_3)s^2 + (\tau_1 + \tau_2 + k(\tau_3 + \tau_2))s + 1 + k - \gamma\}}{\{(g_{mp1} + \frac{1}{R_3})\{(1 + \tau_1 s)(1 + \tau_2 s)(1 + \tau_4 s)\}\}}$$

- Relative location of poles and zeros determine nature of impedance (inductive of capacitive)
- If the first zero occurs a decade prior to the first pole, input impedance is inductive
- $\gamma - \frac{1}{g_{mn1}r_{op1}} > 0.9$ and any two time constants being equal ensures that a zero occurs a decade prior to the first pole

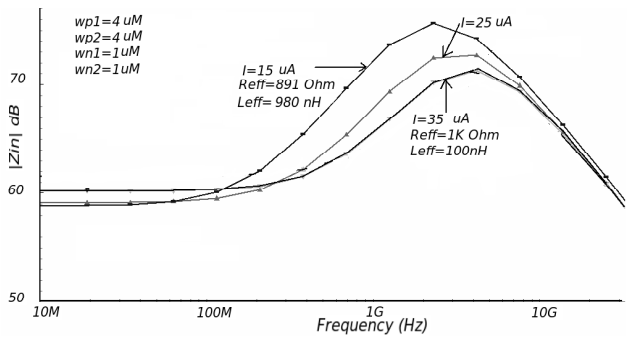


$$R_{eff} = \frac{(1-\gamma) + \frac{1}{g_{mn1} r_{op1}}}{g_{mp1} + \frac{1}{r_{op1}}}$$

$$C_{eff} = K C_{gx}$$

$$L_{eff} = \frac{r_{op1}}{g_{mp1} r_{op1} + 1} \left\{ \frac{C_{g1}}{g_{mn1}} + \frac{C_{g2}}{g_{mp2}} + \frac{C_{g2}}{g_{mp2} g_{mn1} r_{op1}} + \frac{C_{g3}}{g_{mn1} g_{mp1} r_{op1}} \right\} \quad (1)$$

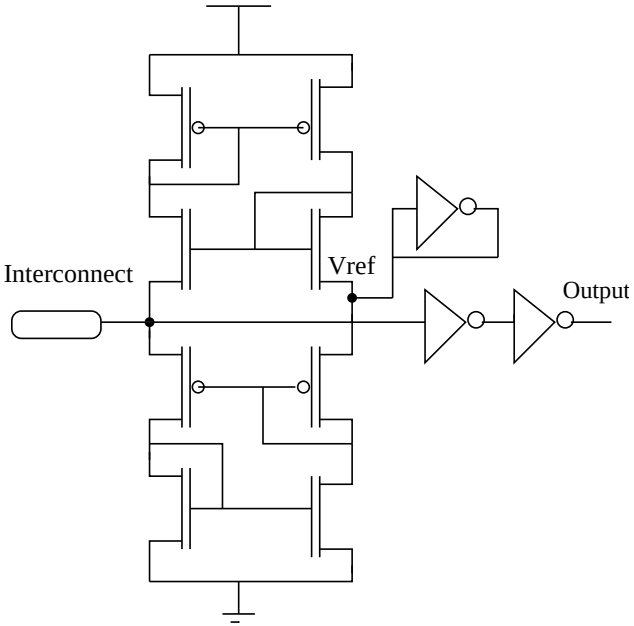
Beta Multiplier : Input Impedance Control



It is possible to generate effective inductance of hundreds of nano Henries for a practical range of input current and transistor geometries using beta multipliers.

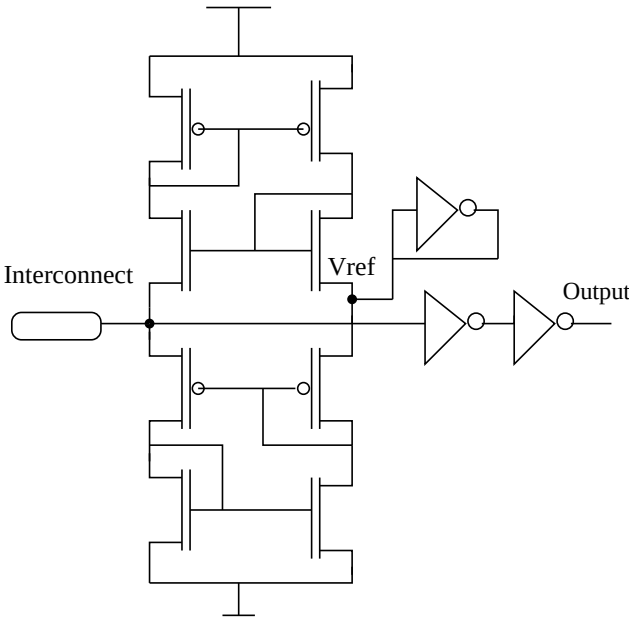
- Their effective resistance can be controlled by ratios of transconductances while its effective inductance depends on the absolute value of transconductance.
- It is possible to control R_{in} and L_{eff} with very little interaction between the two.
- Inductance changes from 100nH to 980nH while the value of effective resistance remains within 12% of its nominal value for $20\mu A$ change in the current.

Current Mode Receiver Circuit with Beta Multiplier



- Effective impedance offered by the receiver is equal to the parallel combination of impedance offered by individual beta multipliers.
- Voltage at node linerx swings around V_{ref}. A small voltage swing on the line is sensed and amplified by receiver amplifier.

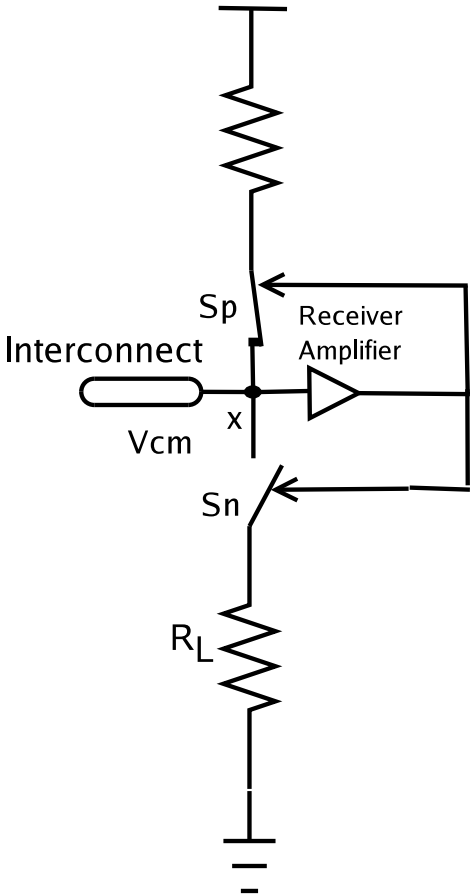
Current Mode Receiver Circuit with Beta Multiplier



- V_{ref} is generated by shorting the input and the output of an inverter, so that the value of V_{ref} is the same as the switching threshold of the receiver amplifier across all process corners.
- V_{ref} generation circuit consumes static power.

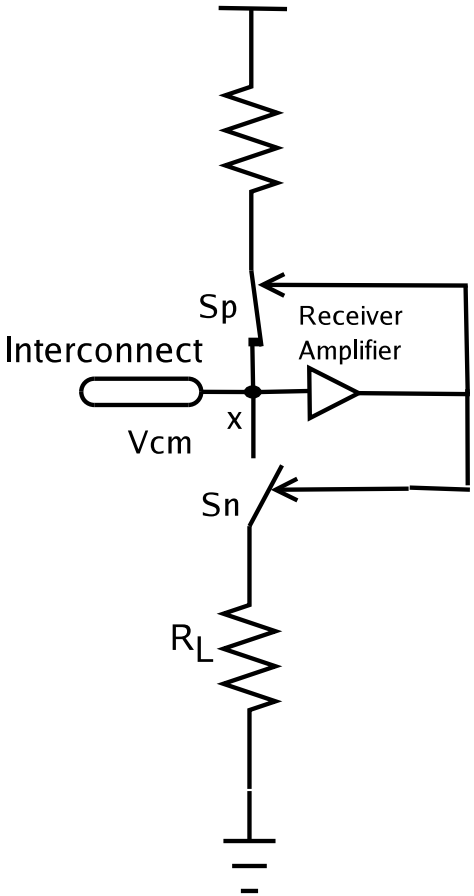
r_{out} of V_{ref} generation circuit comes in series with beta multiplier Z_{in} and hence, the beta multiplier has to be sized accordingly.

Current Mode Receiver Circuit: Dynamic Input Impedance



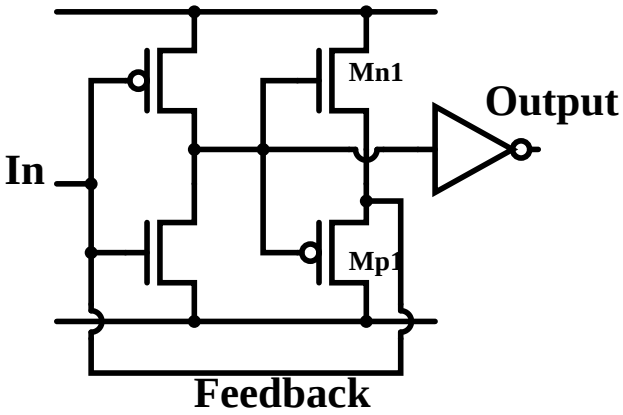
- We would like the receiver circuit to initially offer high impedance (while the transmitter is charging the line) and later (in steady state) to offer a small resistance.
- It is possible to achieve this by using feedback.

Current Mode Receiver Circuit: Dynamic Input Impedance



- In steady state either of the two switches Sn and Sp, is ON. The state of these switches is controlled by the receiver amplifier. The state (ON/OFF) of these two switches flips as voltage on line flips with input transition.
- Because of delay through the receiver amplifier, the interconnect node is a high impedance node during input transition, enabling faster charging/discharging of line capacitors.

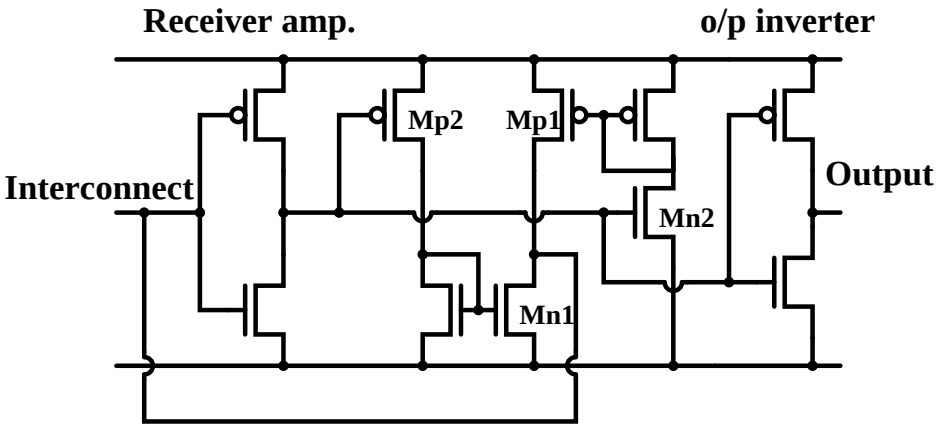
A Receiver with Source Follower feedback



Feedback is enabled when the output of the first inverter changes by more than V_{Tp} or V_{Tn}, turning on either the n or the p source follower.

- Feedback prevents any further change in the line voltage.
- The receiver circuit will cause somewhat higher voltage swing on line because of non-zero V_{sb} of transistor Mn1.
- The operating points of source follower and receiver amplifier may not be same under all process corners.

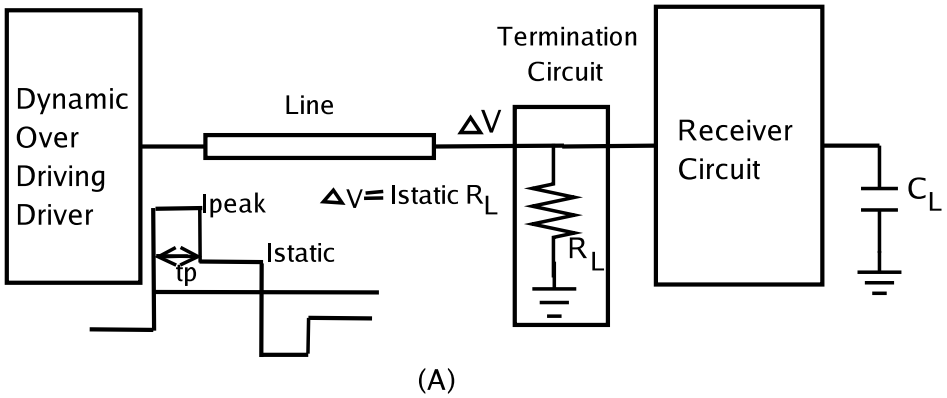
A Current Mode Receiver with Dynamic Input Impedance

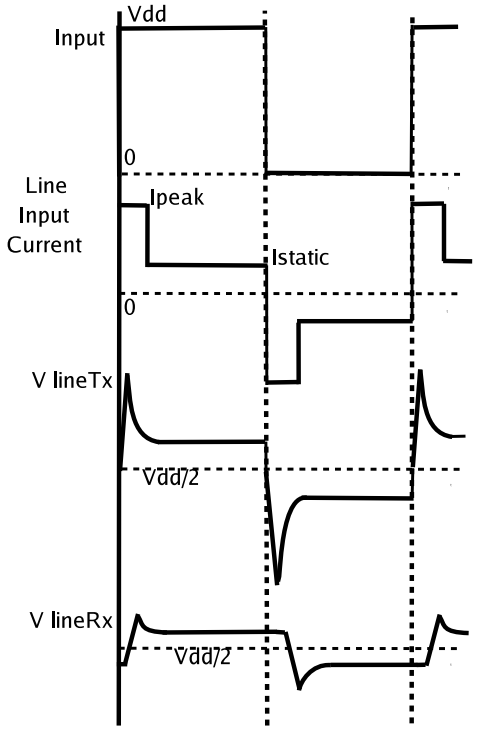


In this receiver proposed by Katoch *et al*, either Mp1 or Mn1 is ON in steady state.

- The arm with the ON transistor consumes static power.
- It offers very low input impedance.
- If higher input impedance is required, long channel transistors must be used, which increases the delay of the receiver circuit.

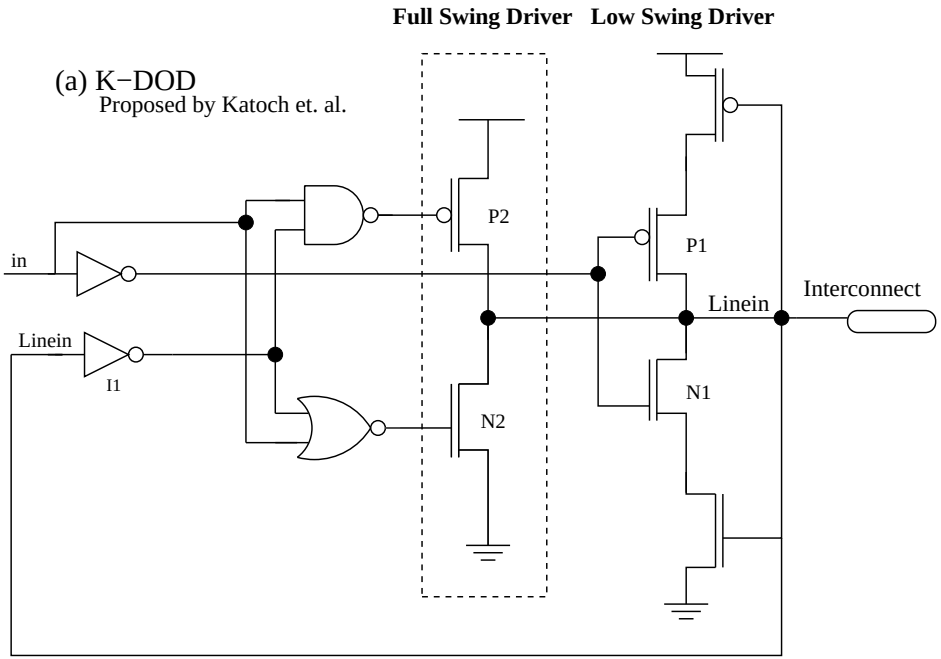
Dynamic Overdriving: Concept





- Dynamic overdriving means driving an interconnect by large current during input transition and by small current for the rest of the period.
- In frequency domain, DOD means magnifying high frequency components of input signal.

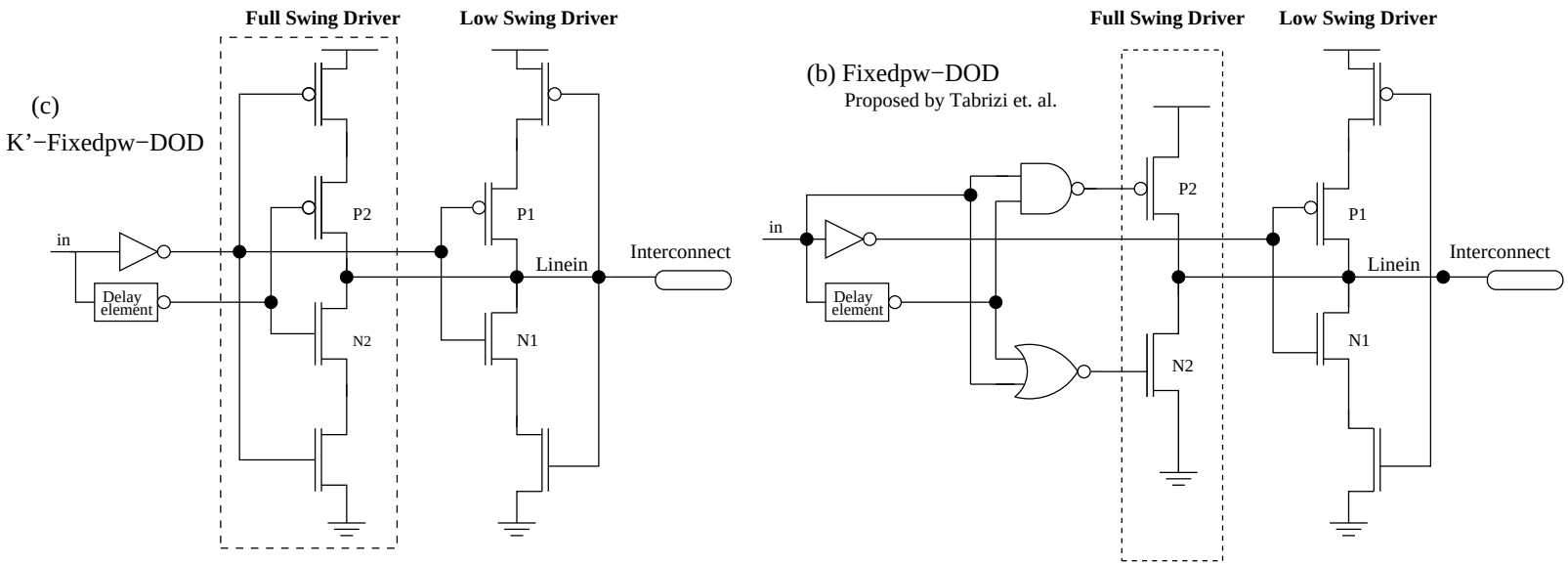
Dynamic Overdriving Driver Circuits



In this driver circuit proposed by Katoch *et al*, the full swing driver provides large current during input transition.

- The full Swing driver is turned off as soon as line voltage crosses switching threshold of the inverter I1.
- Small swing driver either sources or sinks current from the line depending on the input bit.
- Input to the feedback inverter is not full swing. Hence it consumes static power.

Dynamic Overdriving Driver Circuits



- In the driver circuit suggested by Tabrizi et. al. the full swing driver is turned off after a fixed time period given by delay element.
- The driver circuit of Figure C eliminated the big NAND and NOR present in the driver proposed by Tabrizi et. al.

Simulation Setup

- Technology $0.18\mu m$ UMC, $V_{dd} = 1.8$
- All signaling systems are designed such that they present equal input capacitance ($1\times$Minimum sized inverter) and drive the same load of four min sized inverters(FO4).
- Interconnects modeled as a 5section RC: $R_0 = 178\Omega/mm$, $C_0 = 0.192pF/mm$, $L = 0.5nH/mm$

Comparison of Receiver Circuits: Speed and Power

- Receiver circuits are designed for line voltage swing of 50mV. The designed source follower receiver offers 65mV of voltage swing.
- Driver circuit K'Fixedpw-DOD is designed for overdrive current(I_{peak}) of 200μA.
- Power is measured at 1Gbps and delay measured at 100Mbps

Driver + Receiver	Power (μW)	Delay (ns)	Throughput (Gbps)
K'-Fixedpw-DOD + Diode	452	1.5	1.0
K'-Fixedpw-DOD + Beta Multiplier	450	0.964	1.25
K'-Fixedpw-DOD + Katoch	445	1.19	1.1
K'-Fixedpw-DOD + SF	423	1.29	1.15

Comparison of Driver Circuit:Power and Delay

- All three driver circuits are designed for the same overdrive current ($I_{peak} = 400\mu A$) and overdrive duration ($t_p = 130ps$).
- The designed drivers Fixedpw-DOD and K'-Fixedpw-DOD employ the same inverter chain(three minimum sized inverters).

Driver	Power(μW)	Driver Delay (ps)
K-DOD	464	190
Fixedpw-DOD	273	156
K'-Fixedpw-DOD	252	152

Why Process Variation Tolerant

- In modern technologies, 3σ variation in device parameters is 40% of their nominal value.
- Variation in delay of interconnects with buffer insertion scheme makes timing verification of modern SOCs an iterative task.
- In an SOC, driver and receiver circuits of a repeaterless current mode signaling scheme are very much likely to be at different parts of the chip. Transistor parameters of driver and receiver may not be identical. This can degrade throughput or even correctness of data transmission.
- Hence, a current mode signaling scheme which is robust against inter-die and intra-die process variations is required.

Parameters Affecting Performance

The speed of a current mode signaling scheme with dynamic overdriving driver is a strong function of the following parameters.

a) Voltage Swing on line (ΔV)

b) Duration for which strong driver is ON (t_p)

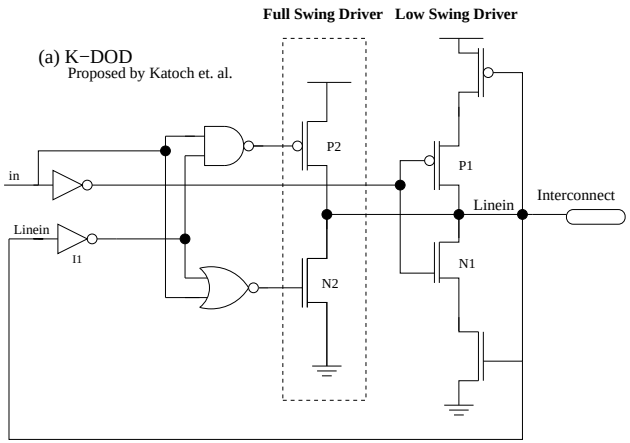
c) Current supplied by the strong driver during input transitions (I_{peak})

Variations in any of these three parameters cause significant variations in the speed of a CMS with dynamic overdriving

Performance of Current Mode Schemes with Process Variation

- CMS scheme proposed by Katoch et. al. performs well across all process corners when transistor parameters of transmitter and receiver are identical. Its performance degrades significantly in the presence of intra-die process variations.
- CMS scheme proposed by Tabrizi et. al. is less sensitive to intra-die process variations but its throughput degrades significantly in the worst process corner.
- The perfomance of this scheme is worst in the skewed corners where speed of logic circuit doesn't degrade much. Hence, with this scheme interconnects can become a bottleneck in the overall speed of the chip.
- We have deleloped a new CMS scheme that performs well under inter-die and intra-die process variations.

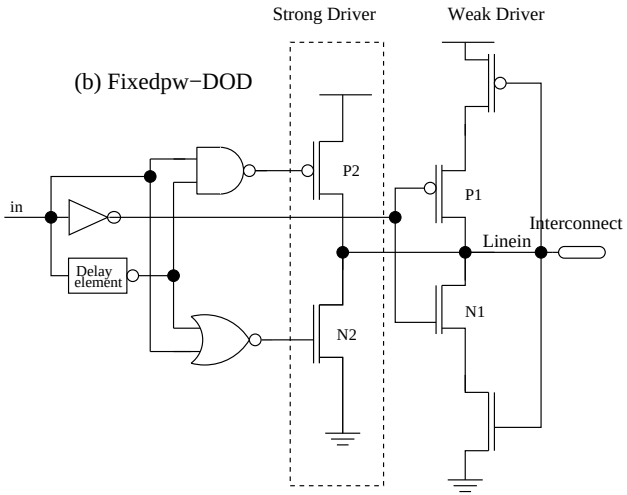
Analysis of Existing Current Mode Signaling Schemes



- **Proposed by Katoch et. al.**: The driver circuit employs a feedback inverter which controls turning off of the strong driver. Receiver employs an inverter as an amplifier to amplify small voltage swing on the line.
- Here, steady state voltage swing at receiver end should be more than the mismatch between switching threshold(V_M) of the transmitter and the receiver inverter for faithful reproduction of the signal.

- Mismatch in V_M leads to a large difference in rise delay and fall delay of the scheme which leads to degradation in data rate.
- In corner based analysis the entire chip is in the same corner. For identical inverters at transmitter and receiver, the scheme is very robust against four corner variations.

Analysis of Existing Current Mode Signaling Schemes

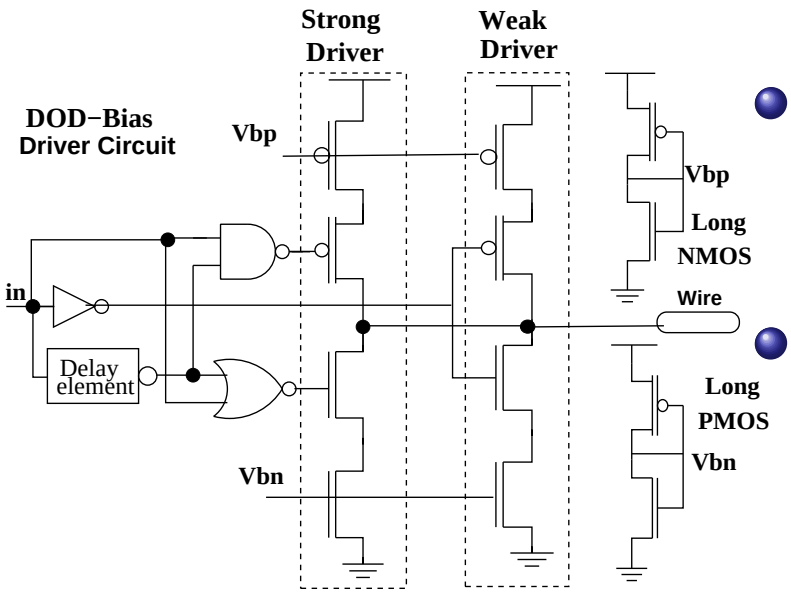


- Less sensitive to V_M mismatch between driver and receiver inverters as ON duration of the strong driver is determined by the delay element.
- In SS and FF corners, change in I_{peak} is somewhat compensated by change in ON duration in the opposite direction.

- In skewed corners, the I_{peak} changes significantly while delay of delay element remains nearly unchanged.
- Leads to difference in rise and fall delays which causes degradation in throughput.
- In skewed corners, steady state voltage swing on line is also uneven around switching threshold of receiver amplfier.
- Performance of this sginaling scheme degrades significantly in the skewed corners where speed of logic circuit does not degrade much.

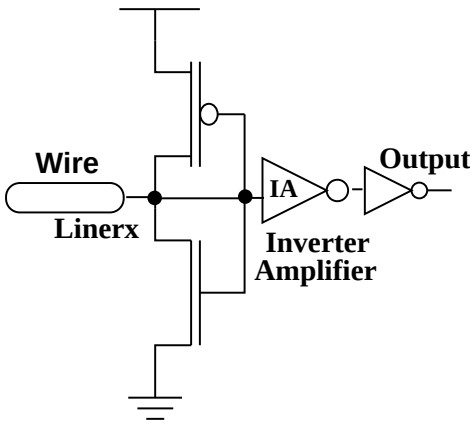
Proposed Current Mode Signaling Scheme: Driver Circuit

Why not to employ constant current source at driver ?



- Duration for which strong driver is ON is controlled by delay element.
- I_{peak} and current supplied by weak driver (I_{static}) is controlled by bias voltages Vbp and Vbn.
- In Vbp generation circuit small PMOS transistor acts as process corner sensor and a long channel NMOS transistor which acts as a resistor.
- The bias voltages Vbp and Vbn are close to Vdd/2 in typical process corner. These bias voltages,Vbp or Vbn, are lower or higher than Vdd/2 based on process corner.

Proposed Current Mode Signaling Scheme: Receiver Circuit



- Diode connected inverter followed by inveter amplifie The amplifier inverter can also be seen as a current comparator that compares current through PMOS an NMOS.
- The diode connected inverter and receiver amplifier (inverter IA) are designed using fingers and placed close to each other so that their switching thresholds are nearly same under all process conditions.
- With proposed driver and receiver, voltage swing on line ΔV remains nearly unchanged across process corners.
- $\Delta V = I_{static} R_L$, Where $R_L = \frac{1}{gm_p + gm_n}$.
- In FNSP and SNFP corners, R_L and I_{static} both remain nearly unchanged.

Simulation Setup

- Technology $0.18\mu m$ UMC, $V_{dd} = 1.8$
- All signaling systems designed such that they present equal input capacitance ($1\times$Minimum sized inverter) and drive same load of four min sized inverters(FO4).
- All the signaling schemes, current mode and voltage mode, are designed for throughput of 2.5 Gbps in typical process corner.
- All the CMS schemes are designed for a given voltage swing on line based on sensitivity of the circuit to on-chip PVT variations.

Minimum Voltage Swing on Line

- **Vdd Vaiations:** 5% (of Vdd) signal related and 5% signal unrelated variation in both Vdd and Vss. Signal unrelated variations are modeled as triangular wave of 2GHz frequency. Vdd and Vss change in opposite direction reducing magnitude of supply by 10%.
- **Temperature Variations:** Transmitter and receiver are assumed to be operating at $30°C$ and $130°C$ respectively.
- **On-chip process variations:** 33.33% of overall process variations given in model file provided by the foundry. The worst case for on-chip process variations is when all transistors of transmitter are in TT_{SNFP} or TT_{FNSP} corner and all the transistors of receiver are in TT_{FNSP} or TT_{SNFP} corner.

CMS system	Line Voltage Swing (mV)		
	Process	Voltage	Temp

Spped-Power-Area Comparison

- In the proposed scheme bias generation circuit will be shared by all the wires in a bus. Considering typical bus width of 16, one by sixteenth of power and area of bias generation circuit is added in total power and area of a single wire.

Signaling Scheme	Delay (ps)	Throughput (Gbps)	Power (μW)	Area (μm^2)
Proposed CMS	490	2.63	113	3.07
CMS-Fb	570	2.77	140	2.00
CMS-Fpw	503	2.56	114	2.45
Voltage Mode	1100	2.85	655	12.53

- Proposed CMS scheme shows 14% and 19% improvement in delay and power, repectively over the CMS proposed by Katoch et. al

Effect of Inter-die Process Variations

- Seperate analyses for Inter-die and Intra-die Process Variations
- Throughput is defined as maximum rate at which data can be transmitted with $V_{OH} > 0.8Vdd$ and $V_{OL} < 0.2Vdd$. Throughput of a system is measured by applying 1000 random bits.
- The performance of CMS schemes with all six combination of drivers and receivers have been analyzed.

CMS system		Percentage Degradation	
Driver	Receiver	Delay	Throughput
DOD-Bias	Rx-D	22	**22.4**
DOD-Fb	Rx-D	16	15
DOD-Fpw	Rx-D	20	36
DOD-Bias	Rx-Fb	17	24

Effect of Inter-die Process Variations

- A 7-stage ring oscillator with each inverter driving FO4 load is considered as representative of logic core.

Signaling System/ Logic Circuit		Percentage Variation			
		SS	FF	SNFP	FNSP
DOD-Bias	Rx-D	-22.4	+6	**-7**	**-7**
DOD-Fb	Rx-D	-14	< 2	**-3**	**-4**
DOD-Fpw	Rx-D	-22.4	+10	**-34**	**-33**
Voltage Mode		-27	+6	< **1**	**-2.8**
Ring Oscillator Freq.		-23	+19.0	**-2.88**	**-3**

- The degradation in throughput of CMS with the driver DOD-Fpw is large and the worst case corner for throughput is SNFP.
- The proposed signaling scheme requires some amount of overdesign so that interconnects do not become bottleneck

Effect of Intra-die Process Variations

- The worst case for intra-die process variations is when all the transistors of transmitter are in TT_{SNFP}/TT_{FNSP} while all the transistors of receiver are in TT_{FNSP}/TT_{SNFP} corner.

CMS system		Percentage Degradation	
Driver	Receiver	Delay	Throughput
DOD-Bias	Rx-D	4	**9.5**
DOD-Fb	Rx-D	16	36
DOD-Fpw	Rx-D	6	16
DOD-Bias	Rx-Fb	10	12
DOD-Fb	Rx-Fb	13	**33**
DOD-Fpw	Rx-Fb	10	**14**

- In the worst case of on-chip process variations this process conditions logic frequency degrades by less than 1%.
- The degradation in throughput of the CMS scheme with the