Simulation and Fabrication of Novel MOS Device Architectures

A dissertation submitted in partial fulfillment of
the requirements for the degree of

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by

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This work is dedicated to my parents

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Declaration of Academic Ethics

I declare that this written submission represents my ideas in my own words and where others′ ideas or words have been included, I have adequately cited and referenced the original sources. I declare that I have properly and accurately acknowledged all sources used in the production of this thesis.

I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

Date: June 28, 2012

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Abstract

The scaling limitations of conventional MOSFET necessitates new MOS device architecture That can operate at low power applications. The study of novel MOS device architectures that can replace conventional MOSFETs in ultra sub-micron technology is the main aim of this project. “Tunnel FET (TFET)” is a promising device that can operate in deep sub-micron regime due to its low subthreshold swing and the absence of short channel effects. Tunnel FET works based on the principle of Band-to-Band tunneling, this tunneling rate can be improved by using sharp doping profiles at source-channel interface. With the existing epitaxial growth of thin film techniques sharp doping profiles can be achieved in vertical direction, which calls for study of vertical Tunnel FETs. Three types of vertical TFET device architectures was proposed and simulated, structure of the vertical TFET was optimized based on device level performance. A Solid phase epitaxial regrowth technique have been used to optimize the depositing conditions of amorphous Silicon on heavily doped substrate in fabricating the vertical Tunnel FET. An advanced tunneling model called as “Dynamic nonlocal tunneling model” was used in simulating Tunnel FETs.

When the channel length scales down to sub 20 nm regime, the conventional MOSFET requires sharp doping profiles at source-channel and drain-channel interfaces in order to overcome punch through effect. So the “Junction less transistors (JLT)” that do not have any junctions along the source-channel-drain path is an interesting device in ultra short channel regime. ZnO is a transparent, wide bandgap semiconductor and is suitable for low cost opto-electronic devices. We proposed a new device architecture for ZnO based semiconductor on insulator-junction less transistor (SOI-JLT) and bulk planar junction less transistor (BPJLT) that effectively reduces the channel thickness by half. The proposed device has better scalability than existing JLT. An attempt was made in fabricating ZnO based JLT, a detailed process flow of ZnO based JLT and optimizing conditions for ZnO deposition are discussed.

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Chapter 1

Introduction

1.1 Introduction

The advancement in the silicon based CMOS technology lead to prominent growth in semiconductor industry over last few decades. Invention of transistor by William Shockley in 1949 created a revolution in the semiconductor industry. Later Metal Oxide semiconductor Field Effect Transistor (MOSFET) came in to industry and it currently rules the VLSI arena. These devices are very tiny and have less power dissipation compared to the bulky vacuum tubes. The Scaling of MOSFET has been following the Moor's law so that speed and packing density gets doubled for every two years. Transistors have been shrinking over the last few decades from the micrometer scale, now it reached in to nanometer regime.

Scaling of MOSFET is governed to achieve high speed and more packing density with low cost per chip. Continuous down scaling of conventional MOSFETs leads to fundamental limits that can no longer be overcome by technology innovation alone. Scaling of MOSFETS beyond sub 100 nm regime suffering from short channel effects [1] which limit the physical limit of scaling of MOSFETs. Today semiconductor industry is looking for low power and low operating voltage, however scaling of supply voltage in MOSFET is limited by Sub threshold Swing(SS) of 60 mV/dec which limits I_{ON}/I_{OFF} ratio. The thermionic emission of carrier injection in a MOSFET puts a lower limit on a SS at a value of 60 mV/dec at room temperature. This limitation necessitates study of new device architectures that use different modes of carrier injection.

"Tunnel FET" (TFET) which works based on the quantum mechanical Band to Band Tunneling is a potential device and exhibit good properties as compared to MOSFETS. TFET can

achieve very low off currents as well as temperature independent sub threshold swing. So, the study of this device is interesting for future VLSI applications. Tunnel FET is nothing but a gated p-i-n diode (Fig. 1 (a)) operated in reverse bias. The low off currents in the p-i-n diode gives low standby leakage currents of TFETs. Moreover the structural symmetry of p-i-n structure with that of a MOSFET offers the ease of fabrication with the existing CMOS technology.

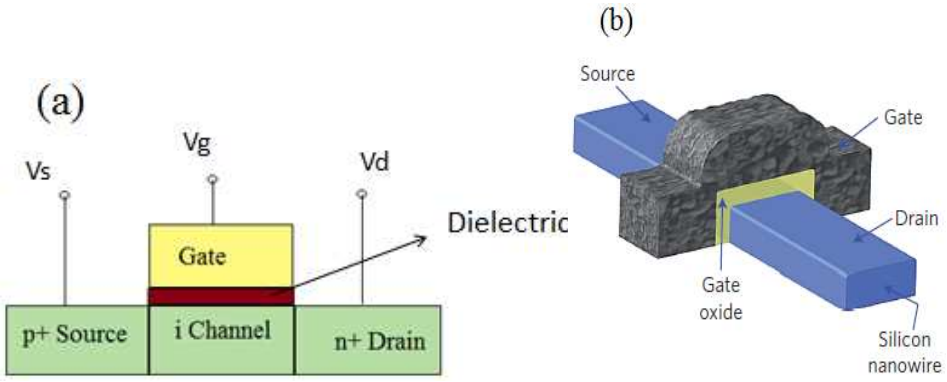

Figure 1.1: Schematic representation of (a) TFET and (b) JLT.

Several structures have been proposed for Silicon TFETs over the last few years. Vishwanath Nikam et al. [2] proposed horizontal SOI-TFET structures. Krishna K Bhuwalka et al. proposed vertical p-i-n structure TFET [3]. Even though TFET has less SS compared to MOSFET of comparable Gate length, Si-TFETs have low 'ON' currents which fail to meat the ITRS requirements [4] . Several device architectures with different geometries and materials have been explored to increase the 'ON' currents. Kathy Boucart et al. [5] reported that Double Gate Tunnel FET with High-k gate dielectric at least doubles the I_{ON}, while I_{OFF} is still in the fA or pA range. Krishna K Bhuwalka et al. [3] reported that a δp+ SiGe layer near the source-channel interface lowers the tunneling barrier height and hence increases the 'ON' current but at the same time 'OFF' current also increases. Hasanali Virani et al. [7] proposed "Dual-κ spacer TFET structure" which gives better I_{ON} compared to the traditional TFETs. TFET has different scaling rules in comparison to conventional MOSFETs. Krishna K Bhuwalka et al. [8] reported that parameter like V_T, subthreshold slope (SS) improved with t_{ox} scaling and independent with Gate length scaling.

Another serious Short channel effect that limits the scaling of MOSFET below sub 20 nm regime is punch through. As the channel length scales down below 20 nm, the two junctions formed at the source-channel, drain-channel interfaces will merge and form a direct path between source and drain, thus may loose transistor action. To avoid this one needs to use steep

doping profiles at source-channel and drain-channel interfaces, but due to dopant fluctuation in lateral direction achieving steep doping profiles is a chalanging task. The novel device like Junction less transistor (JLT) that do not have any junctions along the channel will therefore be an efficient device in nano scale regime. JLT is nothing but gated nano wire resistor as shown in the Fig. 1(b). The channel is heavily doped semiconductor and gate controls the current flowing through it. The Work function of gate material is such that it should deplete the entire channel in the off state. The positive voltage at the gate brings the device out of depletion and there is a direct conduction path between source and drain.

The concept of multi gate control can be applied to JLTs also. Jean-Pierre Colinge et al. [18] reported that the fabricated Si-nano wire gated resistors have full CMOS compatibility and near ideal sub threshold swing of 60 mv/dec. J.P. Colinge et al. [**?**] reported that simulated SOI JLT offer better SS and DIBL than tri gated MOSFETs. Chi-Woo Lee et al. [20] superimposed the carrier concentration contour lines of JLT and MOSFET on gray scale representation of the norm of the electric field. They found that in MOSFETs peak electron concentration coincides with the region of high electric fields, where as in JLT peak electron concentration coincides with the region of low electric fields and thus mobility degradation can be relaxed in JLT once device size reaches to nano scale level. Sung-Jin Choi etc al [21] experimentally investigated that V_t is very sensitive to width of the Si-nano wire in JLT than that of conventional MOSFET because in JLT channel is heavily doped. Chi-Woo Lee et al. [22] proposed a technique to improve SS by impact ionization and they found that its impact is more pronounced in JLT compared to normal MOSFET because region over which impact ionization takes place is much larger in JLT than that of MOSFET. Suresh Gundapaneni et al. [24] proposed Bulk planar JLT for the first time which can be made an idea of junction isolation rather than dielectric isolation used in SOI JLT. They found that BPJLT offers better scalability than the SOI JLT by reducing effective device layer thickness by half of its physical thickness, also BPJLT offers wide tuning range for I_{OFF} and I_{ON} by tuning well bias and well doping simultaneously.

For particular gate material the off state leakage current of JLT depends on channel thickness. If channel is very thin it is easy to switch the JLT from ON state to OFF state and vice-versa and thus growing thin films on SOI substrate is an interesting topic. The transparency and conductivity properties of Zinc oxide (ZnO) makes it suitable for fabrication of thin film transistors (TFT) [23]. ZnO is a wide and direct bandgap semiconductor and has many applications in optoelectronic devices. Moreover, higher electrical conductivity, mobility and larger binding

energy make ZnO films suitable for transparent thin film transistors, laser diodes and photo detectors. ZnO has wurtzite crystal structure with bandgap of 3.3 eV. Due to this large band gap, device made up of ZnO can have higher breakdown voltages and ability to sustain large electric fields and high temperatures. Furthermore, bandgap of ZnO can be tuned in the wide range by alloying with magnesium oxide (MgO) or cadmium oxide (CdO) [35]. Since ZnO is reactive to most acids, ZnO films can easily etched by wet chemical etching and adds better flexibility in the processing and integration of electronic and opto-electronics devices. ZnO thin films can be made by MOCVD, MBE, sputtering and sol-zel methods.

Irrespective of growth method, as grown ZnO films always act as an n-type semiconductor, hence the junctionless device architecture is of interest for ZnO transistors. As discussed in the literature [25], the unintentional n-type conductivity is due to presence of native defects like Zinc interstitials and oxygen vacancies. However most of the arguments based on hypotheses that reduction of electrical conductivity as the oxygen partial pressure increases. According to [33, 34], oxygen vacancies in ZnO are deep donors rather than shallow donors and cannot contribute any electrons to conduction band, so subject remain controversial.

Controllable n-type doping can be achieved by adding impurities like Al, Ga, In, F and Cl etc. The group III impurities Al, Ga and In when substituted on Zn sites, extra valence electron of these impurities is loosely bounded, can easily excited to conduction band and is free to move. Similarly the group VII elements like F, Cl have one more valance electron than O, when substituted on O site act as shallow donors in ZnO. The p-doped ZnO is difficult to get, because of low solubility of p-type dopants and their compensation by unintentional n-type impurities. In the literature [35], it is discussed that elements like Li, Na, N and Cu etc behave like p-type impurities in ZnO, but getting Stable p-doped ZnO films is still under research.

Rf sputtering is a frequently used method for making ZnO films. The film quality depends upon deposition parameters like process gas pressure, substrate temperature and rf sputtering power. The increase in substrate temperature, rf power and decrease in process gas pressure leads to enlargement in grain size and enhanced crystallinity [27, 28]. Increasing rf power or decreasing pressure also leads to reduction of resistivity and hence improvement in carrier mobility and concentration [28, 29]. But Wang Xiaojing et al. [26] reported that as pressure increases, crystallinity and grain size of AZO film increasing first and then deteriorated. This is due to the bombardment of high energy particles to film surface is less in the low pressure regime, where as in high pressure regime as pressure increases particles collide with gas

molecules and results in reduced sputter yield. The post annealing treatment enhances the crystallinity of ZnO films, but annealing ZnO films to very high temperature creates a compressive stress in ZnO films if thermal expansion coefficient of ZnO is greater than the underlying substrate. Z. B Fang et al. [32] reported that ZnO films annealed in the temperature region of 450-600^{O}C has angular peak position (2 theta) nearer to its powder value, and films annealed in this regime are stress free. The ZnO films annealed in the temperature regime of 450-600^{O}C have highest refractive index and packing density [31, 32]. X. Q. Wei et al. [30] compared quality of ZnO films annealed in vacuum, Nitrogen and Oxygen ambient and concluded that films annealed in Oxygen ambient shows good crystallinty.

1.2 Organization of the Report

The report is organized in to five chapters. Chapter 2 details about the working principle and physics involved in the operation of Tunnel FETs and JLTs. The results of device simulation and issuses related to fabricating vertical TFETs are discussed in Chapter 3. The ways to increasing the switching capability of JLT and a detailed process folw of ZnO based JLT are discussed in chapter 4. The conclusion and future scope of the work are listed in Chapter 5.

Chapter 2

Tunnel FETs and Junction less Transistors

In TFET gate controlled tunneling determines the device ON current. Since probability of tunneling depends on tunneling barrier height and width, these devices show temperature independent characteristics. Moreover, the band to band tunneling determines the device performance unlike MOSFETs where carrier mobility is dominant. This makes it possible to scale down channel length of TFET below 10 nm without decreasing performance. The basic operation of tunnel FET involves tunneling of charge carriers from valance band to conduction band. Since tunneling takes place in a small region, gate length of these devices can be scaled to the distance of tunneling barrier width which is less than 10 nm in Si. On the other hand, JLT has no source/drain junctions so device is free from punch through effect and allows to fabricate devices with smaller gate lengths. JLT eliminates the need for ultra fast annealing and reduces the thermal budget. Since there is no source, drain implants device is less sensitive to underlap and overlap gates.

2.1 Device structure and operation of TFET

The basic structure of TFET is a gated p^+-i-n^+ diode as shown in Fig 2.1, where gate is on an intrinsic channel region. p and n regions are heavily doped while the channel region is intrinsic. Here p-type region acts as a source of electrons in n-channel mode and n-type region acts as a source of holes in p-channel mode of operation of TFET. In both modes of operation, current is due to tunneling of electrons from valance band to conduction band. Gate controls the surface tunneling width and hence tunneling current. In the absence of gate bias reverse biased p-i-n leakage current (I_{bulk}) flows which is below the ITRS requirement for sub 100 nm technology

there by achieving less off currents. This current depends on device geometry (L, W) and doping profile in three regions. However, it is nearly independent of t_{ox} and gate bias V_{GS}. For low value of gate bias, band-to-band tunneling probability is low, I_{bulk} determines the standby leakage current (I_{OFF}) of TFET. since the p-i-n diode structure results in full thermal diffusion barrier for electrons and holes as compared to only half for the conventional MOSFETs, I_{OFF} is ideally low.

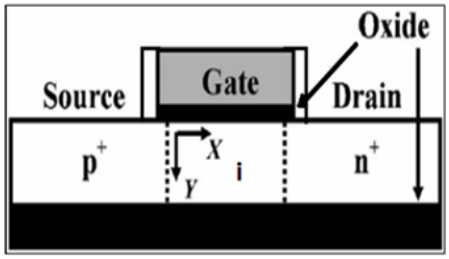

Figure 2.1: Schematic representation of a tunnel FET [2]

To operate p^+-i-n^+ diode in reverse bias, a positive voltage should be applied to n^+ Si region in Fig 2.1. Applying a positive voltage at the gate causes accumulation layer of electrons at Si-SiO_2 interface and thus acts like N channel FET. As shown in Fig. 2.2, applying positive voltage at gate causes the conduction band and valence band bend down ward in the channel region thus lowering the tunneling width near p^+ source and channel interface. This results in tunneling of electrons from valence band of p^+ source to conduction band of channel. Increases in gate voltage further pushes down the conduction band and valence bands in the channel region, tunneling width at source-channel interface further decreases and current increases exponentially. Similarly in p-channel operation, applying negative voltage at gate forms accumulation of holes and causes the conduction band and valence band bend up ward in the channel region, thus lowering the tunneling width near n^+ source and channel interface. So electrons tunneling from valence band of channel to conduction band of n^+ Si as shown in Fig 2.2.

Unlike conventional MOSFET, where the terms n-channel and p-channel refers the electron induced or hole induced current flow, for a TFET the terms are to distinguish whether the tunneling junction is created by electrons (n-channel) or by holes (p-channel) in the intrnsic channel region. The current flow in both n-channel and p-channel is due to electrons tunneling from valance band to conduction band. Thus with a mid band gap material, intrinsic

channel and symmetric drain and source doping profiles, the TFET on silicon has symmetric n-channel and p-channel current-voltage characteristics. This is an advantage over the MOSFET where current-voltage characteristics are not symmetric due to difference in electron and hole mobilities.So for a given technology node, channel width 'W' is different for n-MOSFET and p-MOSFET. But for TFET same channel width can be used. In a tunnel FET same device can be operated in either modes of operation by applying opposite polarity of gate voltage, which makes the device ambipolar. For a symmetric source and drain doping profiles,either n/p-channel TFET is ON, while other is OFF. This results in large leakage currents if the device is in off state. So it is common practice to use heavily doped source and lightly doped drain to decrease ambipolar leakage.

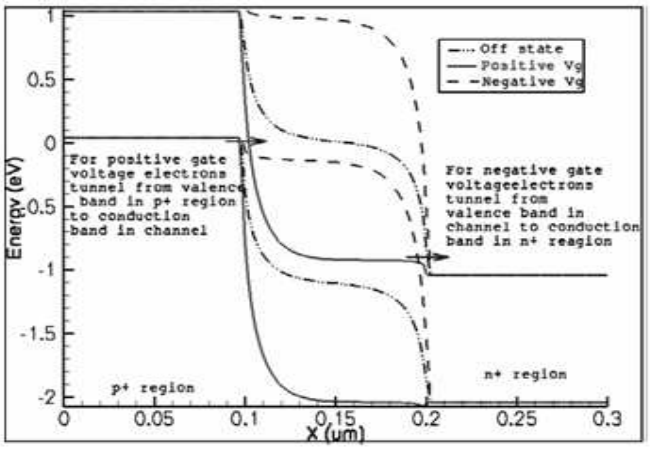

Figure 2.2: Band diagram for zero, positive and negative gate voltages [3]

2.1.1 Transfer characteristics and electrical parameters

TFET has different current-voltage characteristics than that of MOSFET. In a conventional MOSFET, diffusion current is dominant in the subthreshold regime where as drift current is dominant in the ON condition. However in TFETs, tunneling current is dominant. The transfer characteristics of a n-channel TFET is shown in Fig 1.3. Drain current consist of two components.

$$I = I_{pin} + I_{B2B}$$

At very low value of gate voltage i.e. in the flat portion of the transfer characteristics, p-i-n diode leakage current (I_{pin}) dominates the Band-to-Band tunneling current.At relatively higher gate

voltages, band to band tunneling current (I_{B2B}) dominates and it increases exponentially with applied gate voltage. Since TFET has different current mechanism as compared to MOSFET, the electrical parameters like V_t and SS are redefined. Threshold voltage based on the constant current method is defined as the gate voltage required to attain fixed drain current of 10^{-7}A. Since energy barrier narrowing is function of gate and drain voltages, gate threshold voltage and drain threshold voltages were defined [9]. Gate (Drain) threshold voltage V_{tG} (V_{tD}) is defined as the gate(drain) voltage for which energy barrier narrowing starts to saturates with applied voltage. Sub-threshold Swing (S) is an important parameter which describes the I_{ON}/ I_{OFF} ratio. It is defined as the gate voltage required to change drain current by one decade. Smaller the S, better will be the device performance. From the Kanes model the value of S is given by

$$S_{TUNNEL} = \frac{dV_{GS}}{dlog(I_{DS})} \quad = ln10 \frac{V_{GS}^2}{2V_{GS} + B_{kane} W_g^{1.5}/D}$$

where W_g is the band gap and D is device geometry parameter. In the above equation, W_g is the only temperature dependent term which is weak function of temperature. So TFET can exhibits almost temperature independent subthreshold swing. Unlike MOSFET, in TFET 'S' is dependent on gate voltage, because there is large reduction in tunneling width at a lower gate voltages and the reduction of tunneling width gets smaller as gate voltage increases. So there are two definitions of subthreshold swing were defined for TFET[5]. The Point SS is defined as the minimum swing value at any point in transfer characteristics. For calculating average subthreshold swing, SS is calculated for every decade from I_{vt} to I_{OFF} and then taken the average.

2.2 Device structure and operation of JLT

The basic structure of JLT is a gated nano wire resistor. Fig 1.4 shows the structure of n-channel SOI-JLT. The channel is heavily doped si-nano wire so that device is capable of getting good ON currents. A n-channel JLT requires a high work function gate material such as platinum or p^+ polysilicon in order to deplete the entire channel in the OFF state. So when Zero bias is applied to gate, channel is depleted of carriers, resulting in no conduction between source and drain. By applying positive voltage at gate, the channel comes out of depletion and results in a conduction path between source and drain. As like conventional MOSFET V_t strongly depends

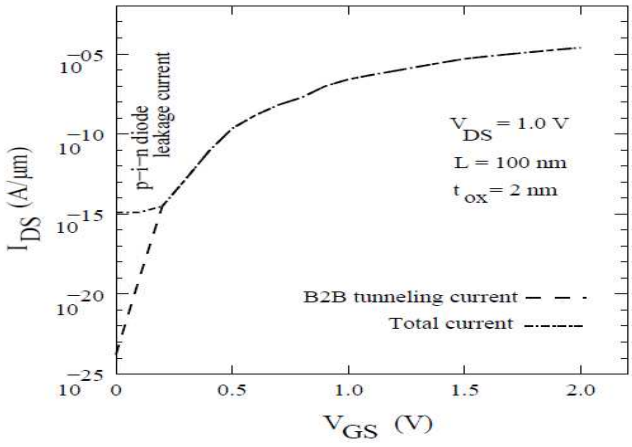

Figure 2.3: Transfer characteristics of n-channel TFT [3]

on channel doping and gate work function.

2.3 Summary

Working principle and physics involved in the operation of TFET and JLT was studied.

Chapter 3

Simulation and fabrication of vertical Tunnel FETs

3.1 Introduction

Tunnel FETs work based on the principle of Band-to-Band tunneling. The tunneling rate can be improved by using sharp doping profiles at source-channel interface. In the horizontal TFET shown in Fig 1.1(a), source and channel can be doped with the implantation where we cannot achieve abrupt doping profiles. But with the existing epitaxial growth of thin film techniques sharp doping profiles can be achieved in vertical direction, which calls for the study of vertical Tunnel FETs . In this chapter three types of vertical tunnel FETs were proposed and compared based on the simulation results. The Dynamic nonlocal tunneling model was used for the first time in Simulating Tunnel FETs. The solid phase epitaxial regrowth technique was discussed to fabricate vertival TFETs.

The Synopsis TCAD tool SENTAURES was used to carry the 2-D device simulations. The structure was drawn in the SENTAURES tool called Sentaurus Structure Editor (SDE). Constant doping profiles were used for source, channel and drain. The structure was simulated in SENTAURES tool called Sentures Device. The 'Non-local Tunneling model' is used which is more accurate than Kane's model used in [3]. The parameter pair m_t determines the tunneling masses m_c and m_v [17]. These values were calibrated to 0.65 [7]. SRH doping dependence recombination model was used. Besides doping dependence, E-normal mobility model and energy bandgap narrowing models were used. The circuit simulation of optimized vertical TFET was done in two steps. First extract the device parameters like terminal currents and

capacitances at all possible operating ranges and construct extensive data tables. These Look-up tables was implemented in Verilog-A language and subsequent circuit simulations was carried in a tool called CADANCE IC STUDIO.

3.2 Structure and working principle of vertical TFETs

The main test structures used for the simulation are shown in Fig 3.1. The working principle of all the structures is the same. Until and unless specified all the explanations given in this chapter with respect to structure 1 with channel thickness of 2 nm. same explanation can validates to others also. In all the structures underlying substrate acts as a source. So, a lowest resistivity sample is preferable to get more tunneling currents.The channel and drain can be grown epitaxially on the source. An oxide of 1.1 nm thickness can be thermally grown on the channel. A metal with a work function of 4.1 in case of n-channel TFET was defined on the oxide which acts as a gate. Here source is of p-type where as channel and drain are of n-type as like conventional TFETs. In this study source, channel and drain doping concentrations of 1E20,1E14 and 1E18 cm^{-3} were used. Structure 1 and 2 were simulated for channel thicknesses of 2 nm, 4 nm, 6 nm, 8 nm and 10 to optimize the device current. The structure 3 is more realistic where the deposited thickness on the flat surface (4 nm thick channel and 2.2 nm thick oxide) is twice that of on the slant surface (2 nm thick channel and 1.1 nm thick oxide).

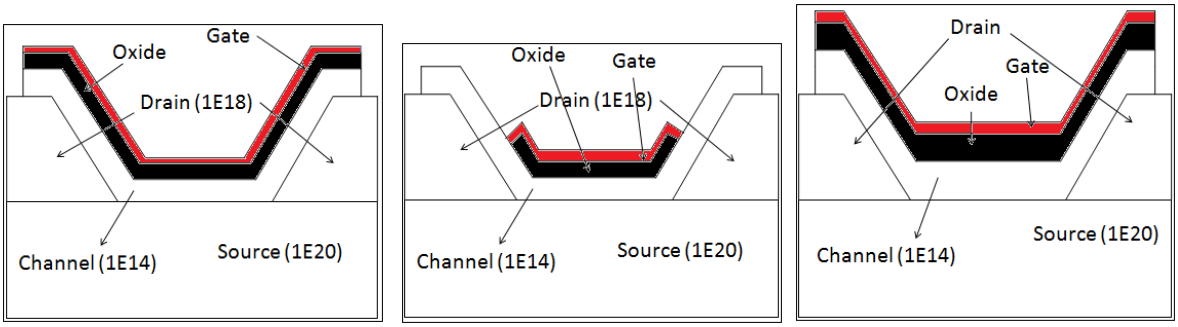

Figure 3.1: Device architecture of tunnel FET (a) structure 1 (b) structure 2 (c) structure 3.

The working principle of the device is same as the conventional horizontal TFET that is shown in Fig 2.1. The device can be operated in reverse bias by applying +1 volts to drain. Gate voltage is sweeping from 0 to 2 volts. Applying positive voltage at gate creates an accumulation of electrons which causes the conduction band and valence band bend down ward in the channel region thus lowering the tunneling width near p^+ source and channel interface. This results in

tunneling of electrons from valence band of p^+ source to conduction band of channel. The electrons that are tunneled in to the channel are collected by the drain. As the positive gate voltage increases tunneling width reduce further as shown in Fig 3.2 (a), as a result current increases exponentially. Tunneling width is also function of the drain voltage. Fig 3.2(b) shows the effect of drain voltage on tunneling width. Inset in Fig. 3.2(b) shows that as drain voltage increasing from 0 to 0.4 v, there is a large reduction of tunneling width, after that drain bias has no effect on tunneling width which shows clear saturation behavior.

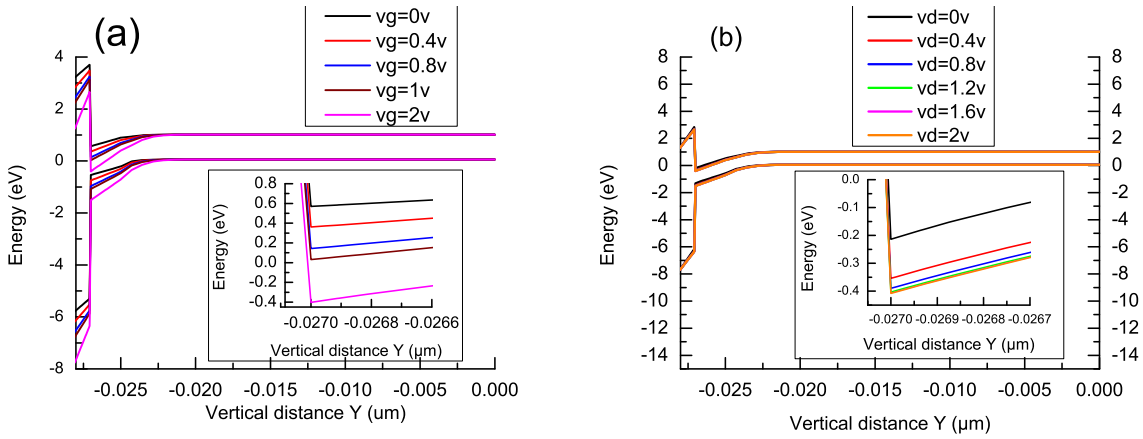

Figure 3.2: Tunneling width modulation with (a) Gate voltage and (b) Drain voltage.

3.3 Current-Voltage characteristics

The n-channel and p-channel TFET transfer characteristics are shown in Fig 3.3. Here work function of the gate metal is 4.1 eV and 5.2 eV for n-channel and p-channel respectively. In n-channel TFET, the ON current I_{ON} at V_{DS}=1 V and V_{GS}=2 V for 2 nm channel thickness is of 20 μA/μm. This is very much less than the technology requirement. The leakage current I_{OFF} is the p-i-n diode leakage current value of 0.02 fA/μm at V_{GS}=0 v. The threshold voltage V_t observed at I_{DS}= 0.1 μA/μm is nearly 1.15 v. The gate voltage V_{OFF}, at which Band-to-Band tunneling starts to dominate is 0.45v. Up to 0.45 v, I_{DS} is at a value of I_{OFF}, after that drain current start to increase exponentially because of continuous reduction in tunneling width.

The output characteristics of n-channel TFET for different gate voltages is shown in Fig 3.4. For V_{GS}=0 v, reverse bias p-i-n diode leakage current flows which is in the order of few fA. For $V_{GS} > 0$ V, as drain voltage increases, current increases in an exponential manner up to particular voltage called saturation voltage and after that current saturates. This is because at

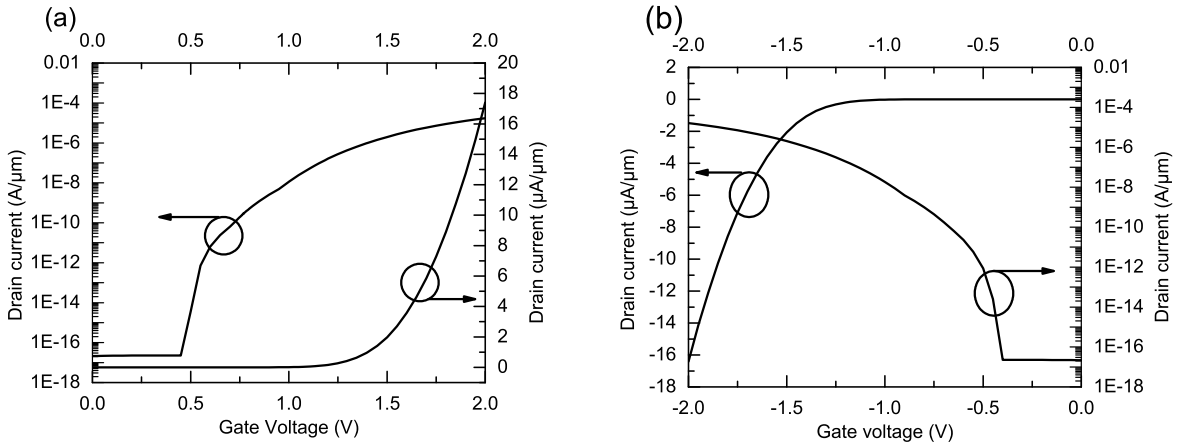

Figure 3.3: Transfer characteristics of (a) n-channel TFET and (b) p-channel TFET.

low drain voltages, as drain voltage increases tunneling width decreases and current increases exponentially, once it reached saturation voltage influence of drain voltage on tunneling width get reduced, so drain current slowly saturates. Fig 3.5(a) shows Energy band diagram in vertical direction for different drain voltages at a gate voltage of 1.6 V. The tunneling width abruptly decreases up to saturation voltage of 0.1 V, after that drain voltage has almost no effect on tunneling width. Moreover, this saturation voltage increases with increases in gate voltage. Fig 3.5(b) shows that for gate voltage of 2 V, saturation voltage increases to 0.15 V from its value of 0.1 V at gate voltage of 1.6 V. The proposed structure shows good saturation behavior so, an inverter designed with this structure can have sharp Voltage transfer characteristics.

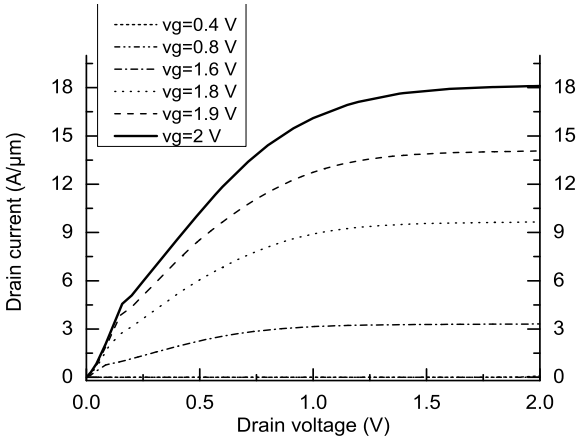

Figure 3.4: Output characteristics of n-channel TFET for different gate voltages

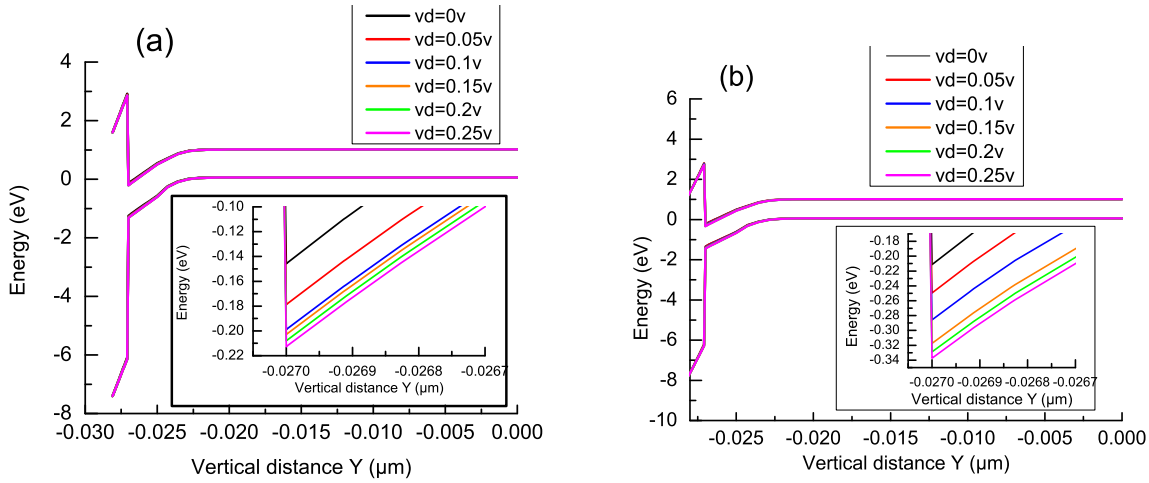

Figure 3.5: Saturation of reduction in tunneling width (a) for V_{GS}=1.6 V and (b) V_{GS}=2 V.

3.3.1 Dependence of drain current on channel thickness

Drain current is aggressively dependent on channel thickness. Fig 3.6 shows the n-channel transfer characteristics for the structure 1 with the channel thicknesses of 2 nm, 4 nm, 6 nm, 8 nm and 10 nm. As expected V_{OFF} get shifted to right and I_{ON} decreases with increase in channel thickness. From the Fig 3.6, it can be observed that device with channel thickness of 2 nm follows a different trend that of others. In 2 nm case there is an inflection point around gate voltage of 1 v. The reason to this can be explained with the barrier tunneling contour plots. Fig 3.7 shows the e-barrier and h-barrier tunneling contour plots for gate voltages of 0.4 v, 0.6 V, 0.8 V and 1 V. At a gate voltage of 0.4 V, there is no tunneling so drain current is at p-i-n diode leakage current. While gate voltage changing from 0.4 V to 0.6 V, tunneling happens at the slant portion of the channel region because at these less gate voltages electric field at the corner is more enough to create tunneling. So drain current start to increases from the gate voltage of 0.45 V. Moreover, at these less gate voltages electric field is not enough high for the tunneling to happen in a flat portion of the channel above the source. From the h-barrier tunneling contour plot of Fig 3.7(b), it can be observed that tunneling start to happen in the flat portion of the channel region at a gate voltage of 1 V. Therefore drain current again start to increase with the increased slope results in an inflection point at V_{GS} = 1 V. The same can be explained with the help of Fig 3.8, which shows the transfer characteristics of the device with channel thickness of 2 nm, having oxide thickness of 1.1 nm in the slant portion of region, 2.2 nm in the flat portion of region and its corresponding e-barrier tunneling contour plots for different gate voltages. Here there is no inflection point in the transfer characteristics because tunneling in the flat portion

of the channel region not starts at all even at V_{GS} = 2 V. So, unlike previous case tunneling increase monotonically without any inflection. In the transfer characteristics of Fig 3.8(a), it can be noticed that V_{OFF} increases to 0.55 V because increase the oxide thickness over flat channel region may slightly change the electro statistics in the slant portion of region.

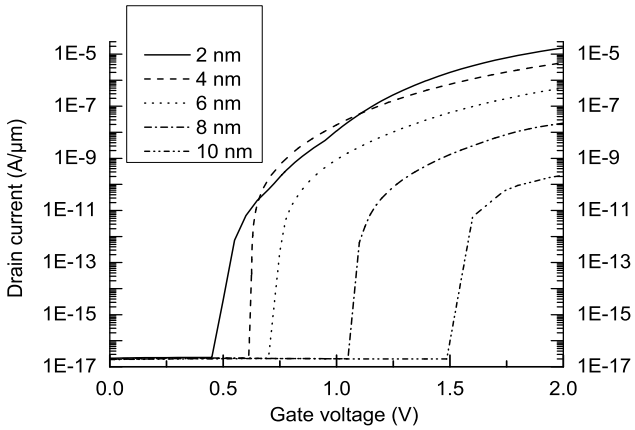

Figure 3.6: Transfer characteristics of n-channel TFET with channel thickness of 2 nm, 4 nm, 6 nm, 8 nm and 10 nm.

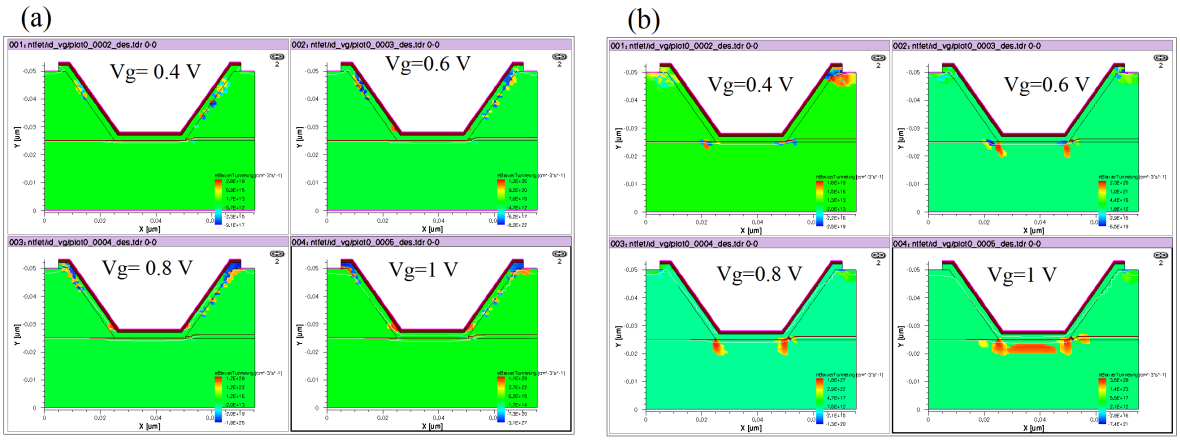

Figure 3.7: (a) e-barrier tunneling and (b) h-barrier tunneling contour plots of the structure 1 with channel thickness 2 nm for gate voltages of 0.4 v, 0.6 V, 0.8 V and 1 V.

However, device with channel thickness of 4 nm, 6 nm, 8 nm and 10 nm follow the same trend in which current monotonically increases without any inflection point. Fig 3.9 shows the e-barrier tunneling contour plots of the device with channel thickness of 4 nm for different gate voltages. Increasing Gate voltage up to 0.6 V does not cause any tunneling, so drain current is dominated by p-i-n diode leakage current. Increasing voltage from 0.6 V to 0.8 V, causes tunneling to happen in the both slant portion and flat portion of regions at the same voltage i.e

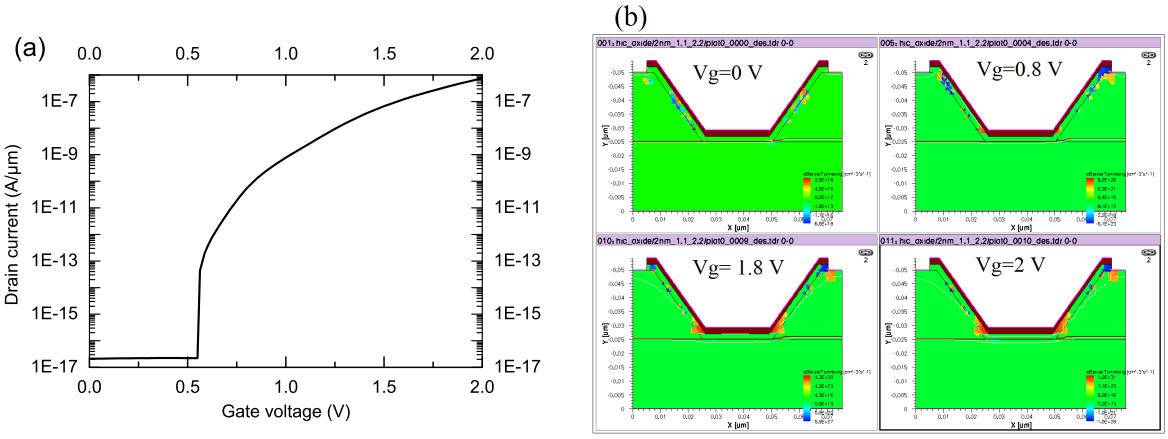

Figure 3.8: (a) Transfer characteristics and (b) e-barrier tunneling contour plot of the structure 1 with channel thickness 2 nm, having oxide thickness of 1.1 nm in the slant portion of region and 2.2 nm in the flat portion of region for V_g=0, 0.8, 1.8 and 2 V.

around 0.61 V. Unlike in 2 nm device, here electric fields in both regions are high enough for tunneling to start at the same voltage. Therefore current start to increase beyond 0.61 V without any inflection point. The same reason can also be validates to devices with channel thickness of 6 nm, 8 nm and 10 nm. Moreover from the Fig 3.6, it can be observed that for the gate voltages less than 1 V (approximately) current in 4 nm device is higher than that of 2 nm. Because at these gate voltages tunneling happens only in small (slant portion) region of channel in 2 nm device, but in 4 nm device it happens all over the channel. However, beyond 1V tunneling happens all over the channel in 2 nm device also, so drain current is more than that of 4 nm device due to high electric fields.

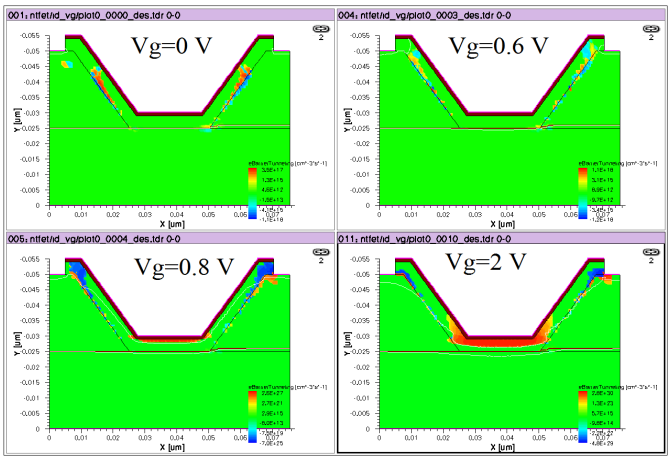

Figure 3.9: e-barrier tunneling contour plot of the structure 1 with channel thickness 4 nm for v_g=0, 0.6, 0.8 and 2 V.

Transfer characteristics of structure 2 with different channel thickness and structure 3 is

shown in Fig 3.10. The structure 2 with channel thickness of 2 nm and structure 3 have an inflection point in their transfer characteristics, this is because of the same reason explained in the case of structure 1 with channel thickness of 2 nm. Output characteristics of all the devices follow the same trend as shown in Fig 3.4. So far operation and behavior of n-channel TFET were discussed, same behavior can be seen in p-channel TFET also.

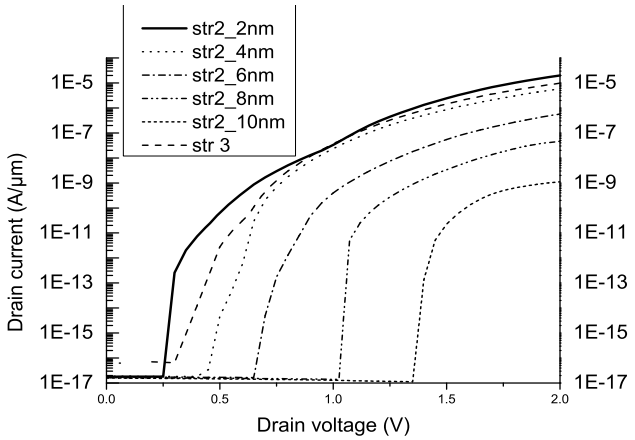

Figure 3.10: Transfer characteristics of structure 2 with different channel thickness and structure 3.

3.4 Device optimization

In the previous subsection working principle of different device structures have been studied. Among all the structures the better device has to optimized based on the I_{ON} and electrical parameters like V_t and SS. Optimization may also be carried out in terms of circuit level performance, but scope of this report limited to the optimization based on device level performance only.Among all these structures, structure 1 and structure 2 with channel thickness of 6 nm, 8 nm and 10 nm are not of interest because of their worse ON currents in spite of their better subthreshold swing. Remaining five devices : structure 1, structure 2 with channel thicknesses of 2 nm, 4 nm and structure 3 denoted as st1_2nm, st1_4nm, st2_2nm, st2_4nm and st3 are of interest to optimize in terms of I_{ON} and subthreshold swing. The threshold voltage is defined at a drain current of 1 X 10^{-7} A/μm. For calculating average subthreshold swing, SS is calculated for every decade from 1 X 10^{-7} A/μm to 1 X 10^{-17} A/μm and then taken the average. Fig 3.11 compares the five structures with respect to I_{ON} and subthreshold swing. Though the device st2_2nm gives better ON current, it has worse subthreshold swing. But with the device st1_4nm

Subthreshold swing can be reduced by approximately 30 mV, without degrading I_{ON} by not more than one order of magnitude. Therefore the device st1_4nm works well in terms of both I_{ON} and subthreshold swing, also its transfer characteristics did not have any inflection point as shown in Fig 3.6.

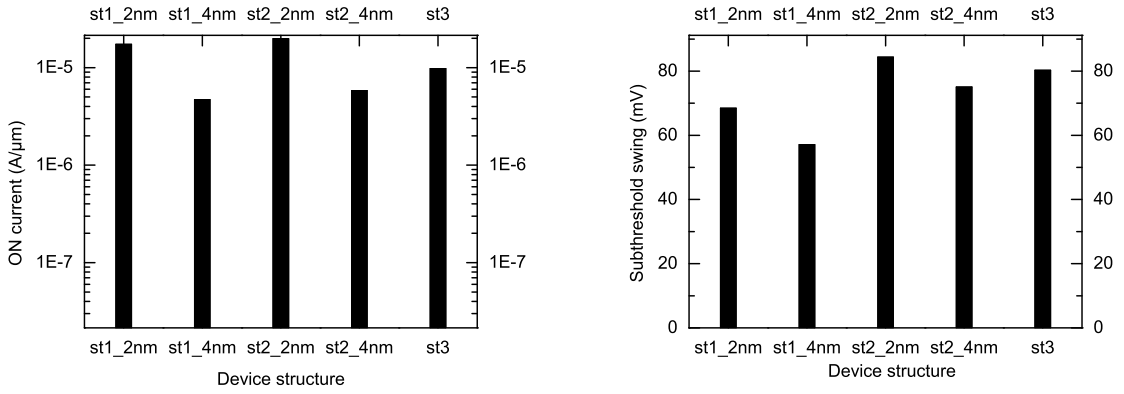

Figure 3.11: Effect of device architecture on (a) ON current and (b) Average subthreshold swing.

3.5 Circuit simulation

Circuit simulation plays an important role in design of digital as well as analog circuits. Device level optimization validates only if the circuit performance improves as the result of optimization. Though the device optimization gives good performance at the device level it is not guarantee that it gives good performance at circuit level also. The circuit level performance of structure 3 was estimated using Look-up table method.

Using the LUT based modeling of circuit simulation, symbols of n-TFET and p-TFET of structure 3 was created. Using the symbols of nTFET and pTFET an Inverter was designed. The voltage transfer characteristics (VTC) of inverter is shown in Fig 3.12. This smooth characteristics has rail-to rail swing and convincing that TFET structure works well at circuit level also. The Inverter threshold V_M is 0.52 V, which is slightly deviated to right from its theoretical value (0.5 V) because pTFET offers slightly higher current than the nTFET. The values of V_{IH} and V_{IL} calculated from that noise margin of an inverter is obtained as NM_H =0.38 V and NM_L=0.45 V. Fig 3.13(b) shows the transient response of a TFET inverter with a fanout of 1 (as shown in Fig 3.13 (a)) for a pulse input voltage of 1 V with 50 ns of rise and fall times. The pulse width was chosen to capture transient behavior of the inverter very well. The average de-

lay of an inverter is 174.5 ns and peak overshoot of 40.7 %. It is observed that TFET inverter has large overshoot due to its higher gate to drain miller capacitance. In a MOSFET Inverter, during normal operation when the transistor is ON, the gate capacitance (C_{gg}) is mainly contributed by gate to source capacitance (C_{GS}) where as in TETs the gate to drain capacitance (C_{gd}) reflects the entire gate capacitance and gate to source capacitance (C_{gs}) is very small. This is because in MOSFETs, band bending is high at the drain-channel junction, results in higher potential drop which in turn results in lower gate to drain capacitance (C_{GD}). Where as in TFETs, band bending is low at drain-channel junction results in lower potential drop which in turn results in higher C_{gd} and C_{gs} is very low due to presence of source side tunnel barrier[12].

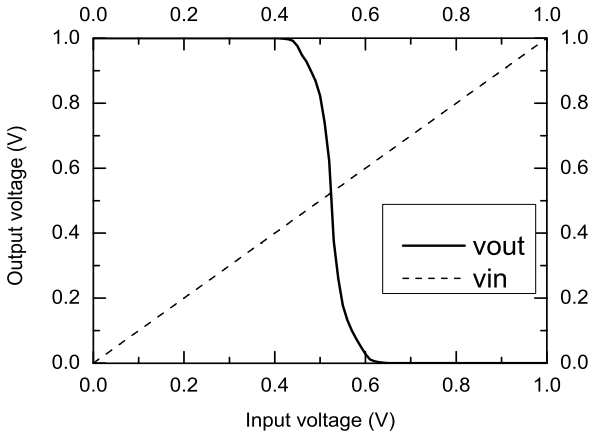

Figure 3.12: Voltage transfer characteristics (VTC) of a TFET inverter.

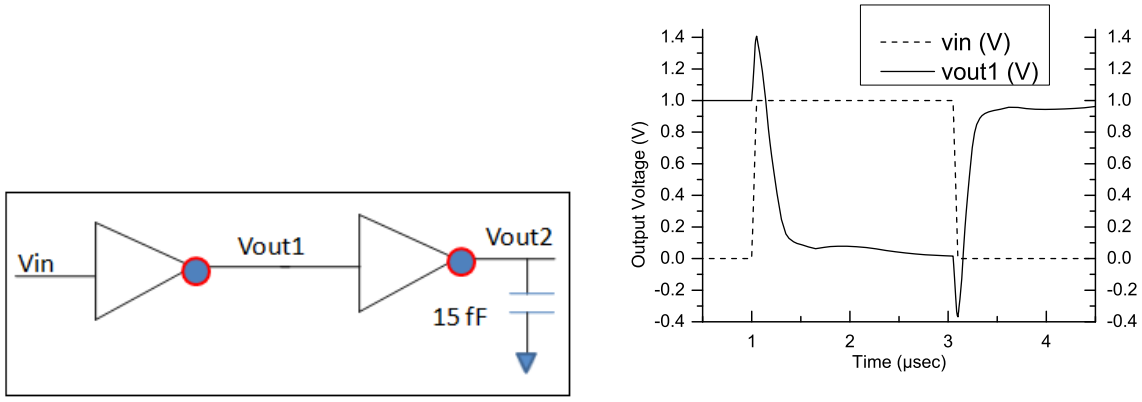

Figure 3.13: Transient response of a TFET inverter.

Ring oscillator circuits are commonly used as test circuits for comparing devices of different architectures and technologies. Stage delay and power dissipation are two main perfor-

mance criteria used for comparing various Device architectures. Here 15 stage ring oscillator using TFET was simulated for the following Power-Delay analysis. Fig3.14(a) shows the output of ring oscillator circuit for the representative case of V_{DD}=1 V. The time period of oscillations is 22.44 μs which translates to stage delay of 748 ns. Power-Delay analysis is carried out by plotting Average Power Vs Stage Delay of the ring oscillator circuit for different V_{DD}s. As the V_{DD} is increased the stage delay reduces where as the average power increases. A straight line with -ve slope in a log(power) vs log(Delay) plot in Fig 3.14(b) indicates an hyperbolic relation between power and the delay. Fig 3.14(b) also shows that peak overshoot decreased as the V_{DD} decreased. Similar analysis has to be done for remaining structures also so that circuit level performance of the device can be uniquely optimized.

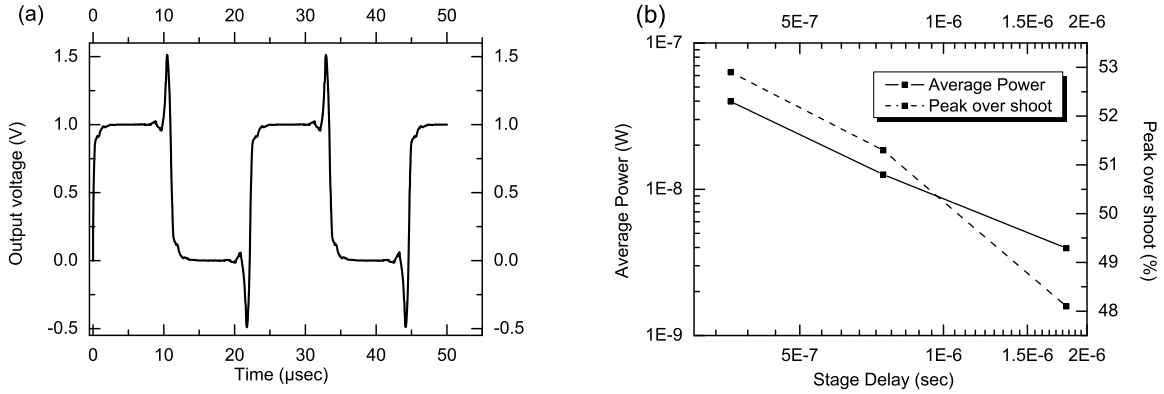

Figure 3.14: (a) Ouput voltage (b) Power-Delay analysis of 15 stage Ring oscillator.

3.6 Dynamic Non-local tunneling model

All the results discussed so far has done using Nonlocal barrier tunneling which involves charge-transport process at interface or contacts. It needs to define a special purpose nonlocal mesh for each part of the device where tunneling takes place. A nonlocal mesh consists of nonlocal lines, each of which connects the vertex of normal mesh to the interface for which nonlocal mesh is created by a shortest path. These nonlocal lines represents the tunneling path for the carriers i.e tunneling path does not depend upon actual band edge profile. Moreover in the device like TFET, tunneling current consist of point tunneling (occurs at source-channel interface) and line tunneling (occurs with in the source)[13]. Since nonlocal tunneling is an interface specific, it can captures the tunneling at source-channel interface, but does not capture the tunneling within

the source. Therefore an advanced tunneling model is needed in which tunneling path depends upon actual band edge profile. From 2009 version on wards Sentaurus device simulator offered a “Dynamic non local band-to-band tunneling model” which is a potential tunneling model for devices like TFETs.

Dynamic nonlocal band-to-band tunneling model implements both direct and phonon assisted tunneling processes[14] i.e it involves the nonlocal generation of electrons and holes in direct and indirect band gap semiconductors. Here the scope of discussion is limited to only phonon assisted tunneling process. Tunneling happens from valance band of one region to conduction band of other, and electrons and holes generated nonlocally at the ends of tunneling path. The good thing in this model is that the tunneling path is determined dynamically based on the potential profile rather than predefined nonlocal mesh as in the case of nonlocal tunneling model. So it does not require user defined nonlocal mesh. This model dynamically determines the tunneling path based on the following assumptions.

- The tunneling path is a straight line whose direction is opposite to the gradient of the valence band at the starting position.
- The tunneling energy at the starting position and at the ending position is equal to the valence band energy and conduction band energy plus band offset respectively.

For a given tunneling path that starts at x = 0 and ends at x = l, holes and electrons are generated at x = 0 and at x = l respectively. The net recombination rate is given as[14]

$$R_{net} = A(\frac{F}{F_o})^p exp(-\frac{B}{F})$$

where F0 = 1V/cm, F is constant force on electron taken to be in x-direction and p=2 for direct tunneling and p=2.5 for phonon assisted tunneling. For the phonon-assisted tunneling process, A and B are[17]

$$A = \frac{g(m_v m_c)^{5/2}(1+2N_{op})D_{op}^2(qF_o)^{5/2}}{2^{21/4}h^{5/2}m_r^{5/4}\rho\varepsilon_{op}[E_g(300K)+\Delta_c]^{7/4}}$$
$$B = \frac{2^{7/2}\pi m_r^{1/2}[E_g(300K)+\Delta_c]^{3/2}}{3qh}$$

where g is the degeneracy factor, Δ_c is the conduction band offset, D_{op}, ε_{op}, N_{op} are the potential, energy, and number of optical phonons, respectively.

The parameters of the dynamic nonlocal band-to-band tunneling model and their default values are listed in Table.1. The prefactor A and the exponential factor B are chosen as the input parameters. Here Δ_c, ε_{op} and m_v/m_c represents the conduction band offset, phonon energy and the effective mass ratio respectively. Specifying $\varepsilon_{op} > 0$ in parameter list, selects the phonon-assisted tunneling process, and parameters A, B, ε_{op}, m_v/m_c determine the tunneling masses m_v and m_c by the above equations where as in nonlocal tunneling model, tunneling masses m_v and m_c directly specified in parameter list. Apart from this, 'MaxTunnelLength' is another parameter in parameter file which specifies the maximum tunneling path, beyond which band-to-band tunneling can be neglected.

Table 3.1: Default parameters for Dynamic nonlocal path band-to-band tunneling model

Symbol	**Parameter name**	**Default value**	**Unit**
A	Apath1	4E14	$cm^{-3}s^{-1}$
B	Bpath1	1.9E7	Vcm^{-1}
Δ_c	Dpath1	0	eV
ε_{op}	Ppath1	0.037	eV
m_v/m_c	Rpath1	0	1

3.6.1 Calibration of Dynamic nonlocal tunneling model

The parameters of dynamic nonlocal band-to-band tunneling model A, B, ε_{op}, m_v/m_c are calibrated against the experimental data of tunnel diode reported in[15]. Here MaxTunnelLength set to 25 nm, the values of ε_{op}, m_v/m_c set to their default values. While varying the parameters A and B simulated ON state current is matched with the experimental data, but simulated OFF state current is many orders of magnitude less than the experimental data. Therefore carrier life time (τ_{max}) is varied to match the simulated OFF state current with the experimental result. Fig 3.17 shows fairly good agreement of the simulated characteristics with the experimental IV characteristics[15] for a reverse biased tunneling diode obtained with A=5.1E14, B=1.5E7 and τ_{max} = 1E-10. The values of A and B reported above are used throughout the work, but default value of τ_{max} (1E-5) is used instead of calibrated value of 1E-10. This is because to get best fit in Fig. 3.15 the less value of τ_{max} is used in calibration, but in practical device τ is much greater than calibrated value.

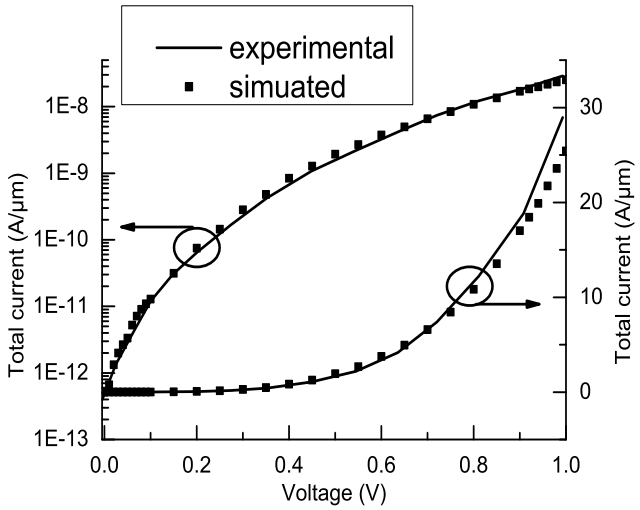

Figure 3.15: The simulated (solid line) and experimental (symbols)[15] characteristic of reverse biased silicon tunnel diode showing a fairly good agreement for the parameters discussed in the text.

3.6.2 Simulation result of TFET with Dynamic nonlocal BTBT model

The simulations was done with the TFET device proposed by Hasanali Virani[7] which is shown in Fig 3.16(a). Here source is of p-type with doping concentration 1E20 cm^{-3}, while drain and channel are of n-type with doping concentration are 1E18 cm^{-3} and 1E17 cm^{-3} respectively. An analytical Gaussian doping profile was used for source and drain where as channel is of constant doping profile. This TFET device was simulated using the dynamic nonlocal band-to-band tunneling model with its calibrated parameters. Fig 3.16(b) shows the comparison of transfer characteristics obtained with the nonlocal tunneling model and dynamic nonlocal band-to-band tunneling model. It can be observed that nonlocal tunneling model overestimates the current because it determine the tunneling path based on user-defined nonlocal mesh.

Moreover from the Fig 3.16(b), it can be observed that a nonlocal tunneling model gives better subthreshold swing than the dynamic nonlocal tunneling model. The reason for this can be explained by Fig 3.17, which shows the electron band-to-band tunneling contour plots of nonlocal and dynamic nonlocal band-to-band tunneling models at different gate voltages. In case of nonlocal tunneling model, at a gate voltage of zero volts there is no tunneling even though bands are aligned as shown in Fig 3.18. At a gate voltage of 0.2 V, electric field is large enough to create tunneling in the region where nonlocal mesh is created. So current abruptly increases at the voltage around 0.2 V. However unlike nonlocal tunneling model, dynamic non-

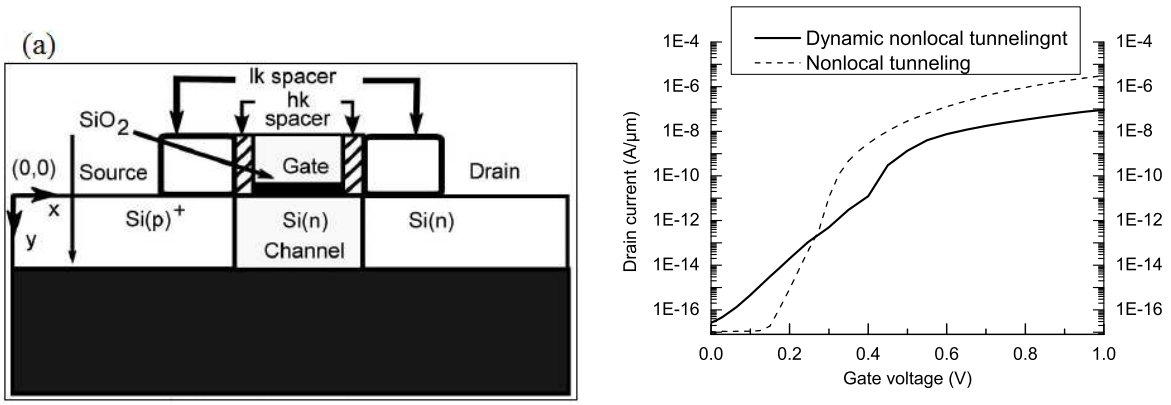

Figure 3.16: (a) Dual-κ spacer TFET structure[7] (b) Comparison of I-V characteristics of nonlocal and dynamic nonlocal band-to-band tunneling models.

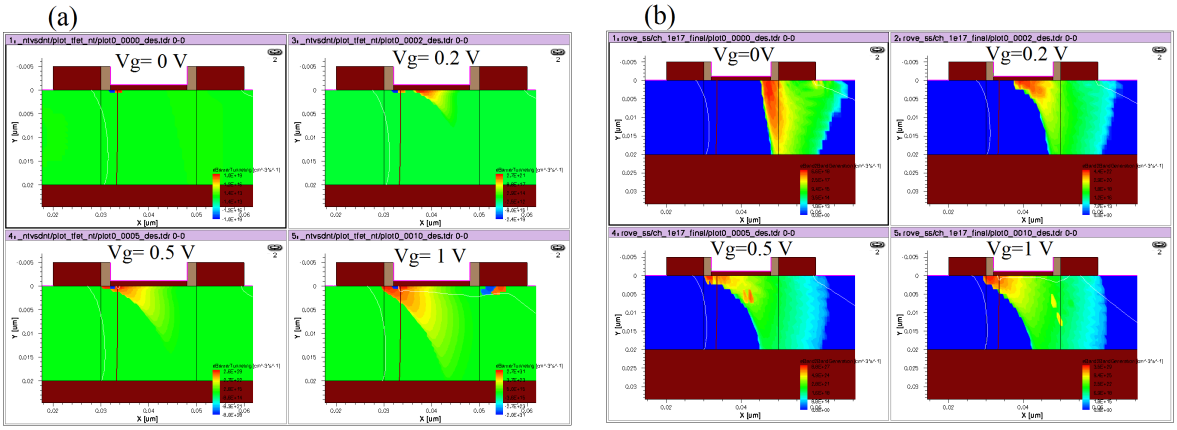

Figure 3.17: Band-to-band tunneling contour plots of (a) Non local tunneling model (b) Dynamic non local tunneling model at gate voltages of 0, 0.2, 0.5 and 1 V.

local band-to-band tunneling model is not an interface specific, and it involves the actual tunneling when band edges are aligned. Since bands at source and at drain end are aligned (as shown in Fig 3.18), tunneling can happen even at zero volts as shown in Fig 3.17(b), so off state current in dynamic nonlocal tunneling model is larger than its counter part. As gate voltage increases, the point along the channel where the band is aligned with that of source, moves from drain end at 0 V to source channel interface at 0.5 V as shown in Fig 3.17(b) and Fig 3.18. So current increases approximately in linear fashion up to 0.5 V as shown Fig 3.16(b), and once tunneling start to happen it increases exponentially. In summary Dynamic nonlocal band-to-band tunneling model is accurate than the nonlocal tunneling model. Though the dynamic nonlocal tunneling model is not quite impressive with the transfer characteristics due to degraded subthreshold swing, it is very accurately models the device like TFET and output characteristics with this tunneling model exhibits good saturation behavior as shown in Fig 3.19.

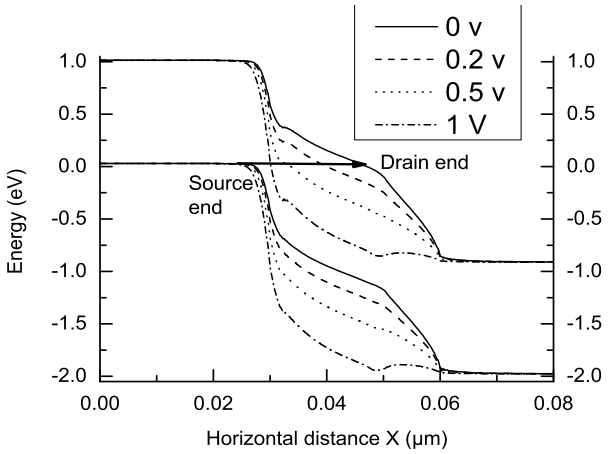

Figure 3.18: Energy band diagram along the channel just below the Si-SiO_2 interface for gate voltages of 0, 0. 2, 0.5, 1 V.

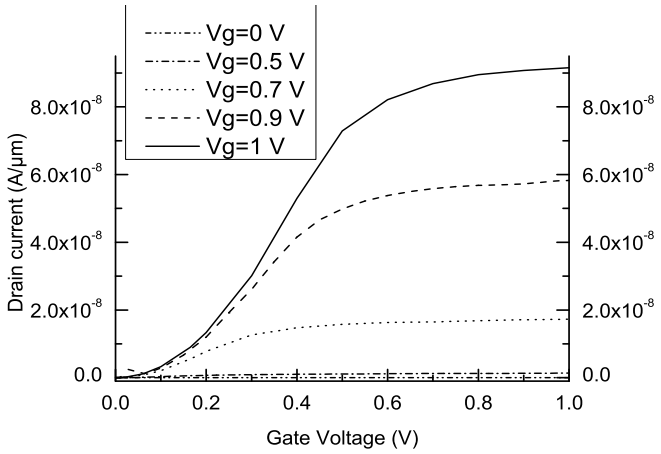

Figure 3.19: Output characteristics with dynamic nonlocal tunneling model for gate voltage of 0, 0.5, 0.7, 0.9, 1 V.

3.7 Solid phase Epitaxial Regrowth for Tunnel FET Fabrication

The vertical TFETs that has been introduced can be fabricated by an epitaxial growth.Usually CVD process involved in epitaxy requires High temperatures around 1000^{o}C. If the channel in vertical TFETs grown at this temperature, dopants can easily diffuse from underlying highly doped source to channel, and channel is no more an intrinsic region. Therefore a low temperature epitaxy have to be used so that dopants may not diffuse in to channel region, but at this temperature a perfect crystallization may not be achieved and grown layer is in amorphous form. A solid phase epitaxial regrowth technique has been attempted to crystallize the amor-

phous layer.

Solid phase Epitaxial Regrowth (SPE) is a two step process[16]. It is done by first depositing an amorphous film on the mono crystalline substrate by the CVD or other methods, which may be done at very low temperatures. Then in second step substrate is heated at ambient pressure to transform the amorphous film into a single crystal film. This process is typically performed on one side of the substrate at a time. Since deposition carried at low temperature fully crystallized structure may not achieve but a polycrystalline structure can be obtained, and some times it is sufficient to make a device. Three experiments have been done to grow an intrinsic layer on a heavily doped p-type substrate. Since a heavily doped source is required in vertical TFET, all the experiments have done on a lowest resistivity of 0.005 Ω Cm, p-type (1 0 0) oriented substrate. The process flow involved, RCA cleaning and silane deposition. The silane deposition step is different for three experiments. Table 3.2 describes all three experiments named as Experiment-1, Experiment-2, and Experiment-3 and their recipes. In all three experiments, silane deposition step has done at same conditions in an "Hot-Wire CVD Reactor". Experiment-1 involved pre and post annealing process and Experiment-2 involved only pre annealing where as Experiment-3 involved neither pre annealing nor post annealing. Pre annealing helps in removing any native oxide that is present on the substrate before silane deposition and post annealing helps in crystallizing the grown layer.

Table 3.2: Recipe used in three experiments ('-' indicates that particular process step has not done).

Name	**Pre annealing**	**Silicon deposition**	**Post annealing**
Experiment-1	At 800^{o}C, in H_2 gas for 10 min	At 250^{o}C, for 2 min	At 500^{o}C, in H_2 gas for 5 min
Experiment-2	At 800^{o}C, in H_2 gas for 10 min	At 250^{o}C, for 2 min	-
Experiment-3	-	At 250^{o}C, for 2 min	-

3.7.1 Results and Discussion

The Scanning electron microscopy (SEM) is a type of electron microscope technique, in which a high energy beam of electrons focused on the sample, and secondary electrons emitted from the target reveal the information about surface morphology, composition and crystallographic orientation. SEM images has taken for three samples in all the experiments, with that one can find uniformity and thickness of deposited film. Fig. 20 shows the SEM images of three sam-

ples. Due to lack of contrast difference between deposited a-Si and underlying c-Si, interface was not visible clearly. The thickness of deposited film is roughly estimated. Thickness of a-Si layer in Experiment-1 is about 250 nm, in Experiment-2 and in Experiment-3 thickness are about 130 nm and 100 nm respectively. In Experiment-3 deposited thickness is less compared to Experiment-1 because it does not involved pre annealing step and so native oxide presents on the surface decreases the growth rate. SEM results are not satisfactory, and cannot give any conclusion. So TEM imaging needs to be done to give conclusion about crystallization.

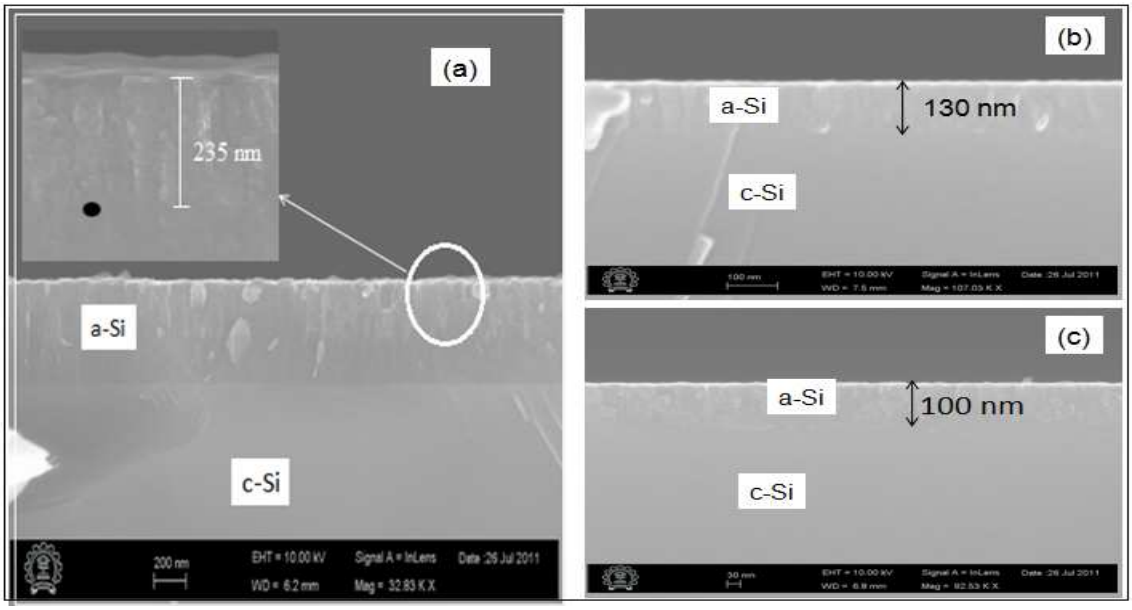

Figure 3.20: SEM images of sample in (a) Experiment-1 (b) Experiment-2 (c) Experiment-3.

The Transmission electron microscopy (TEM) is a power full technique in which a High voltage beam of electrons is transmitted through an ultra thin sample, there by forming an image by the interaction of electrons transmitted through the sample. To get TEM images, sample should be ultra thin to the transparency of electron. So TEM analysis involved Sample preparation in which thickness of sample get reduced to around 50 μm. TEM images has taken for the two samples in Experiment 1 and Experiment 3. While doing sample preparation, sample under goes many mechanical stress, and top surface may be etched. So in Experiment-1 a 150 nm thick Al metal was deposited. Since atomic weight of Al is not much differed from Si,There is a small contrast difference between the two as shown in Fig. 3.21(a). So in Experiment-3 a 140 nm thick Chrome gold was deposited, since there is a large atomic weight difference between Cr and Si, a large contrast difference between the two can be observed.

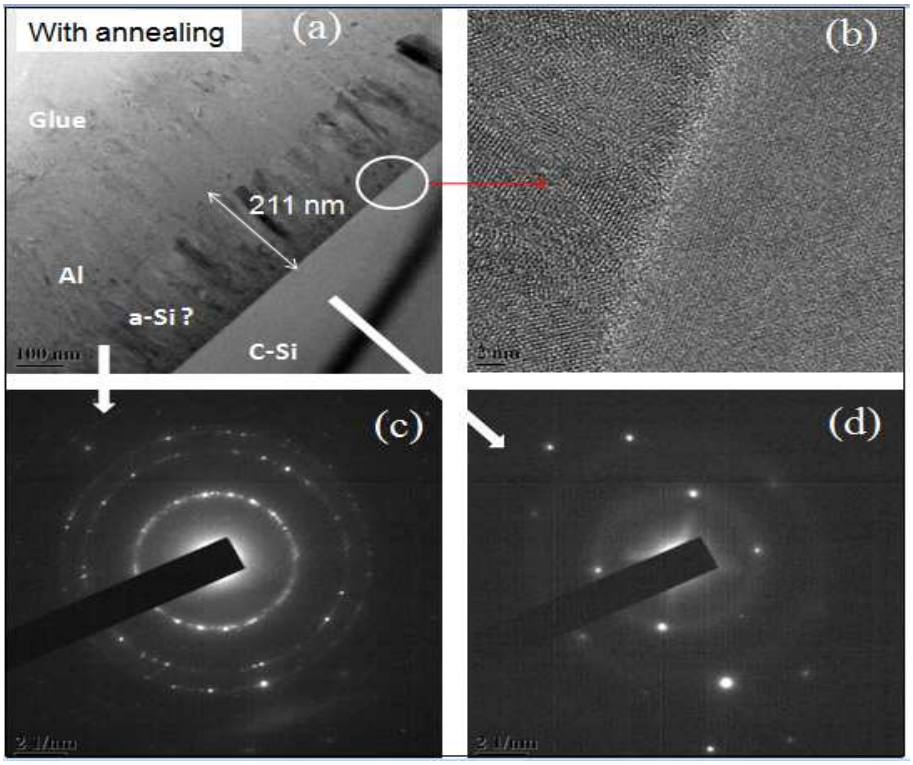

Figure 3.21: TEM images and diffraction pattern of sample in Experiment-1.

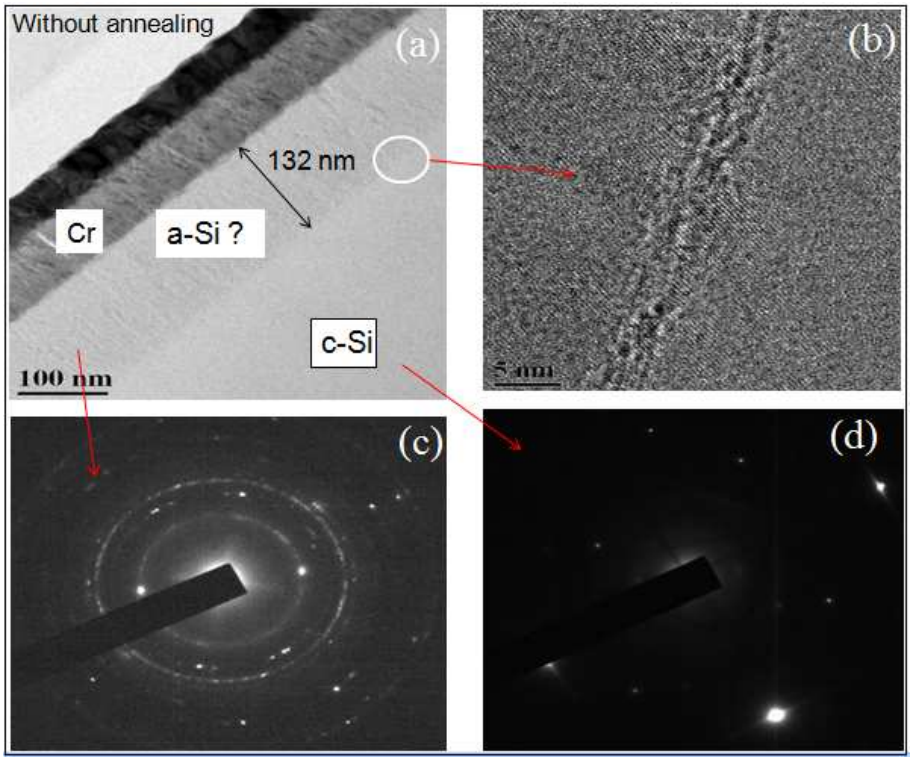

Figure 3.22: TEM images and diffraction pattern of sample in Experiment-3.

Fig. 3.21 shows different material deposited on the sample, interface layer of amorphous-crystalline Si and diffraction pattern in both a-Si and c-Si in Experiment-1. In the figure (b) lattice fringes can be observed in a-Si, which indicates that deposited layer is partially crystallized. The diffraction pattern in Fig (c) has rings which indicates deposited layer is of polycrystalline nature and it is no longer amorphous. Fig (d) shows the spotty diffraction pattern in crystalline silicon. Deposited layer thickness is around 211 nm, approximately matched with SEM result. Fig. 3.22 shows different material deposited on the sample, interface layer of amorphous-crystalline Si and diffraction pattern in both a-Si and c-Si in Experiment-3. Here also some lattice fringes can be observed in a-Si that indicates partial crystallite and diffraction pattern shows the rings that means as deposited silicon is not amorphous, it is polycrystalline because at the deposition temperature of 250 ^{o}C, some atoms are partially crystallized. In Experiment-1 a-Si layer has more lattice fringes and its diffraction pattern has less rings, which indicates that grown layer in experiment-1 is more crystallized because it involves annealing process. Though the grown layer in Experiment-1 is better crystallized, this is not sufficient to make device.

3.8 Summary

Three types of vertical TFET devices have been proposed and simulated. Structure of the device is optimized based on the I_{ON} and SS. Circuit simulation of the TFET inverter and ring oscillator have been done to validate the device operation at circuit level. The physics behind the Dynamic nonlocal band-to-band tunneling model was discussed. The parameters of the new model was calibrated with the experimental data. The calibrated model is used to simulate the Dual-κ spacer TFET. A Solid phase epitaxial regrowth technique have been used to optimize the depositing conditions of amorphous Silicon on heavily doped substrate. TEM results gave conclusion that as deposited sample is no longer amorphous, and pre annealing increased the growth rate while post annealing increased the amount of crystallization.

Chapter 4

ZnO based Junction less transistors

4.1 Introduction

ZnO is a transparent wide bandgap semiconductor (a band gap of approximately 3.37 eV at room temperature) with hexagonal wurtzite structure. The combined properties of transparency, low thermal budget processing and unintentional n-type conductivity make ZnO Thin film transistors suitable for low cost opto-electronic devices. Recently active matrix organic light-emitting diodes (AMOLED), LCDs were realized by using bottom gate ZnO thin film transistors[39, 40]. The fabricated ZnO TFT has on currents of 129 μA at a V_{GS}=40 V and V_{DS}=10 V[39]. The top gated enhancement mode ZnO TFT attained good on currents of 1 mA relatively at lower operating voltages[41].

The top gated transistors had large drive current because of enhanced gate coupling. The Junction less transistor (JLT) that do not have any junctions along the conducting path has full CMOS compatibility and is immune to short channel effects[18, **?**]. Moreover the ZnO TFT is suffering from short channel effects (e.g., channel length modulation, degrading subthreshold slope and lowering the V_t) when its channel length scaled down to less than 5 μm[42]. So there is a scope to make JLT with ZNO active channel layer.

The JLT is normally on device and a large work function gate material is needed to turn it off when the gate voltage is zero. Since the off state leakage currents depend upon the channel thickness, the channel thickness of a SOI-JLT should be scaled in proportion with its gate length in order to maintain good on to off current ratio[43]. But getting ultra thin channel layer is expensive and difficult. Moreover, one can get an advantage of enhanced crystallization and improved conductivity with thicker ZnO films[44, 45]. Bulk planar JLT that creates a junc-

tion isolation and reduces the effective channel thickness to half of its physical thickness, but requires highly doped substrates in excess of 5E18 cm^{-3} for ultra short channel device[24].

We propose a new device architecture that reduces effective channel thickness by growing a highly doped substrate layer on lightly doped substrate. The highly doped substrate layer can be easily grown by existing implantation or diffusion. The newly proposed device has an advantage of better scalability and good I_{ON}/I_{OFF} ratio in addition to full CMOS compatibility, low thermal budget processing and low cost of existing JLT devices. Highly doped substrate layer and substrate layer are used anonymously.

4.2 Simulation setup

The SOI-JLT and BPJLT were simulated using Sentaurus 2-D device simulator which solves the drift- diffusion equation for both electrons and holes. Since ZnO material is not available in the tool, Zno was defined as n-doped Silicon with carrier concentration of 1E19 cm^{-3}. The simulation of a JLT mostly depend upon the band gap models, mobility models and dielectric constant of a semiconductor. So only these model parameters of ZnO listed in Table 4.1 were used in place of Silicon parameters and rest of the models were used same as those of Silicon. The doping dependent mobility model of ZnO was calibrated against the experimental data [46] as shown in the inset of Fig 4.3. Constant doping profiles were used, bandgap narrowing models were switched on due to higher doping profiles used in the device architecture. SRH recombination model, Doping dependent and transverse field dependent mobility models were included. The models did not include any tunneling model.

Table 4.1: The model parameters of ZnO used in the device simulation.

Parameter	**Value**
Bandgap	3.37 eV
Dielectric constant	3
Electron effective mass	0.24
Electron affinity	4.28 eV
Hole effective mass	0.59
Bulk electron mobility	200

4.3 Device structure and operation

The buried oxide layer (BOX) thickness varies from few tens of nanometers to hundreds of nanometer in the conventional SOI-JLT . But the electrostatics of a device can be improved using thin BOX layer. Fig 4.1 shows effect of well bias and well doping on I_{ON} and I_{ON}/I_{OFF} ratio of ZnO based SOI-JLT with different BOX thickness of 50 nm and 10 nm. The influence of well bias and well doping is very low in case of SOI-JLT with box thickness of 50 nm. Whereas the SOI-JLT with box thickness of 10 nm is very sensitive to well bias and well doping due to improved electrostatics. By decreasing well bias or increasing well doping I_{ON}/I_{OFF} ratio can be improved by many orders of magnitude without degrading on currents by not more than one order of magnitude. So, the switching capability of SOI-JLT can be improved by using thin BOX layer until the field across the BOX reaches its break down level.

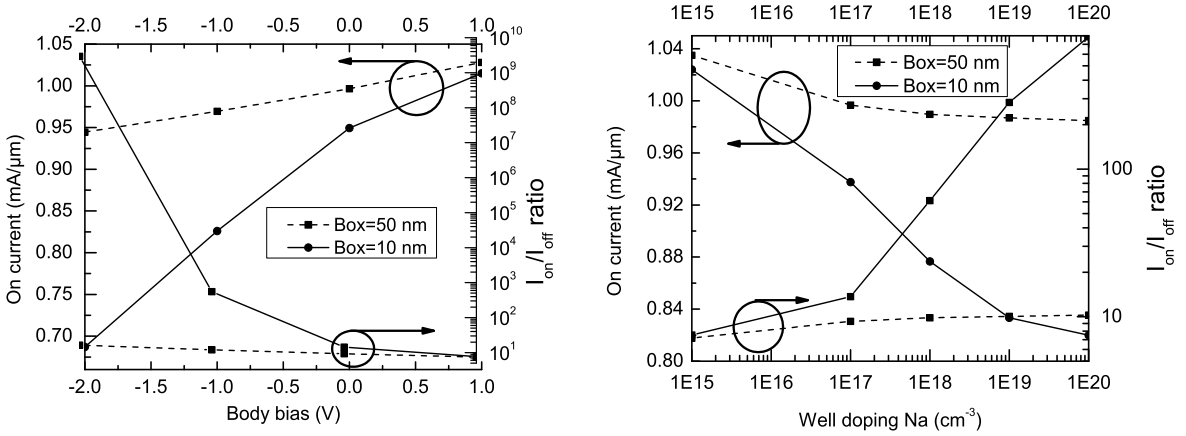

Figure 4.1: Influence of (a) body bias and (b) well doping on the I_{ON}, I_{ON}/I_{OFF} ratio of SOI-JLT with box thicknesses of 50 nm and 10 nm.

The switching capability of SOI-JLT can be improved with substrate doping, but getting substrate doping as high as 1E20 is very difficult. So we proposed a new architecture as shown in Fig 4.2(a) in which substrate layer is grown on lightly doped substrate. The substrate layer can be made by implantation or diffusion of boron and it resembles a V_t implant in normal CMOS process flow. Furthermore the thickness of substrate layer has no effect on the I-V characteristics as it is heavily doped. So, this process being not critical do not require any high temperature annealing and had an advantage of low thermal budget. The concept of substrate layer can be extended to BPJLT also as shown in Fig 4.2(b). Both the devices have identical doping profiles along the conducting path from source to drain. The p-type work function gate material is used in both the devices. In both devices, Silicon is used as a substarate material.

Table 4.2: The parameters of the device architectures used in the device simulation.

Parameter	Value
BOX thickness of SOI-JLT	10 nm
Doping of semiconductor body	1E19 cm^{-3}
Thickness of semiconductor body	10 nm
Thickness of substrate layer	20 nm
Doping of substrate layer	1E20 cm^{-3}
Gate work function	5.6 eV
EOT of gate dielectric	1.1 nm
Substrate doping	1E17 cm^{-3}
Gate length	20 nm

The device parameters used in the simulation are listed in Table 4.2.

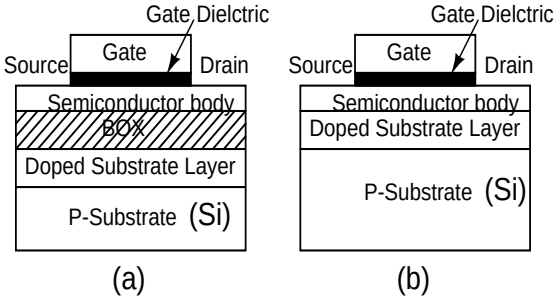

Figure 4.2: Schematic representation of (a) SOI-JLT and (b) BPJLT with substrate layer

4.4 Results and discussion

The newly proposed ZnO SOI-JLT was simulated with the models described in section II. In addition, the Si SOI-JLT was also simulated for comparison. In both cases the device parameters and materials are same except the channel layer. As shown in the Fig 4.3, the ZnO SOI-JLT (shown in blue) attained better subthreshold characteristics and lower V_t than Si SOI-JLT (shown in black). This is because of the reason that the dielectric constant of ZnO is 4 times lower than that of Si and so is the capacitance. The voltage applied at the gate is divided across the series combination of oxide capacitance (C_{ox}) and channel capacitance (C_{ZnO} in case of ZnO SOI-JLT, C_{Si} in case of Si SOI-JLT). Since both the devices have same EOT

of 1.1 nm, C_{ox} is same in both cases. But C_{ZnO} is four times smaller than C_{Si}. So, for the

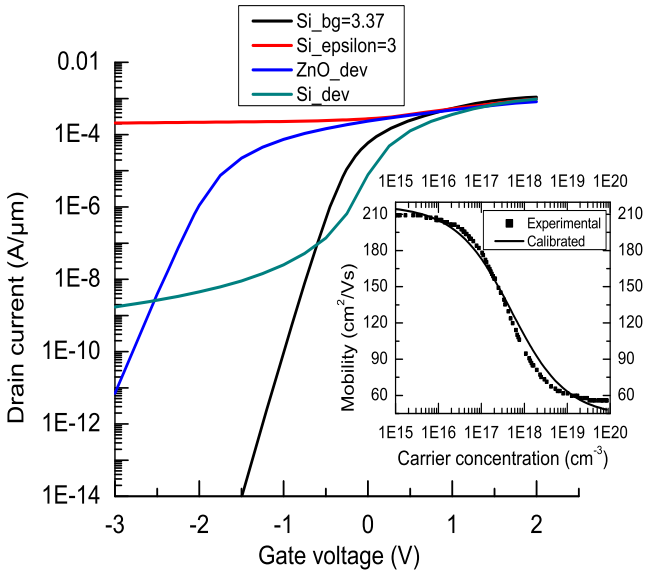

Figure 4.3: Comparison in I_d-V_g characteristics of ZnO SOI-JLT and Si SOI-JLT with substrate layer with the parameters listed in Table 4.2. The inset shows the calibration of doping dependent mobility of ZnO against experimental data [46].

same incremental gate voltage, the fraction of gate voltage appeared across the channel layer is larger in ZnO SOI-JLT than in Si SOI-JLT. So ZnO SOI-JLT requires less gate voltage to come out of depletion and attains less V_t than Si SOI-JLT. The improved subthreshold characteristics of ZnO SOI-JLT is due to its high bandgap than Si. To prove these concepts, we simulated Si SOI-JLT by changing only the band gap of Si from 1.1 to 3.37 (band gap of ZnO) and observed better subthreshold characteristics but V_t same as that of normal Si SOI-JLT as shown (red) in FIg 4.3. Similarly we simulated Si SOI JLT by changing only the dielectric constant of Si from 11.7 to 3 (dielectric constant of ZnO) and observed lower V_t as shown (pink) in Fig 4.3.

As discussed earlier thin BOX layer improved the switching capability of a conventional SOI-JLT. By using high-κ dielectric material instead of BOX, enhancement of switching capability can be further improved due to substrate layer. Fig 4.4 shows the effect of dielectric constant of BOX (with same physical thickness of 10 nm) on I_{ON} and on-to-off current ratio. By using high-κ dielectric material like HfO_2 instead of SiO_2 for BOX, on-to-off current ratio was improved by eight orders of magnitude, without degrading I_{ON} by not more than 50%. But effective BOX thickness being 1.1 nm (for physical thickness of 10 nm HfO_2) can not withstand to high electric fields in ultra short channel regime. So we used dielectric constant of 9 with

effective BOX thickness of 4.5 nm which can be obtained.

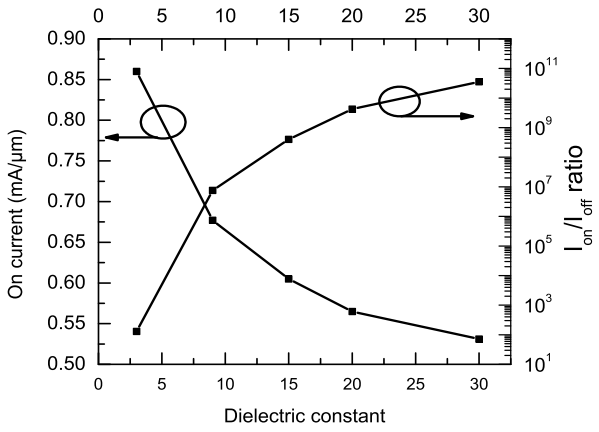

Figure 4.4: Effect of dielectric constant of BOX in SOI-JLT (with the parameters listed in Table 4.2) on I_{ON} and I_{ON}/I_{OFF} ratio.

The concept of using substrate layer was extended to BPJLT also. Since BPJLT creates a junction isolation instead of dielectric isolation [24], the effect of substrate layer is more in BPJLT than in SOI-JLT. Fig 4.5 shows the I-V characteristics of both SOI-JLT and BPJLT with and without substrate layer. In both SOI-JLT and BPJLT with substrate layer off state currents are very low. This is because of depletion of bottom part of the channel due to substrate layer, there by reducing the effective channel thickness as shown in the inset of Fig 4.6. The substrate layer further reduced the effective channel thickness in BPJLT than in SOI-JLT. So BPJLT offer very low off currents than SOI-JLT. Furthermore the I_{ON}/I_{OFF} ratio of a BPJLT with substrate layer can be tuned in the range of many orders of magnitude by varying the well bias and substrate layer doping simultaneously.

Fig 4.6 shows the I_d-V_d characteristics of both SOI-JLT and BPJLT with and without substrate layer at a gate voltage of 1 V. Both SOI-JLT and BPJLT with substrate layer exhibits hard saturation at less drain voltages. This is because of reduced effective channel thickness by almost half (as shown in inset of Fig 4.6) requiring less drain voltage to pinch-off the entire channel than the devices without substrate layer. Thus the substrate layer helped in attaining high output impedance which is desired for most circuit applications. This effect is more pronounced in BPJLT because of reduced effective channel thickness than its SOI counter part.

Fig 4.7 shows the I_d-V_g characteristics of BPJLT with and without doped substrate layer at different gate lengths and drain voltages. When the channel length of a BPJLT without substrate layer scaled from 1 μm to 20 nm, lowering in V_t due to charge sharing, degradation of

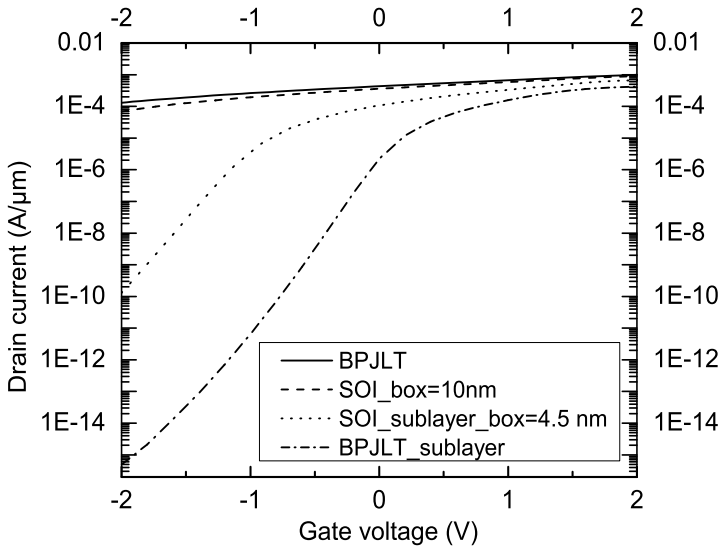

Figure 4.5: Comparison in I_d-V_g characteristics of SOI-JLT and BPJLT with and without substrate layer with the parameters listed in Table 4.2.

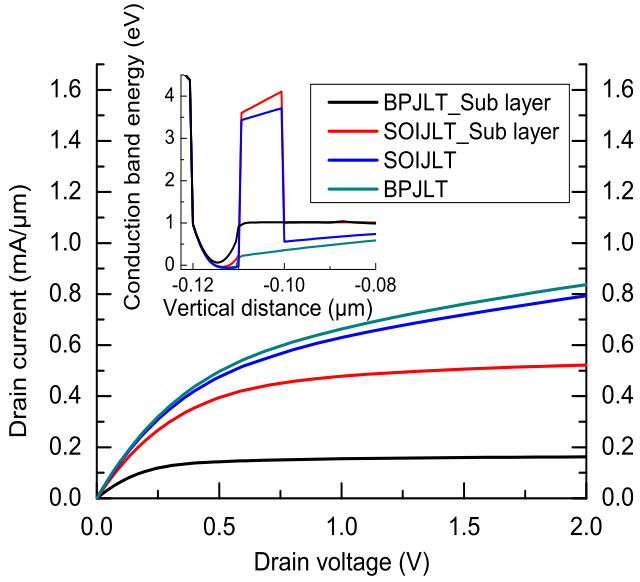

Figure 4.6: Comparison in I_d-V_d characteristics of SOI-JLT and BPJLT with and without doped substrate layer at V_g=1 V with the parameters listed in Table 4.2, The inset shows conduction band energy in vertical direction of the devices taken at the middle of the channel.

subthreshold slope were observed. Also when the drain voltage of a BPJLT without substrate layer is increased from 0.1 V to 1 V, lowering in V_t due to DIBL and degradation of subthreshold slope were observed. However, in case of the BPJLT that are made on substrate layer, the V_t and subthreshold slope relatively insensitive to variation in drain voltage and gate length. Moreover

the ZnO TFT is suffering from channel length modulation when its channel length scaled down to less than 5 μm [42]. But here, both SOI-JLT and BPJLT with substrate layer are free from channel length modulation (as shown in Fig. 6) even at a gate length of 20 nm. So ZNO JLT made on substrate layer has better scalability compared to conventional JLT.

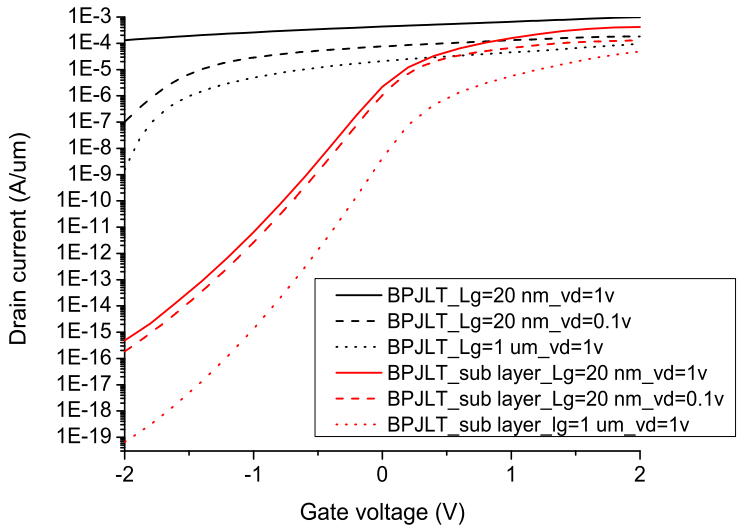

Figure 4.7: Comparison in I_d-V_g characteristics of BPJLT with and without doped substrate layer at different gate lengths and drain voltages with the parameters listed in Table 4.2.

4.5 Process flow Of ZnO based JLT

The detailed process flow of ZnO based JLT is shown in Fig 4.8 and it requires 3 levels of mask alignment. A p-type $\langle$ 100 $\rangle$ oriented, 0.005 Ω Cm Si wafer has chosen as substrate material. An highly doped Si substrate can prefer to achieve double gate control. The standard RCA clean is used to remove any organic and metal impurities. A 50 nm thick buried oxide has grown in the furnace by dry oxidation as shown in Fig (b). The back side oxide etch was done using 5% buffered oxide etch solution (BOE) by protecting front surface with photoresist. The ZnO films was grown by rf sputtering as shown in Fig (c). Then active area was defined by first level lithography using active area mask (mask 1). The NH_4Cl solution is used to etch unprotected ZnO films. In Fig (d), each ZnO thin film act as channel of junction less transistor. Then next step is to grow gate dielectric and gate material. Here a 10 nm thick Al_2O_3 deposited by sputtering is used as gate dielectric and 100 nm thick Al deposited by evaporation is used as

gate material as shown in Fig (e). The gate and gate dielectric can be patterned by second level lithography using gate area mask (mask 2) followed by etching of unprotected Al and Al_2O_3 Using reactive ion etching (RIE) as shown in Fig (f). Finally contacts were made by lift-off process using the probe area mask (mask 3) as shown in Fig (g).

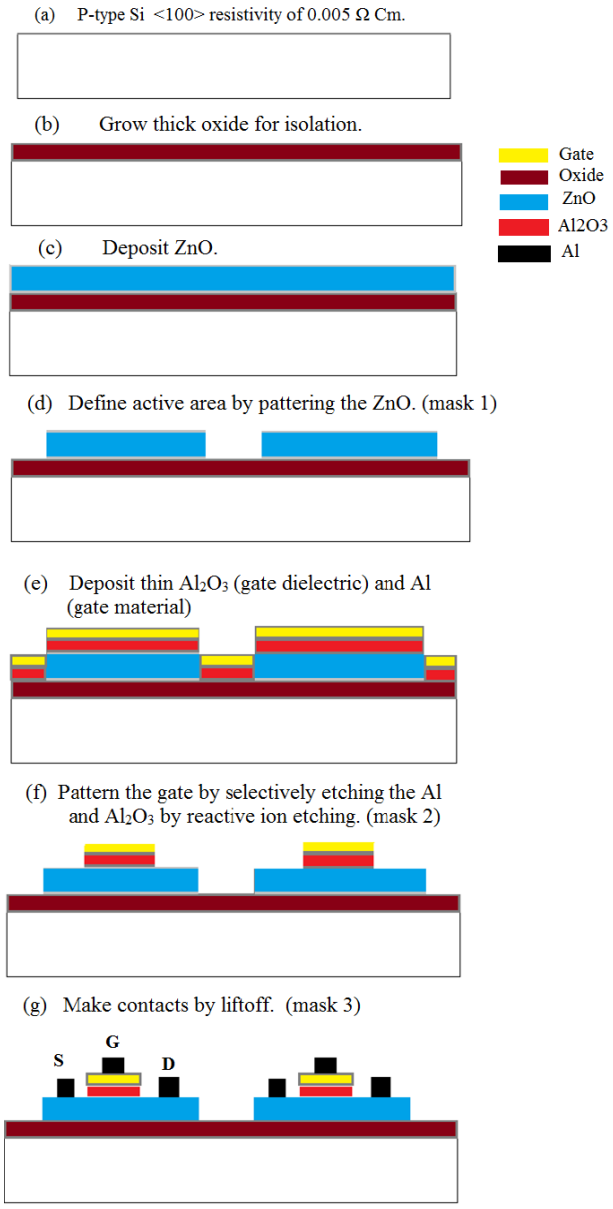

Figure 4.8: Process flow Of ZnO based JLT.

4.5.1 ZnO deposition

The ZnO films was grown by rf sputtering using pure ZnO powder as the target. The size of ZnO target is 5“ and distance between target and substrate is 75 mm. Deposition was done

at room temperature with Argon as the process gas. Since the film quality depends upon the deposition conditions an attempt was made to optimize the deposition conditions. The increase in rf power enhances the film crystallinity and carrier concentration by reducing resistivity [28], so here deposition was done at maximum rf power of 100 W.

Argon pressure strongly effects the film quality. To study the effect of process pressure on film quality, ZnO was deposited on five silicon samples denoted as S1, S2, S3, S4 and S5 at five different pressures of 5E-3, 8E-3, 1E-2, 2E-2 and 3E-2 mbars. For all the samples ZnO was deposited for constant time of 20 min at a constant sputtering power of 100 w. As shown in Fig 4.9 (a) the thickness of the film increased initially and then decreasing with the Ar pressure. This is because in the low pressure regime, the bombardment of high energy particles to film surface is reduced as pressure increases [26]. When the pressure reaches to 8E-3 mbar, thickness reached to maximum. Thereafter, thickness was decreased as pressure increased. This is because as deposition pressure increased, sputtering particles under go many collisions with the gas molecules and mean free path of sputtered species was reduced and resulted in reduction of sputter yield.

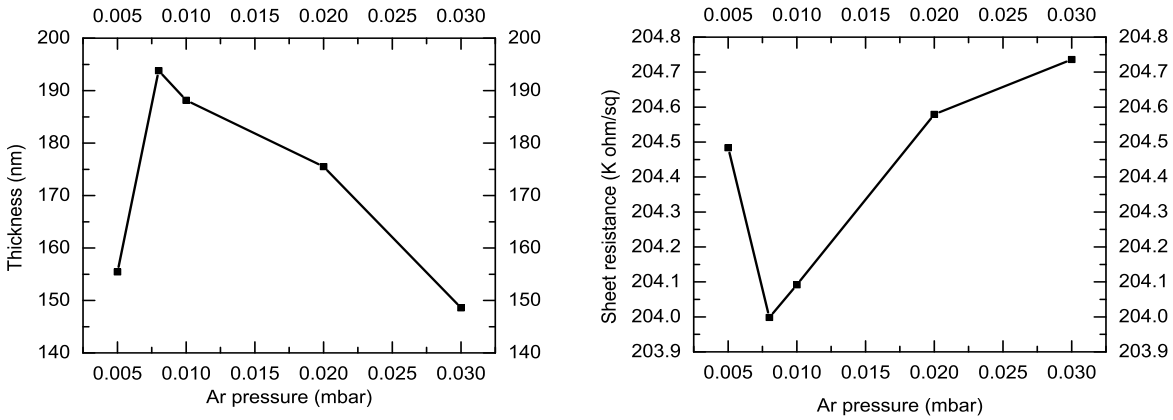

Figure 4.9: Effect of Ar gas pressure on (a) film thickness and (b) sheet resistance.

The influence of Ar pressure on the micro structure of ZnO films shown by AFM images in Fig 4.10. From the figure it can be observed that the film grown at the pressure of 8E-3 mbar has large crystal grains and hence more crystallinity. The sheet resistance of the films was measured by four probe measurement system. The influence of deposition pressure on the sheet resistance was shown in Fig 4.9 (b). The sheet resistance was decreased as pressure increased from 5E-3 to 8E-3 mbar, and it reached to its minimum at 8E-3 mbar, thereafter it increased with the pressure. The film grown at a pressure of 8E-3 has low sheet resistance and large

crystal grains (from the Fig. 33), thus exhibit more crystallinity and carrier concentration. So, the process gas pressure of 8E-3 mbar is the optimum pressure to grow Zno films thus all ZnO films deposited at this pressure through out the work. Before the deposition, process chamber is evacuated to base pressure of 1E-5 mbar. By varying the MFC controller Ar gas pressure set to 8E-3 mbar and deposition has done for specified time. The films grown here are very high resistive with sheet resistance of around 2,00,000. This could be expected because the ZnO target used here is pure ZnO and deposition was done at room temperature. So, these films may not suitable for device operation. The post growth annealing treatment could be done to decrease the sheet resistance of ZnO film.

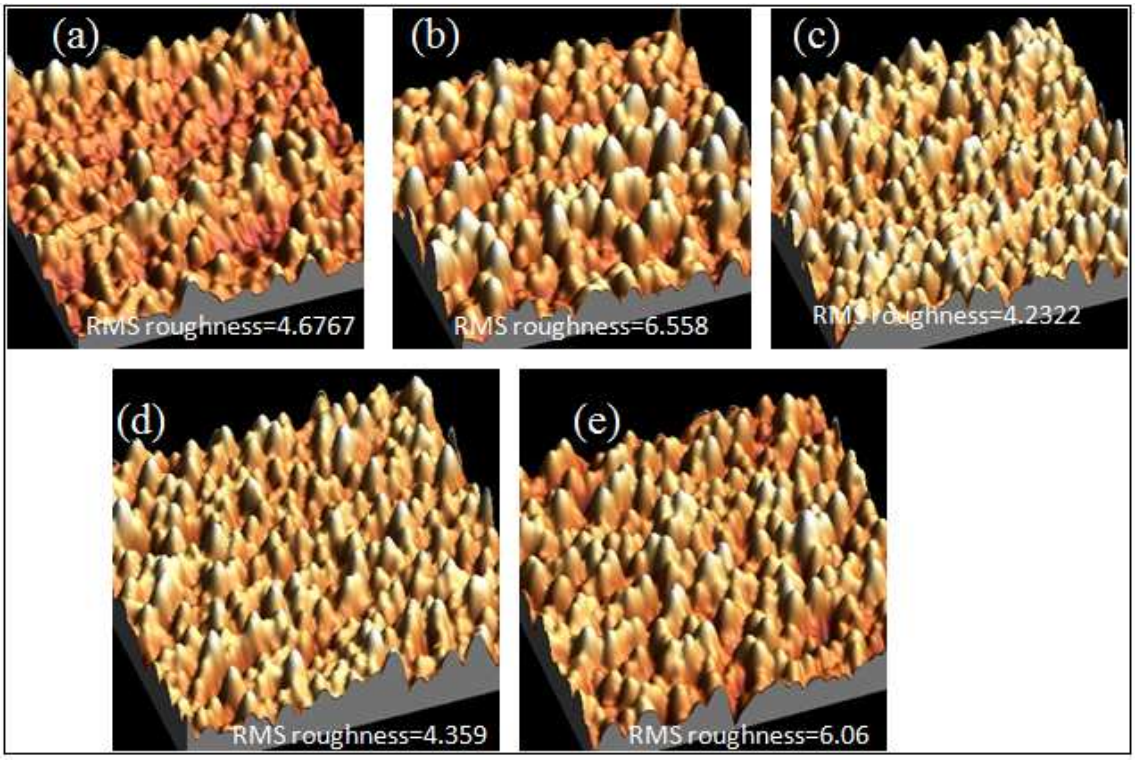

Figure 4.10: AFM images of films deposited at a Ar gas pressure of (a) 5E-3 mbar (b) bE-3 mbar (c) 1E-2 mbar (d) 2E-2 mbar (e) 3E-2 mbar.

4.5.2 ZnO etching

ZnO is reactive to most of the acids, alkaline and mixture solutions, So any of them can be used as etchants for ZnO, but the chosen etchant should not etch the bottom oxide layer. The solution of H_3PO_4, HAC (acetic acid) and H_2O is the frequently used etchant for ZnO [36]. But Tao Zhang et al. [38] reported that etchants like HCl and H_3PO_4 etches the ZnO very fast,

so it is difficult to etch in a controlled manner and leads to over etching and undercuts. They proposed that a weak acids like NH_4Cl provides uniform etch rates for entire surface without any under cuts. When NH_4Cl react with ZnO it under goes the following reactions [37].

$$2NH_4Cl_{(aq)} = 2{NH_4}^+{}_{(aq)} + 2{Cl}^-{}_{(aq)}$$
$$2{NH_4}^+{}_{(aq)} + 2H_2O = 2NH_{3(aq)} + 2H_3O^+$$
$$ZnO_{(s)} + 2H_3O^+ = {Zn}^{2+}{}_{(aq)} + 3H_2O$$

Here 5% NH_4Cl solution is used as etchant for ZnO. The 5% NH_4Cl solution etches the ZnO at a rate of approximately 5.5 nm/sec. Fig 4.11 shows cross section images of 120 nm thick ZnO films grown on SiO_2 after etching for 20 sec and 50 sec respectively. From Fig 4.11 (a), it can be observed that even after etching for 20 sec still some ZnO residuals present on SiO_2 surface, so it is better practice to over etch the film to remove the ZnO particles completely. However over etching for more time etches the ZnO film under the protected area and leads to curved edges as shown in Fig. 4.11 (b). With this fast etch rates, it is difficult to control the etch process of ZnO thin films. So, a less concentration of NH_4Cl can be used to etch thin ZnO films. The 1% NH_4Cl solution has an etch rate of approximately 2.5 nm/sec is used to etch thinner ZnO films.

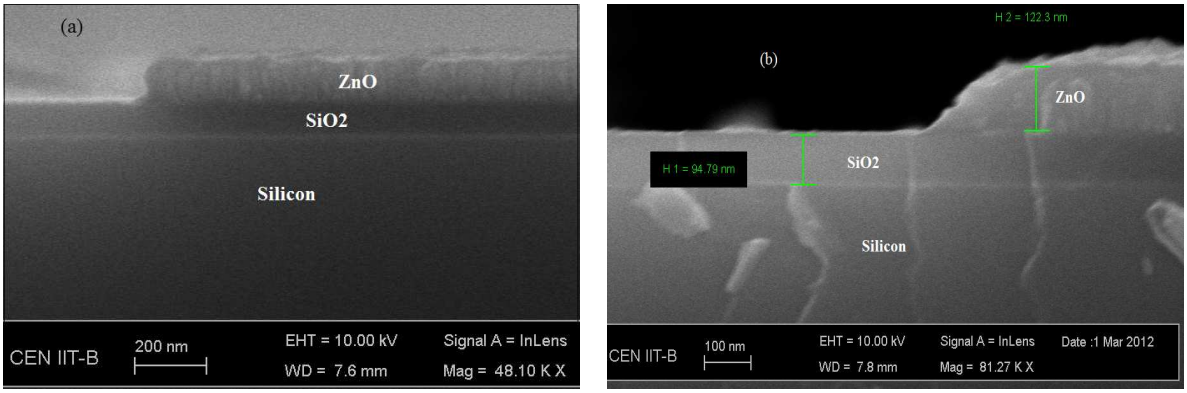

Figure 4.11: The cross section image of 120 nm thick ZnO films grown on SiO2 after etching for (a) 20 sec and (b) 50 sec respectively.

The ZnO based JLT was fabricated with the process described earlier. The I-V characteristics of a fabricated device is shown in Fig. 4.12. I-V characteristics of a JLT is not pretty much good Due to large resistivity of ZnO films. So, the resistivity of ZnO films should be decreased either by using doped ZnO target or by post deposition annealing.

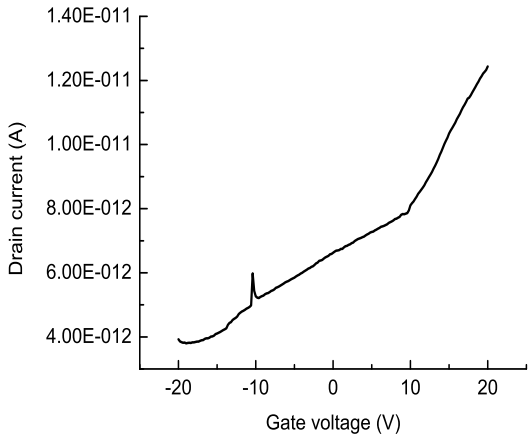

Figure 4.12: AFM images of films deposited at a Ar gas pressure of (a) 5E-3 mbar (b) bE-3 mbar (c) 1E-2 mbar (d) 2E-2 mbar (e) 3E-2 mbar.

4.6 Summary

We proposed a new device architecture for ZnO based SOI-JLT and BPJLT which uses the substrate layer on lightly doped substrate, that can relax the requirement of aggressive scaling of channel thickness by reducing the effective channel thickness by half. By using high-κ material instead of BOX, the on-to-off current ratio was improved by 8 orders of magnitude without degrading the on current by not more than one order of magnitude. The BPJLT with substrate layer has better immunity to channel length scaling and supply voltage scaling than the BPJLT without substrate layer. The detailed process flow of ZnO SOI-JLT was discussed.

Chapter 5

Conclusion and Future Work

Among the three types of vertical Tunnel FET devices, Structure 1 with channel thickness of 4 nm attains sub 60 mV/dec subthreshold swing with degraded ON currents. Circuit simulation of inverter and ring oscillator validates the working of proposed TFET device in circuit level. The device simulation of Dual-κ spacer architecture revealed that the Dynamic nonlocal band -to-band tunneling model model accurately calculated the tunneling currents in TFET devices. TEM results showed that amorphous Silicon deposited by solid phase epitaxial regrowth technique is of polycrystalline nature and amount of crystallization was increased with the annealing process.

We proposed a new device architecture for ZnO based SOI-JLT and BPJLT which uses the substrate layer on lightly doped substrate, that can relax the requirement of aggressive scaling of channel thickness by reducing the effective channel thickness by half. The BPJLT with substrate layer has better immunity to channel length scaling and supply voltage scaling than the BPJLT without substrate layer. An attempt was made in fabricating ZnO based JLT, ZnO deposition conditions were optimized.

The ZnO films that was grown have very high resistivity, resistivity of the films has to be decreased by either using doped ZnO target or by post growth annealing. The proposed ZnO SOI-JLT and BPJLT have to be fabricated and I-V characteristics of experimental devices have to be compared with that of simulation data.

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