Optimization of n-channel and p-channel T-FET

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By

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Abstract

In this work, we explore various optimization techniques using bandgap engineering to enhance the performance of tunnel FETs (T-FET) using extensive device simulations. We show that the heterostructure ($Si_{1-\gamma}Ge_{\gamma}$ source or drain) tunnel FET (HT-FET) architecture allows scaling of the device to sub 20 nm gate length regime. N-channel HT-FET is optimized to meet ITRS low standby power and high performance logic technology requirements with 20 nm gate length, for the first time. Novel optimization technique is proposed for p-channel T-FET which results in better subthreshold slope and increased ON current. For optimizing p-channel T-FET, we use a heterostructure with $Si_{1-\gamma}Ge_{\gamma}$ drain. The Ge content and the gate overlap are used as optimization parameters. Comparative study of gate length scaling effects on Si T-FET and HT-FET is done. We show that for sub 20 nm gate lengths, the heterostructure provides an added advantage of reducing short channel effects. We have also explored the possibility of CMOS implementation of HT-FET.

Key words: Band to band tunneling, sub 60mV/dec subthreshold slope, Tunnel FET (T-FET), Heterojunction tunnel FET (HT-FET), scaling.

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Declaration

The MEDICI models used for T-FET simulations in this work were received from Dr. Krishna K. Bhuwalka.

Chapter 1

Introduction

1.1 Why tunnel FET?

As the continuous down scaling of conventional MOSFET is reaching its fundamental limits, need for a replacement device is growing. MOSFET scaling is limited by various short channel effects like drain induced barrier lowering (DIBL), gate induced drain leakage (GIDL), tunneling leakages, increased power consumption due to non-scalability of subthreshold slope etc. To overcome these problems there is a renewed interest in exploring new devices. Schottky barrier MOSFETs [1-3], impact ionization MOSFETs (IMOSFET) [4-5], tunnel FETs (T-FET) etc. are some such devices, which reduce one or more short channel effects in conventional MOSFETs. Of all these short channel effects, increasing leakage, especially subthreshold leakage due to non-scalability of subthreshold slope is one of the most serious impediments to further scaling of classical MOSFETs. This limitation is due to thermionic emission based carrier injection. To overcome this limitation and continue scaling, one needs to explore novel device architectures which use different modes of carrier injection. Impact ionization MOSFET (I-MOSFET) is one such device having very low subthreshold slope (< 10mV/decade) [4]. However it requires high operating voltages and faces severe reliability issues. Tunnel FET (T-FET) is a device which uses tunneling mechanism for carrier injection. Very low OFF current as well as kT/q independent subthreshold slope has been experimentally demonstrated in T-FETs [6] [7]. Sub 60 mV/decade subthreshold swing is also experimentally demonstrated in these devices [8].

In this chapter we try to understand the T-FET device structure, its working principle and different electrical parameters. The remainder of this report is divided in to three chapters. Second chapter discusses the different optimization techniques for n-channel T-FET and we provide the device design space for n-channel heterojunction tunnel FET (HT-FET). Effect of gate length scaling for n-channel HT-FET is studied. In Chapter 3, we propose a novel device structure for optimization of p-channel T-FETs, and scalability of this device is investigated. In the fourth chapter we discuss the possible applications of tunnel FETs for CMOS logic and ultra low power supply (Vdd<0.5V) applications. Chapter 5 concludes this report, outlining the scope for future work in this direction. The appendix contains the different simulation experiences and, do's and don'ts with T-FET simulations.

1.2 T-FET device structure and working principle

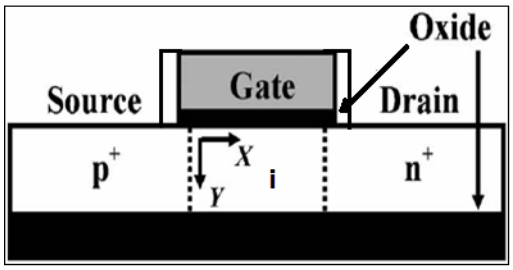


Figure 1.1 Device structure for T-FET

Fig.1.1 shows the tunnel FET structure on SOI. It is a gated P^+-i-N^+ diode, with the gate on intrinsic region, which forms the channel. P^+ region is the source and N^+ region is the drain. To get FET action, P-i-N diode is reverse biased by applying positive voltage at the N^+ region. Reverse biasing the P-i-N diode gives ultra low OFF current in T-FETs. It is desirable to keep the channel intrinsic [9], and hence statistical fluctuation of dopant atoms in the channel is not present. As shown in Fig. 1.2, in the OFF condition, conduction and valence bands are apart. Therefore tunneling of electrons is not possible and OFF current is determined by P-i-N leakage current. For n-channel operation, a positive gate voltage is applied at the gate which creates inversion/accumulation layer of electrons at the Silicon-gate oxide interface. As shown in Fig. 1.2, in the channel region, a positive gate voltage pushes down the conduction and valence bands thus reducing the tunneling width at the p^+ source and channel junction. This results in the tunneling of electrons from valence band of the p^+ region to conduction band of the channel. T-FET is an ambipolar device, i.e. the same device can be used for both p-channel and n-channel device operation.

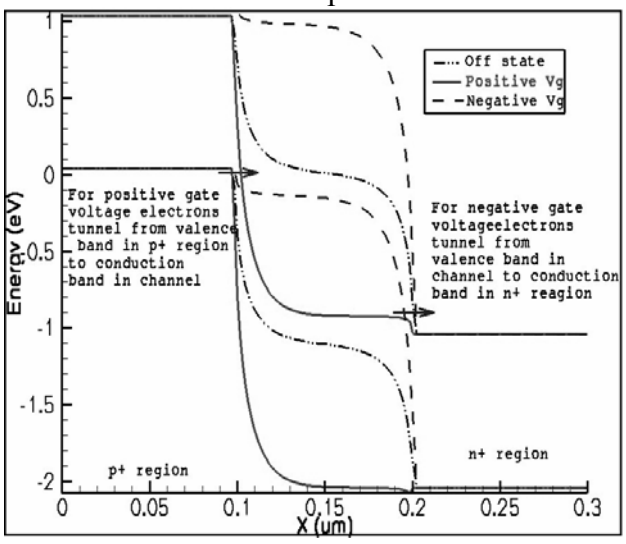
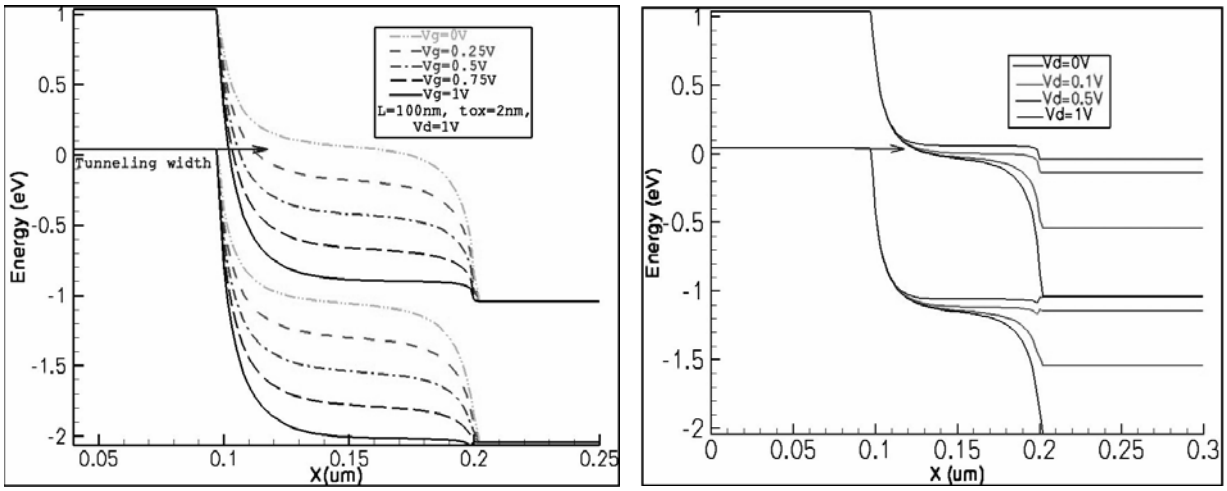


Figure 1.2: Band diagram at Si-SiO_2 interface for zero, positive and negative gate voltage, explaining the working principle of n-channel and p-channel T-FET

For p-channel operation, negative gate voltage is applied at the gate, forming an inversion/accumulation layer of holes at the Silicon-gate oxide interface. This results in pulling up of conduction and valence bands in channel and reduction in tunneling width at the channel and N^+ drain junction.

1.3 Tunneling width modulation

The requirements on the replacement device are such that they should have a MOSFET like action, i.e. carrier injection should be controlled by gate voltage and should show saturation with high drain voltage. In case of T-FETs carrier injection depends on the tunneling width. Fig 1.3 (a) shows the effect of gate voltage on tunneling width for n-channel T-FETs. Increasing gate voltage reduces the tunneling width, which increases the carrier injection. This is similar to conventional MOSFET, where increasing gate voltage reduces the barrier height for thermionic emission based carrier injection. Fig 1.3 (b) shows the effect of drain voltage on tunneling width. There is a reduction in tunneling width for lower drain voltages but there is no effect on tunneling width for high drain voltages, showing a clear saturation behavior.



(a) (b)

Figure 1.3 Band diagram at Si-SiO_2 interface showing tunneling width modulation by (a) gate voltage (b) drain voltage

1.4 Two dimensional T-FET device simulation tools and models

Two-dimensional computer device simulation is a very easy, efficient and cost effective way to understand physics of new devices and their optimization. In this work we have used the MEDICI device simulator. The reasons for choosing MEDICI device simulator

over Sentaurus are explained in Appendix I. For band to band tunneling, Kane's interband tunneling model is used. This model shows good match with experimental results [10]. Apart from Kane's model, a concentration dependent bandgap narrowing model is included, as both source and drain are heavily doped and tunneling current has a strong dependence on bandgap. Since the device characteristics are dominated by band to band tunneling, impact ionization model is not included. The models used here have been experimentally verified in Ref. [11] [12]. As tunneling involves both electrons and holes two carrier solutions are obtained. Gate leakage is not turned ON and all the simulations are done at room temperature.

1.5 T-FET transfer characteristics and electrical parameters

In this section, using the above mentioned device simulator and models we investigate current-voltage characteristics for n-channel and p-channel T-FETs. The characteristics shown in this section are for a Silicon T-FET with 20 nm gate length and tox of 1 nm. Fig. 1.4 (a) shows the transfer characteristics for an n-channel T-FET. There are two components in the T-FET drain current.

$$I = I_{pin} + I_{B2B} \tag{1.1}$$

I_{pin} is P-i-N leakage current which represents the flat portion of transfer characteristics, where band to band tunneling current is negligible. I_{B2B} is the band to band tunneling current which dominates the P-i-N leakage current and results in increase of drain current with gate voltage.

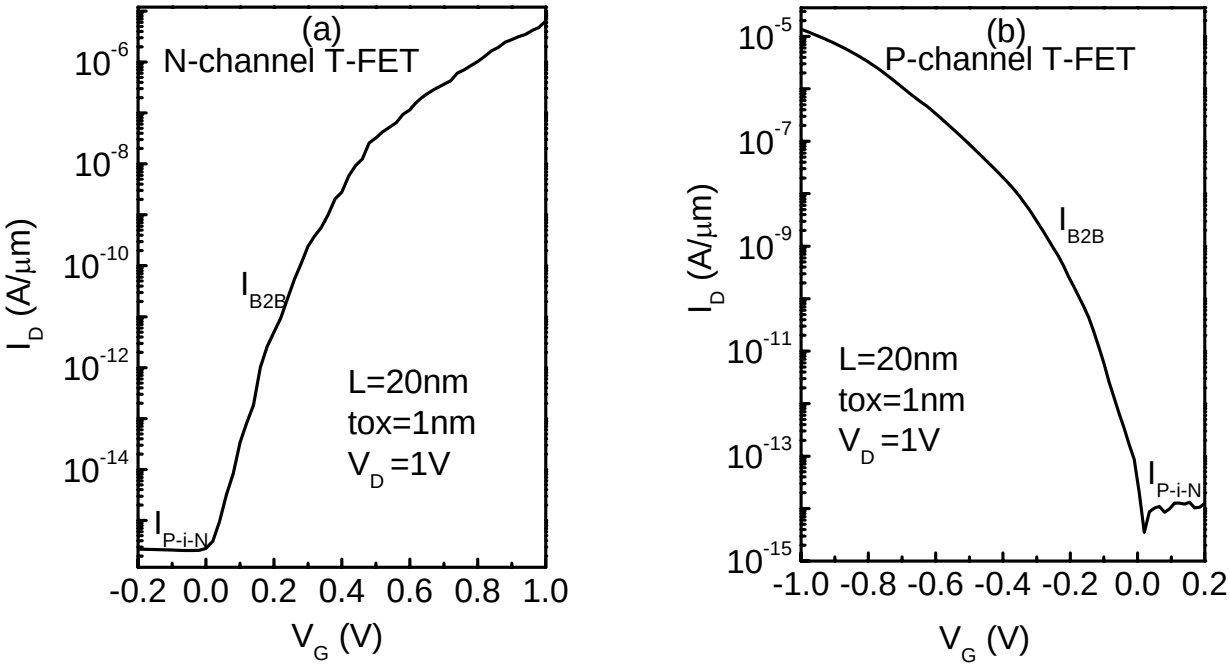


Figure 1.4 Transfer characteristics for (a) n-channel Si T-FET (b) p-channel Si T-FET

Similarly Fig. 1.4 (b) shows the transfer characteristics for a p-channel T-FET. For 20 nm gate length with EOT of 1 nm, an n-channel Silicon T-FET has an ON current of 7 μA/μm while for a p-channel T-FET it is 10 μA/μm. This current is almost two orders of magnitude lower than the ITRS requirements [13].

It is seen that the current voltage characteristics for a T-FETs are different from those of a conventional MOSFETs. For a conventional MOSFET, diffusion current dominates in the subthreshold region and drift-diffusion current in the ON condition, whereas a T-FET has tunneling current in both ON and OFF conditions. The electrical parameters like threshold voltage (Vt) and subthreshold slope (S) have different definitions for T-FET. For conventional MOSFET we define threshold voltage as the gate voltage required to produce surface potential of $2\Phi_B$, where Φ_B is bulk Fermi potential. However for experimental devices, it becomes difficult to determine surface potential and Fermi potential exactly and hence, the device Vt accurately. Other methods for determining Vt like linear extrapolation or maximum gm can not be used for T-FET as its working principle is very different from the conventional MOSFET. Therefore for T-FET we define constant current threshold voltage as the gate voltage required to produce a drain current of $1X10^{-8}$ A/μm. For T-FET we define Vt in saturation region i.e. for high V_D. Subthreshold slope is another important parameter for T-FET. By definition subthreshold slope is the voltage required to change the drain current by one decade in the subthreshold region. From Kane's model the expression for subthreshold slope for T-FET can be obtained as [11]

$$S = \frac{2.3V_G^2}{2V_G + B_{Kane}W_g^{3/2}/D} \tag{1.2}$$

where Wg is the bandgap and D is device geometry parameter. Unlike conventional MOSFET, S for T-FET has strong dependence on gate voltage. This can be explained with the help of band diagrams in Fig. 1.2, which shows that there is a large reduction in tunneling width for lower gate voltage and the reduction in tunneling width becomes smaller with increasing gate voltages. Due to gate voltage dependence there are two definitions of subthreshold slope for T-FET, spot subthreshold slope, calculated at particular value of gate voltage, and average subthreshold slope which is the average of spot values in subthreshold region.

Chapter 2

N-channel Heterojunction tunnel FET (HT-FET)

The working principle for T-FET is explained in detail in Chapter 1. It is observed from transfer characteristics, that Silicon T-FETs have low ON current. This is due to saturation in the tunneling barrier width which is limited by the abruptness of the doping profile at the tunneling junction and the Si band gap, low ON current have been experimentally observed in Si devices [6]. Various optimization schemes have been proposed to increase the ON current, such as use of double gate structure with high-k gate dielectric on ultra thin SOI [14]; using a lower band-gap material, like SiGe[7]; or forming a hetero-junction at the tunneling source [11] [15]. The former approach uses an effective silicon oxide thickness of 0.4 nm (physical thickness of 3 nm with high-k of 29) in order to meet ITRS requirements of 50 nm channel length in terms of ON current. Since this EOT is much thinner than the ITRS specifications [13], use of low band-gap material seems inevitable to sustain high ON current in these devices for sub-20 nm devices. Forming a SiGe delta layer at the tunneling junction in vertical tunnel FETs has been shown to improve the n-channel tunnel FET performance significantly at the same time maintaining the P-i-N diode reverse leakage current level as observed for Silicon tunnel FETs [7]. Tunnel FET with a SiGe source is also shown to improve the performance of n-channel devices [15]. However the performance of the reported devices is significantly inferior to the ITRS requirements.

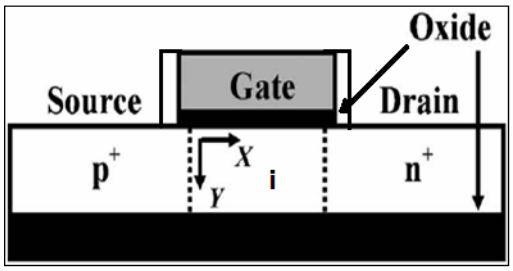
The approaches stated above fails to improve the p-channel tunnel FET performance. This is due to the fact that with SiGe layer, only the valance band discontinuity is achieved. The advantage using a smaller band-gap material in the entire source-channel-drain region is that both n-channel as well as p-channel performance is improved. However, due to lower band-gap, P-i-N diode leakage current increases thereby, losing some of the inherent advantages of the tunneling devices [7].

In this chapter using two-dimensional device simulations, we investigate in detail, the two band-gap modifying approaches for performance and scalability of the planar n-channel tunnel FETs. Performance design space in terms of band-gap using Si/SiGe layer, oxide thickness and channel length is explored. We show that with proper optimization, the n-channel tunnel FET can achieve the ITRS LSTP and high performance logic requirements for 20 nm gate length.

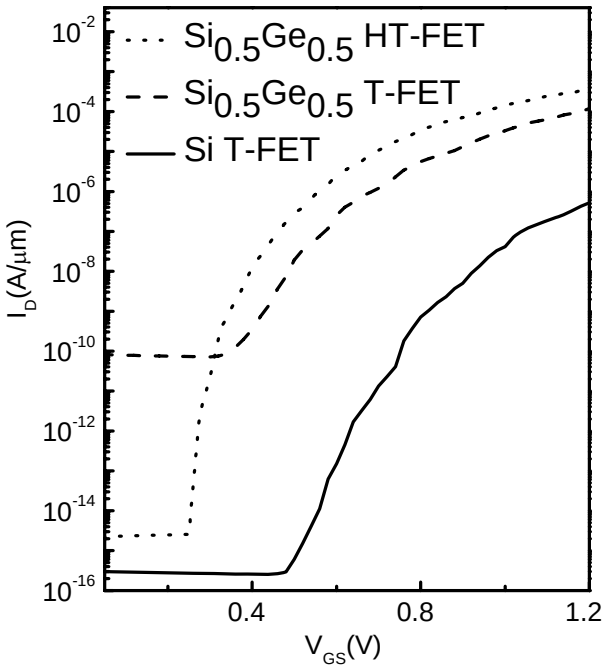
2.1 - Optimization of n-channel T-FET

2.1.1 Band-Gap Optimization:

Fig. 2.1 (a) shows the planar T-FET structure. In this section we focus on three n-channel tunnel FET structures, the first one based on the silicon (Si T-FET) where the device is formed on bulk Si. In the second structure, the source-channel and drain is replaced by SiGe with varying Ge content (SiGe T-FET); and third is the hetero-structure tunnel FET (HT-FET) where the P^+-source of Si T-FET is replaced by P^+-SiGe. Gate work function is fixed at 4.72 eV for these simulations and EOT is 1 nm and a gate overlap of 2 nm was used on both sides. We have used the gate overlap to get smooth transfer characteristics; however there is reduction in I_{ON} with increase in overlap on source side for N-channel HT-FET and drain side overlap has no effect on I_{ON}.



(a)



(b)

Figure 2.1: (a) Gated P-i-N structure for tunnel FET (T-FET). For n-channel HT-FET, P^+-region is $Si_{1-\gamma}Ge_{\gamma}$ and the rest Si. For T-FET, the entire semiconductor is either Si or SiGe. (b) Transfer characteristic for Si and $Si_{0.5}Ge_{0.5}$ T-FET and HT-FET.

Fig. 2.1(b) shows the transfer characteristics for the three structures. For the devices with SiGe, the Ge mole fraction is 0.5 corresponding to a band-gap of 0.75 eV [16]. As it can be seen, both the SiGe T-FET and HT-FET show a significant increase in the ON current as

compared to Si- T-FET. This is because the ON-current for tunnel FETs is an exponential function of the band-gap, I_{ON} for tunnel FET has been derived using Kane's model [10]

$$I_{DS} = A_{Kane} D^2 W_g^{-1/2} V_G^2 e^{-(B_{Kane} W_g^{-3/2})/DV_D} \quad (2.1)$$

Here A_{Kane} and B_{Kane} are constants dependent on the effective mass and W_g is the band gap at the tunneling junction. For SiGe T-FET, reduction in band-gap results in lowering of the tunneling barrier height, while the barrier width remains constant for a given V_G. While this results in improving ON current, sub-threshold swing does not show any improvement. It can be seen from equation (1.2), in Chapter 1, that subthreshold slope S is an inverse function of Wg [11]. Thus, lower Wg result in degraded swing. Furthermore, as the band-gap reduces, reverse biased P-i-N leakage current increases exponentially.

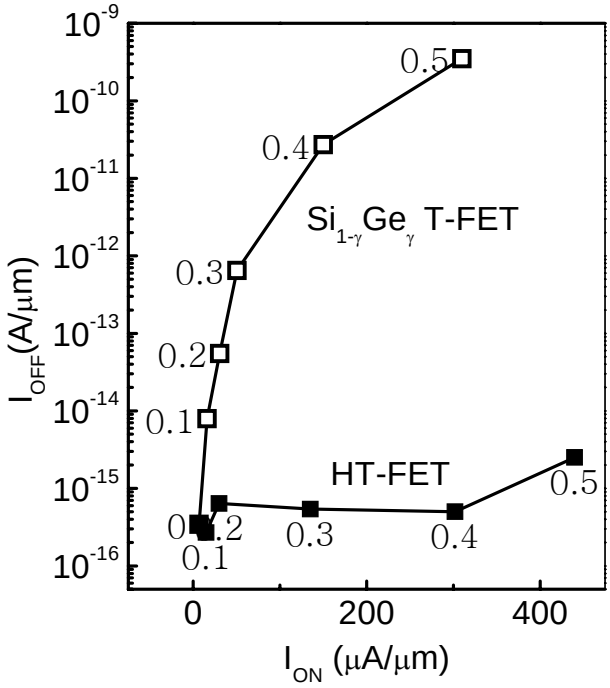


Figure 2.2: Comparison between two band-gap engineering techniques I_{ON} versus I_{OFF} as function of γ for n-channel SiGe T-FET and HT-FET. Values of γ are shown next to the data points.

For the HT-FET on the other hand, tunneling barrier height as well as barrier width is lowered at constant V_G. Since the S is strongly determined by the tunneling barrier width, there is a significant improvement in S and the hetero-structure provides a diffusion barrier comparable to that of Si rendering the P-i-N leakage current almost independent of Ge content. Thus, as

shown in Fig. 2.2, I_{ON}-I_{OFF} improves significantly as compared to SiGe T-FET. I_{OFF} is defined in the flat portion of the I_D-V_G.

2.1.2 Effect of EOT scaling

Fig. 2.3 shows the effect of EOT scaling on transfer characteristic of the HT-FET for Ge content, γ = 0.5 at V_D = 1 V for L= 20 nm. EOT is scaled from 1.8 nm to 0.8 nm. Due to increasing electric field at the tunneling junction, as EOT scales, ON current increases from 110 μA/μm to 529 μA/μm for EOT scaling from 1.8 nm to 0.8 nm. Due to stronger coupling between the gate and tunneling junction, sub-threshold swing improves and V_t lowers (measured at constant drain current of 1E-8 A/μm).

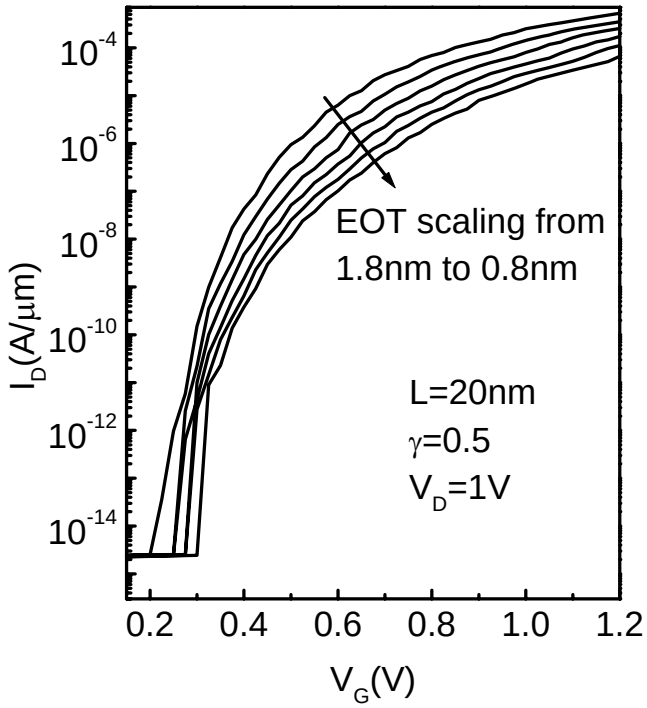


Figure 2. 3: Transfer characteristics for n-channel HT-FET with 50% Ge as function of EOT with L = 20 nm and V_D = 1V. EOT = 1.8, 1.6, 1.4, 1.2, 1.0 and 0.8 nm.

It may be noted that unlike the conventional MOSFET, EOT scaling has little impact on the sub-threshold OFF current. This is because the OFF current is dominated by the P-i-N diode leakage current which is independent of gate oxide thickness. Thus, it remains constant at 1 fA/um corresponding to the P-i-N diode leakage current. It should be pointed out that for very thin gate-oxide, direct tunneling through the oxide will eventually limit the OFF current in these devices. However, this can further be suppressed by using an appropriate high-k dielectric material as in conventional MOSFETs.

2.1.3 Effect of $Si_{1-\gamma}Ge_\gamma$ bandgap on HT-FET

In this section we investigate the effect of $Si_{1-\gamma}Ge_\gamma$ bandgap on HT-FET performance. $Si_{1-\gamma}Ge_\gamma$ bandgap is varied by varying Ge content γ. In MEDICI the band gap for $Si_{1-\gamma}Ge_\gamma$ at T = 90 K is determined by the following equations [16].

$$\begin{aligned} W_g(\gamma) &= W_g(90) - 0.4(W_g(90) - 0.95)\gamma; \gamma \le 0.25 \\ &= 0.950 - 0.667(\gamma - 0.25); 0.25 < \gamma < 0.40 \\ &= 0.850 - 0.575(\gamma - 0.40); 0.40 < \gamma < 0.60 \\ &= 0.735 - 0.433(\gamma - 0.60); 0.60 < \gamma < 0.75 \\ &= 0.67; \gamma \ge 0.75 \end{aligned} \tag{2.2}$$

Since all simulations are done for temperature T = 300 K band gap is calculated from the lattice temperature dependent energy band-gap model as follows [5].

$$W_g(\gamma, T) = W_g(\gamma, 300) + \alpha\left[\frac{300^2}{300 + T} - \frac{T^2}{T + \beta}\right] \tag{2.3}$$

Where $\alpha = 4.73*10^{-4}$ eV/K and β = 636 K.

Fig. 2.4 (a) shows the effect of Ge fraction γ in $Si_{1-\gamma}Ge_\gamma$ on the transfer characteristics of HT-FETs. With increase in γ there is an increase in ON current and reduction in the subthreshold slope. Fig. 2.4 (b) shows the average value of subthreshold slope as a function of γ. Average subthreshold slope is calculated for I_{DS} increasing from I_{OFF} to 1E-8 A/μm.

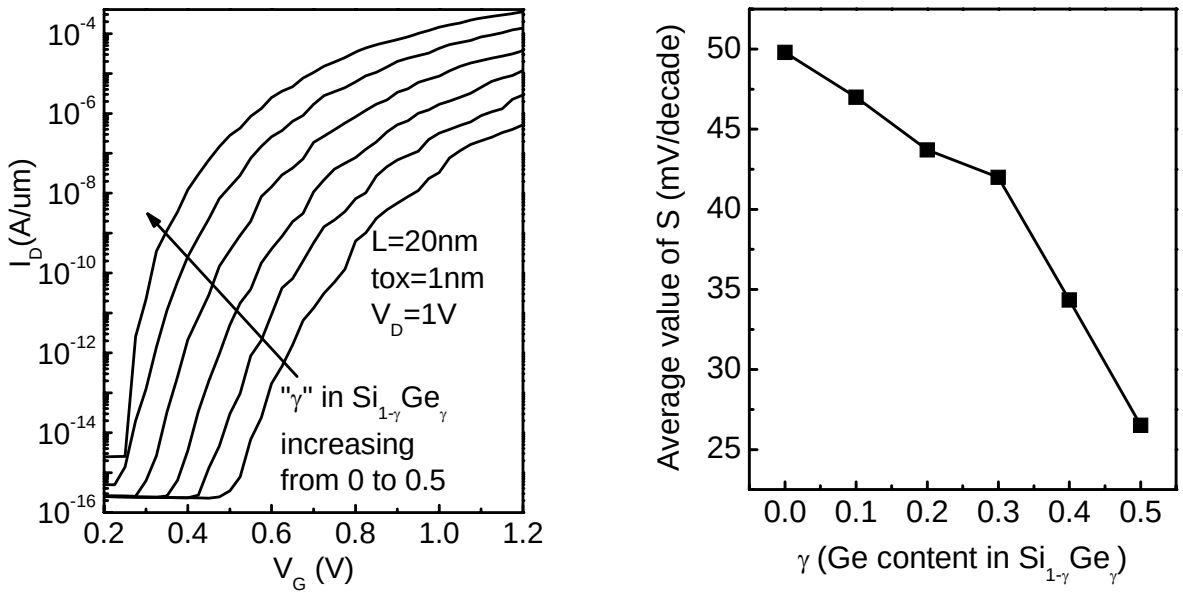


Figure 2.4: (a) Transfer characteristics for HT-TFET as function of Ge fraction of γ

(b) Corresponding average subthreshold slope as function of γ

The reasons for improvement in subthreshold slope is clear from Fig. 2.5 which shows the band-diagram at Si-SiO_2 interface for different gate voltages and for two cases one with $\gamma = 0.0$ and $\gamma = 0.5$. The reduction in tunnelling width with gate voltage is larger for HT-FETs than that for Si T-FETs. We define V_{OFF} as the gate voltage at which band to band tunnelling current dominates the P-i-N leakage current. Due to reduced barrier height for HT-FETs, the tunnelling current for HT-FETs is higher than for Si T-FET with the same tunnelling width, due to this V_{OFF} for HT-FETs is lower than Si T-FETs. This results in lesser bending in conduction band in the channel due to gate voltage for HT-FETs than for Si T-FETs. The steep conduction bands in case of Si T-FETs result in lower reduction in tunnelling width with gate voltage than that for HT-FETs where the conduction bands are flatter. This results in higher average S for Si T-FETs than HT-FETs.

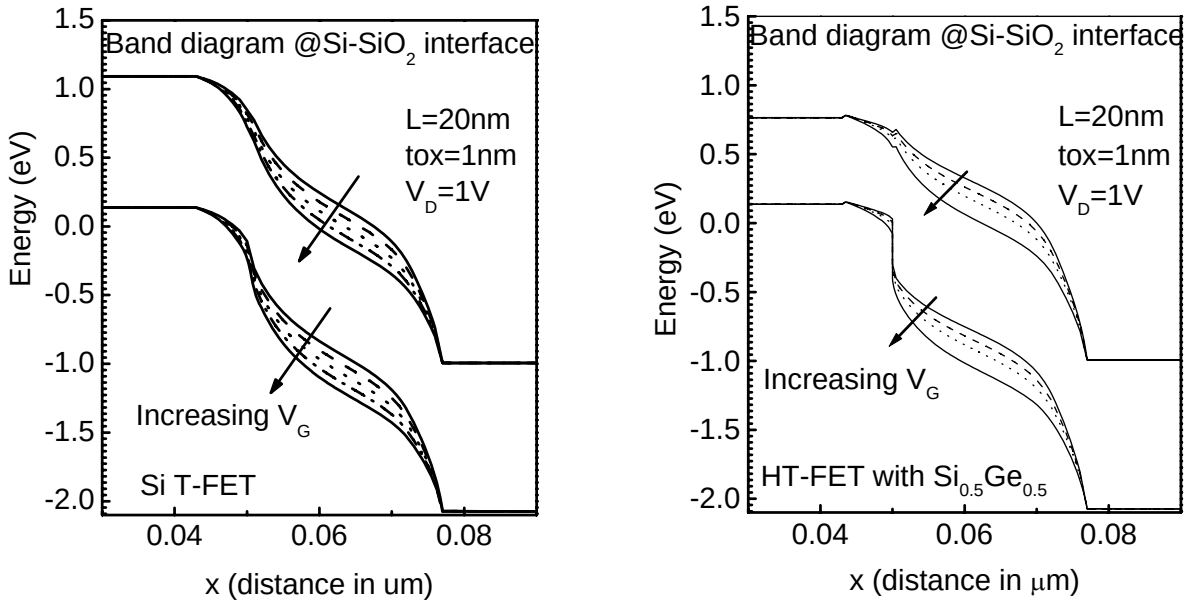


Figure 2.5: Band diagram across the device with gate voltage varied in steps of 0.1 V for Si T-FET and HT-FET; showing that the flatter bands in channel region for HT-FET results in larger reduction in tunneling width with varying V_G.

2.1.4 Impact of gate length scaling

In this section we discuss the impact of channel length, L scaling on the n-channel tunnel FET characteristics. As tunneling probability in Si is negligible for tunneling width, w > 10 nm, the tunnel FET characteristics are expected to be independent of L scaling down to 10 nm. In Fig. 2.6 we show the transfer characteristic for Si T-FET and HT-FET respectively, as a function of L. It is scaled from 70 nm to 15 nm at fixed EOT of 2 nm. As seen in Fig.

2.6, the Si T-FET shows significant degradation in S, resulting in degradation in leakage current, I_{OFF} furthermore; ON-current is almost independent of L scaling. This is due to the fact that when the device is OFF, for a fully depleted channel, the tunnel barrier width, w_0 at

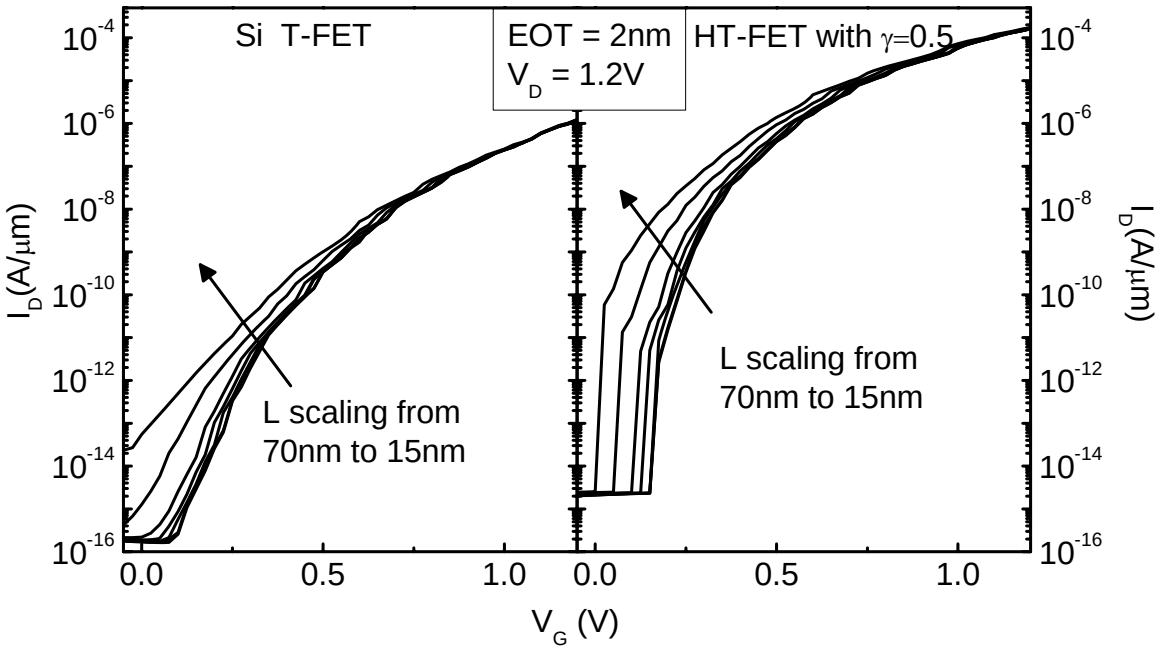


Figure 2.6: Transfer characteristics for n-channel Si T-FET and HT-FET as function of gate length scaling from 70 nm to 15 nm with EOT=1 nm and V_{DS}=1.2V.

V_G=0V is determined by L. As L scales, w_0 scales. This degrades the gate-control at fixed V_{DD}, and similar to conventional MOSFET, subthreshold swing degradation is observed. However, in the ON-state, $V_G \geq Vt$, tunneling barrier width, w is determined by the channel in inversion and is less than 5 nm. Thus, L scaling has little impact on the ON current, and the current-voltage characteristics are essentially independent of L scaling. For the case of HT-FET, as can be seen from Fig. 2.6, the sub-threshold swing as well as I_{OFF} is nearly independent of L scaling. In this case, tunnel barrier width is significantly lowered by band-discontinuity at tunnel junction even at $V_G = 0$ V. Thus, the subthreshold swing as well as I_{ON} is nearly independent of L.

2.1.5 HT-FET for sub 20 nm gate lengths

Fig. 2.6 shows that, for Si T-FET there is large degradation in subthreshold slope for L < 20 nm. Also for L = 15 nm the OFF current for Si T-FET is larger than that for HT-FET. Due to ambipolar nature of T-FET, the OFF current for smaller channel lengths is determined by tunneling at drain end (tunneling current for p-channel T-FET). To reduce OFF current of n-channel T-FET we have to suppress the p-channel characteristics. For sub 20 nm channel lengths HT-FET gives better suppression of p-channel characteristics. Fig. 2.7 (a) shows the band diagram for Si T-FET and HT-FET with L=15 nm in OFF condition. For larger channel lengths the tunneling width at drain end for both Si and HT-FET remains same, however for L=15 nm it is less for HT-FET than that for Si T-FET.

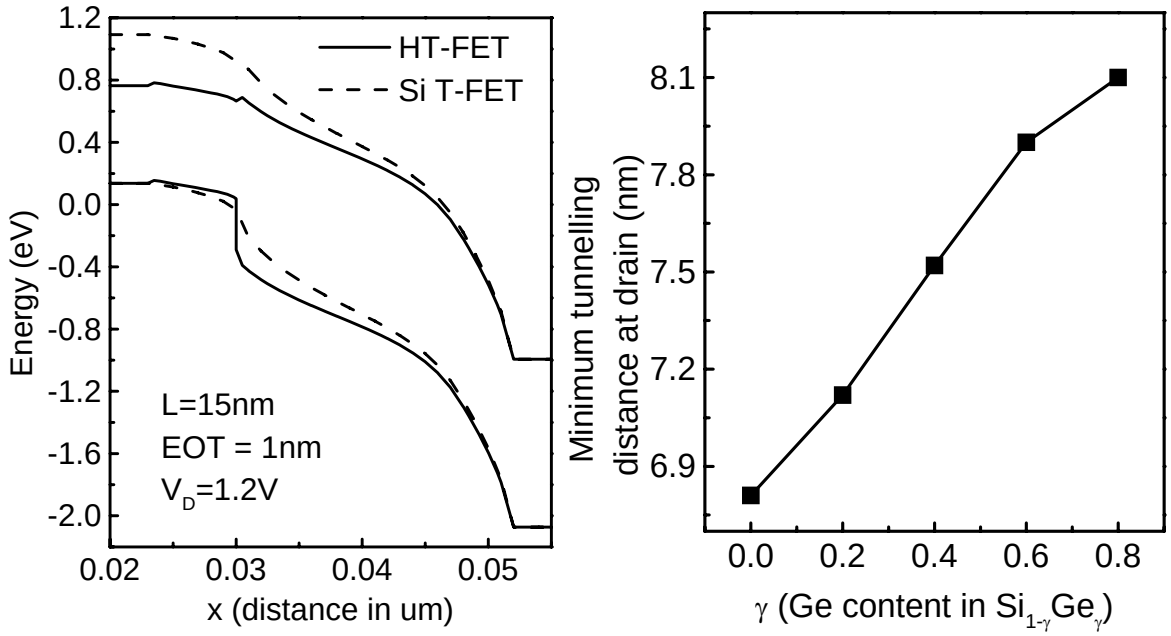


Figure 2.7: (a) Band diagram for n-channel Si T-FET and HT-FET with 50% Ge at Si-SiO_2 interface in OFF condition for 15 nm gate length (b) minimum tunneling width at drain end as function of Ge fraction for n-channel HT-FET.

With increase in the Ge content, valence band offset increases. This increases the tunneling distance at drain end, giving better suppression of p-channel characteristics. This is clear from Fig. 2.7 (b) which shows tunneling width at drain end against γ for L = 15 nm

2.2 N-channel HT-FET Design space

From the results discussed so far, it is seen that I_{ON}-I_{OFF} of the n-channel HT-FET is influenced by EOT and Ge fraction in $Si_{1-γ}Ge_γ$. Gate work function can be adjusted to shift the

transfer characteristics of the HT-FET, so that required values of I_{OFF} can be obtained. We have attempted to optimize these three parameters so that HT-FET meets the ITRS requirements of both low standby power and high performance logic applications for 20 nm gate length. We define V_{OFF} as the gate voltage at which the flat part of the I_D-V_G meets the exponentially increasing section. Gate work function is adjusted so that V_{OFF} = 0V, and definition of I_{ON} and I_{OFF} is similar to conventional MOSFET. The ITRS requirements of low standby power applications and high performance logic applications for 20 nm gate lengths are shown in table 1. Fig. 2.8 (a) shows the ON current for HT-FET as function of EOT and Ge fraction γ in $Si_{1-\gamma}Ge_{\gamma}$. HT-FET meets the ON current requirements for LSTP applications with 55% and more Ge percentage in SiGe for ITRS specified EOT value (1.1 nm). If we use SiGe source with 60% Ge, ON current requirements are met for EOT of 1.6 nm, hence EOT can be relaxed by 5 Å than ITRS specifications. For higher Ge percentage, there is larger freedom to increase EOT. High performance logic requirements are satisfied with Ge percentage of 60% for ITRS specified EOT value of 0.75 nm. For higher Ge percentage in SiGe we can relax the EOT values than ITRS targets. Thicker gate dielectric will reduce the direct tunneling leakage through gate dielectric, which would allow us to take full advantage of the low OFF current of the HT-FET. Fig. 2.8 (b) shows OFF current against EOT and γ. OFF current is almost independent of EOT scaling, however there is exponential increase in OFF current for γ greater than 0.4. However for 60% Ge the OFF current is $2*10^{-14}$ A/μm which is 3 and 7 orders of magnitude less than ITRS specifications for LSTP and high performance logic requirements respectively. Even for maximum Ge percentage the OFF current is less than the ITRS targets. Fig. 2.8 (c) shows the work functions required to bring V_{OFF} point to zero. For LSTP applications γ = 0.6 and EOT = 1.2 nm the work function is 4.5 eV. Similarly for high performance logic applications with 0.8 nm EOT and 60% Ge the work function required is 4.5 eV. Fig. 2.8 (d) shows average subthreshold slope plotted against the device design parameters (EOT and γ). We have defined the threshold voltage as gate voltage required for drain current of $1*10^{-8}$ A/μm. Average subthreshold slope is calculated for currents from I_{OFF} to $1*10^{-8}$ A/μm. For 60% and higher Ge content where HT-FET satisfies ITRS requirements, the subthreshold slope is less than 35mV/decade for EOT less than 1.8 nm. As stated earlier with increase in Ge percentage there is improvement in subthreshold slope. The subthreshold slope also decreases with EOT scaling, but it can be observed that the reduction in subthreshold slope with EOT is higher for lower Ge percentage and becomes less sensitive to EOT for higher Ge percentage. To reduce gate leakage and reduce gate

capacitance we increase the EOT than ITRS specification without much degradation in subthreshold slope as change in S with respect to EOT scaling is very less for higher Ge percentage.

Table 2.1

		LSTP	HP
ITRS specifications	EOT (nm)	1.1	0.8
	V_{DD}(V)	1	1
	I_{ON}(mA/μm)	0.519	1.639
	I_{OFF}(μA/μm)	3.03 E-5	0.7
HT-FET design parameters	γ	0.6	0.6
	Work function	4.5	4.5
n-channel HT-FET performance	I_{ON} (mA/μm)	0.77	1.45
	I_{OFF} (μA/μm)	2 E-8	2.1 E-8
	Average S (mV/decade)	31.5	22.7

Table 1. ITRS specifications for 20 nm gate length devices and performance of n-channel HT - FET

2.3 Summary

In this chapter, we have seen that out of two band-gap engineering approaches, HT-FET gives better performance. We have shown that n-channel HT-FET satisfies ITRS LSTP and high performance logic requirements for 20 nm gate length with a freedom of using higher EOT values than ITRS targets and can be scaled below 20 nm gate length without much degradation in performance.

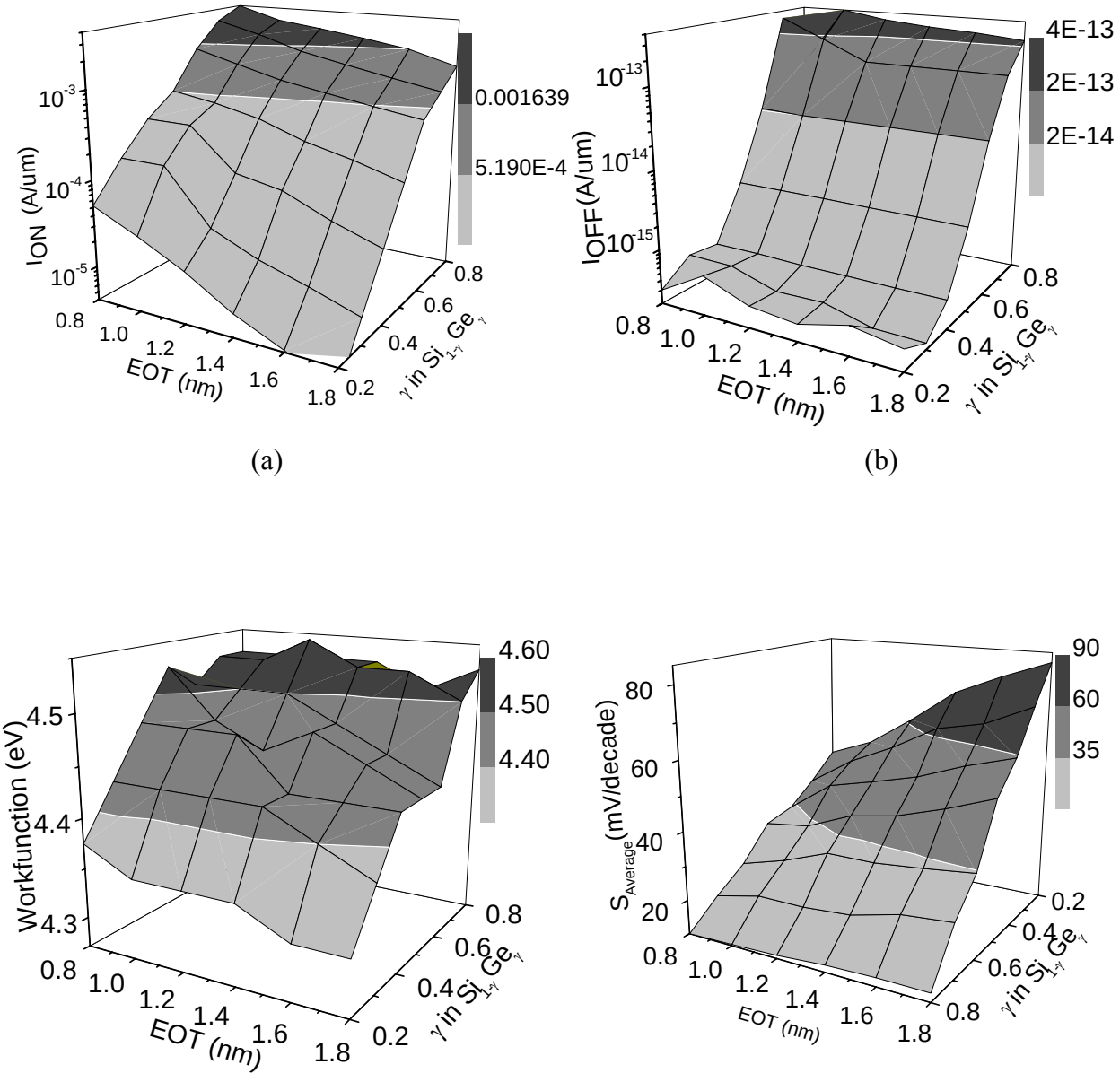


Figure 2.8: Design space for n-channel HT-FET with EOT and Ge fraction γ as device design parameters showing HT-FET meets the ITRS LSTP and High performance logic requirements (a) I_{ON} (b) I_{OFF} (c) gate metal work function (d) subthreshold slope.

Chapter 3

P-channel Heterojunction tunnel FET (HT-FET)

Tunnel FET is an ambipolar device i.e. same device can be used to get p-channel as well as n-channel characteristics. As shown in Fig. 1.2, by applying a negative gate voltage the device can be made to operate like a p-channel tunnel FET. In this case, tunneling takes place from the channel to the N^+ drain. Fig. 3.1 shows the working principle of p-channel tunnel FET.

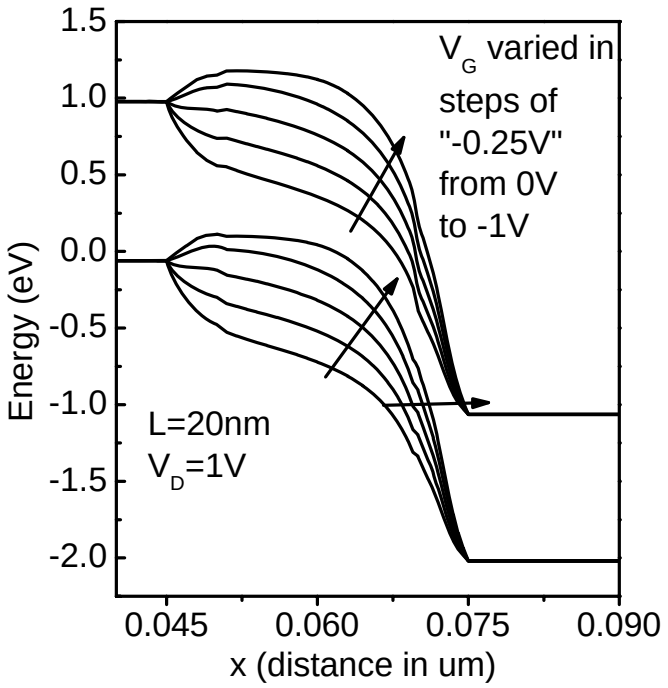
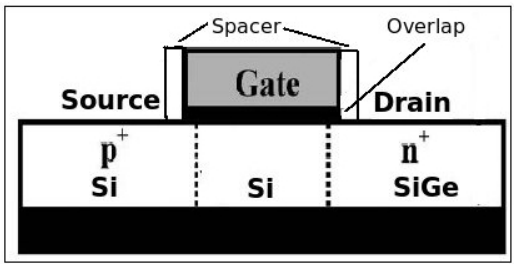


Figure 3.1: Band diagram at Si-SiO_2 interface for Si T-FET showing tunneling width modulation by negative gate voltage for p-channel mode of operation.

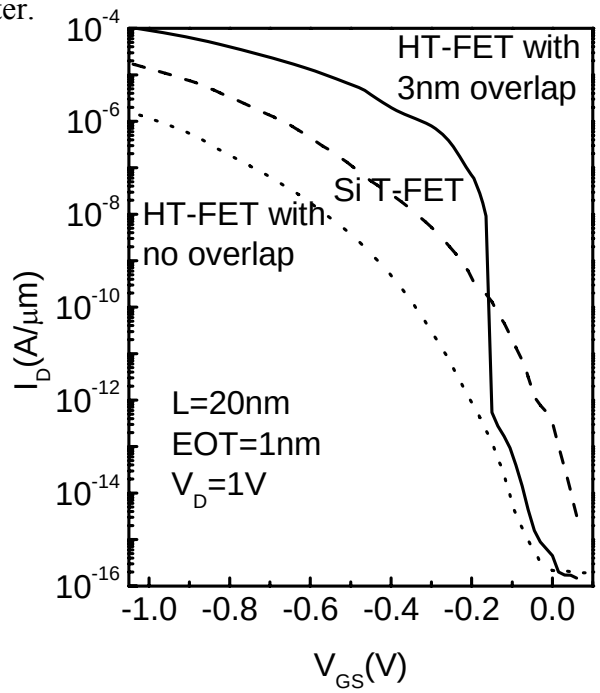
In this case, on application of a negative gate voltage, an inversion layer of holes is formed at the Si-SiO_2 interface. Conduction and valence bands in the channel region, at the Si-SiO_2 interface are lifted, resulting in reduction in tunneling width at intrinsic channel and N^+ drain junction. As seen in Chapter 1, p-channel T-FET on Si shows low ON current. In this chapter we first propose new device architecture (p-channel HT-FET) to enhance p-channel performance. The effects of gate length scaling are discussed in a latter section.

3.1 Optimization of p-channel T-FET

As stated earlier, p-channel T-FETs on Si have low ON current. ON current can be enhanced using lower band-gap material, which would also increase the OFF current as in the case of SiGe N-channel T-FET [17]. The use of heterostructure at tunneling junction does not result in improved performance [18]. This is because in this case, the tunnel junction is formed by the p-channel and N^+ drain and tunneling takes place from the valance band in the channel to the conduction band in the N^+ drain. Simply replacing the Si N^+ drain with SiGe will result in valance band discontinuity but not a discontinuity in conduction band. Thus, in order to enhance the p-channel performance, we propose a novel structure, which is shown in Fig. 3.2 (a). Here, N^+ drain region in Si T-FET is replaced by N^+ SiGe layer and gate overlap on drain side is used as a device design parameter.



(a)



(b)

Figure 3.2 : (a) P-channel HT-FET structure formed by replacing N^+ Si drain of Si T-FET by N^+ $Si_{1-\gamma}Ge_\gamma$ drain and gate overlap on drain side (b) Transfer characteristics for P-channel Si T-FET and HT-FET with 30% Ge and 3 nm overlap and no overlap showing advantages of HT-FET.

Fig. 3.2 (b) shows the transfer characteristics for (i) p-channel Si T-FET (ii) p-channel HT-FET with N^+ $Si_{0.7}Ge_{0.3}$ drain and 3 nm gate overlap and (iii) p-channel HT-FET with N^+ $Si_{0.7}Ge_{0.3}$ drain and with no overlap. For p-channel HT-FET with no overlap, there is no improvement in subthreshold slope or ON current. The transfer characteristics shift left.

However the HT-FET having overlap of 3 nm has higher ON current and lower subthreshold slope. Here we have used overlap of 3 nm on source side to get symmetrical structure, however source side overlap has no effect on transfer characteristics. The reason for improvement in subthreshold slope and ON current can be explained with the help of band diagram in Fig. 3.3 which shows band diagram for p-channel Si T-FET and p-channel HT-FET with 30% Ge in N^+ SiGe drain and 3 nm overlap, at Si-SiO_2 interface for increasing gate voltage in subthreshold region.

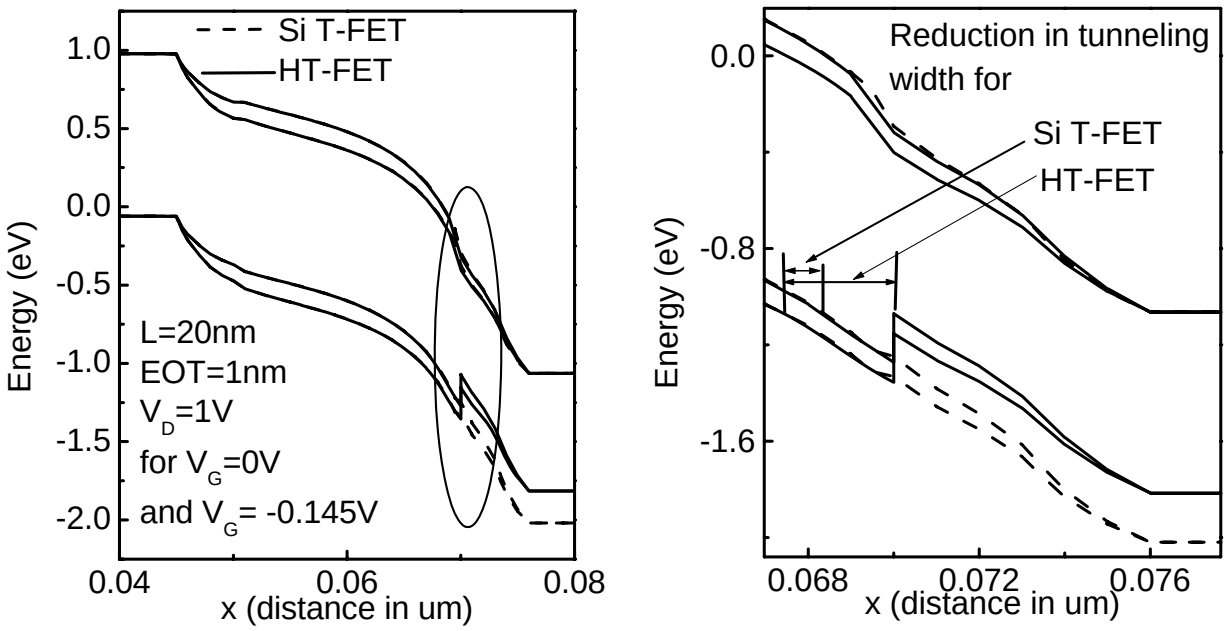


Figure 3.3: Band diagram at Si-SiO_2 interface for p-channel Si T-FET and HT-FET and its enlarged view at the tunneling junction. Due to heterojunction and overlap there is larger reduction in tunneling width for HT-FET than Si T-FET.

With increasing negative gate voltage the tunneling width for electrons tunneling from valence band of channel to conduction band in N^+ drain reduces. In HT-FET, for initial voltages the electrons tunnel from Si channel to SiGe drain as explained earlier. SiGe in drain do not affect the tunneling width and hence the subthreshold slope is similar to Si T-FET. However for sufficiently large negative gate voltage, the valence band of overlapped SiGe aligns with the conduction band of drain SiGe (non-overlapped) causing large reduction in tunneling width and electrons starts tunneling from SiGe valence band to SiGe conduction band. As shown in Fig. 3.3, the valence band offset between Si and SiGe results in a large reduction in tunneling width as compared to a Si tunnel FET. This results in very low

subthreshold slope after Vg = -0.145V in transfer characteristics for the new device structure. Fig. 3.4 shows the effect of gate overlap on transfer characteristics of p-channel HT-FET with 30% Ge. With increasing gate overlap, ON current increases and also the gate voltage for which valence band of overlapped SiGe aligns with the conduction band of drain SiGe, shifts towards zero.

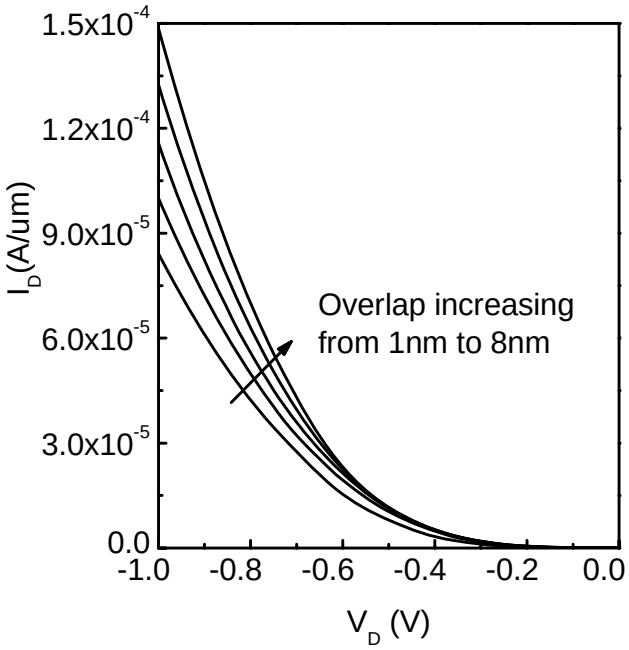


Figure 3.4: Transfer characteristics for p-channel HT-FET with 30% Ge as a function of gate overlap.

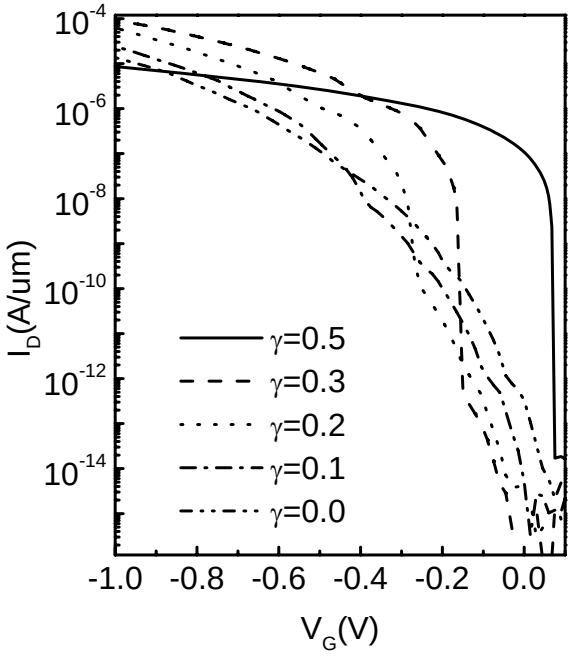


Figure 3.5: Transfer characteristics for p-channel HT-FET as function of Ge fraction, showing for an overlap of 3 nm, 30% Ge gives maximum ON current.

Fig. 3.5 shows transfer characteristics for p-channel HT-FET for different Ge percentages. It can be observed that with increasing Ge percentage the gate voltage for which valence band of overlapped SiGe aligns with the conduction band of drain SiGe, resulting in sudden increase in current shifts towards zero volts. There is an optimum value of Ge percentage for which ON current is maximum. However subthreshold slope improves with increasing Ge percentage.

3.2 Scaling issues with P-channel T-FET

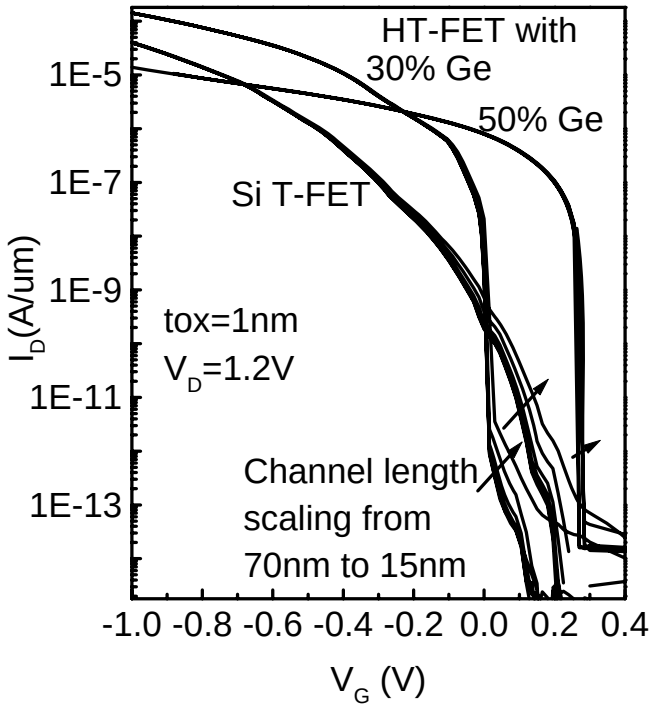


Figure 3.6: Transfer characteristics for p-channel Si T-FET and HT-FET with 30% and 50% Ge and 3 nm gate overlap for gate length scaling from 70 nm to 15 nm

Fig. 3.6 shows the transfer characteristics for p-channel Si T-FET and HT-FET with 30% and 50% Ge and 3 nm gate overlap for different gate lengths. Similar to n-channel Si T-FET there is subthreshold slope degradation and small threshold voltage roll-off with channel length scaling. Subthreshold slope for p-channel HT-FET is similar to Si T-FET till the gate voltage at which the valence band of overlapped SiGe aligns with the conduction band of drain SiGe (non-overlapped), till this point the tunneling mechanism in HT-FET is similar to Si T-FET. However after this gate voltage, HT-FET action starts and determines the current and transfer characteristic becomes independent of gate length. As discussed earlier, with increase Ge percentage the gate voltage at which HT-FET action starts moves towards zero. With higher

Ge percentage (50%), we can make HT-FET transfer characteristics independent of gate length, but at the cost of ON current. Another way to make transfer characteristics independent of gate length without ON current degradation is to do gate work function engineering such that the point at which HT-FET action starts is shifted to zero. This will result in some increase in OFF current, however it is much less than ITRS specifications.

3.3 Summary

In this chapter, we have seen that the proposed novel device structure, p-channel HT-FET shows remarkable improvement in I_{ON} and subthreshold slope over Si T-FET. We have shown that similar to n-channel HT-FET, p-channel HT-FET can be scaled below 20 nm gate length without any sever short channel effects.

Chapter 4

T-FET CMOS implementation

From the discussion so far, it is clear that the HT-FET is the most promising candidate for enabling further scaling without introducing severe short channel effects. After optimizing HT-FET to meet ITRS requirements, in this chapter we will discuss HT-FET implementation for digital CMOS logic. In a latter section of this chapter we will discuss use of HT-FET for ultra low power supply applications as a replacement to conventional subthreshold logic applications. As discussed earlier, both n-channel and p-channel HT-FET shows very low subthreshold slope, which makes them very useful for ultra low power supply applications.

4.1 HT-FET for digital CMOS application

Fig. 4.1 (a) shows the n-channel and p-channel T-FET connections for a CMOS inverter. Fig. 4.1 (b) shows the inverter with symbols for T-FET. Here the notch in the T-FET symbol indicates the tunneling junction [19]. For the HT-FET inverter, p-channel and n-channel T-FETs are replaced by corresponding HT-FETs.

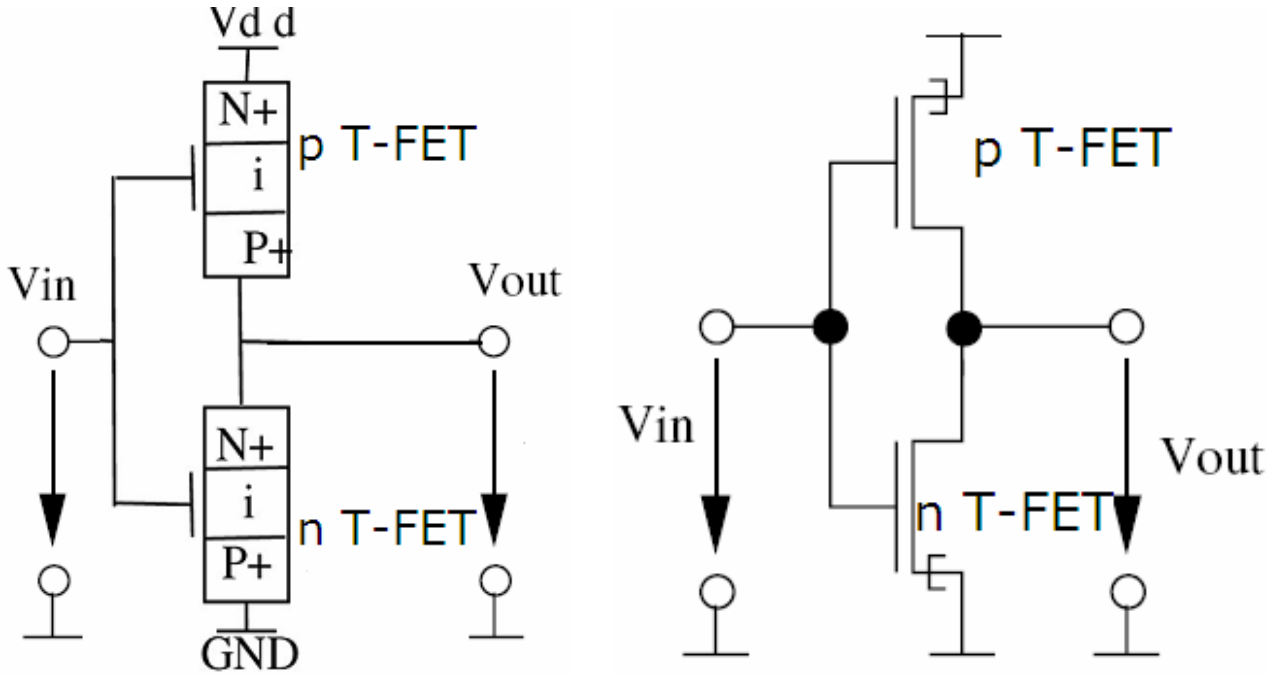


Figure 4.1 N-channel and p-channel T-FETs connected to form CMOS inverter and corresponding symbols for T-FETs.

Similar to conventional MOSFETs, n-channel HT-FETs act as pull down devices and p-channel HT-FETs as pull up devices. The basic idea behind the connection is that the P-i-N diode should be reverse biased. This is done by connecting the P^+ SiGe source of the n-channel HT-FET to ground and the N^+ SiGe drain of the p-channel HT-FET to Vdd. To ensure that the p-channel HT-FET fully conducts when gate voltage is zero, we have to do some gate work function engineering to the p-channel characteristics described in Chapter 3. Fig. 4.2 shows the optimized n-channel and p-channel HT-FET transfer characteristics after gate work function engineering of p-channel HT-FET. Here we have used a gate metal work function of 4.45eV for n-channel HT-FETs and 5.62eV for p-channel HT-FETs. Drive currents for n-channel and p-channel HT-FETs are 520μA/μm and 170μA/μm respectively and can be made equal by adjusting the width factor for the p-channel HT-FET.

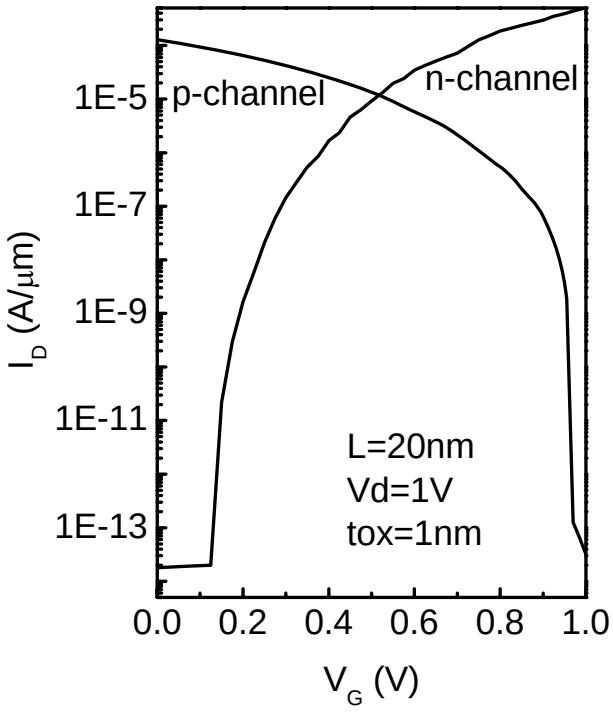


Figure 4.2 Optimized Transfer characteristics for n-channel and p-channel HT-FET after work function engineering

The intent here was to simulate an inverter satisfying ITRS LSTP requirements for 20 nm channel lengths. However the models used, as described in Chapter 1, do not show a match with experimental data for very low values of V_{DS} (Note: all the results discussed in earlier chapters are with maximum V_{DS}). This issue is discussed in appendix A II.

4.2 HT-FET for ultra low power supply applications

High chip power consumption is one of the major hurdles in scaling of logic circuits. Higher power consumption leads to shortened battery life, while higher on chip temperature leads to smaller operating life of chip. This has led to a large and growing interest in ultra low power consumption applications, which might not require high performance. One way to reduce power consumption is to reduce supply voltage. However non-scalability of the subthreshold slope does not allow supply voltage scaling in conventional CMOS logic. In conventional MOSFET technology, ultra low power can be achieved using subthreshold logic, wherein MOSFETs is operated in the subthreshold region (V_{DD}<Vt). Subthreshold logic digital circuits are used in some specific applications which do not need high performance but require extremely low power consumption. Medical equipments such as pace-makers, hearing aids and other applications like wearable wrist watch computation and self powered devices are some examples where subthreshold circuits can be used. However subthreshold logic suffers from the serious drawback of variability. When MOSFETs are operated in subthreshold region, I_D shows strong dependence on process variations and temperature.

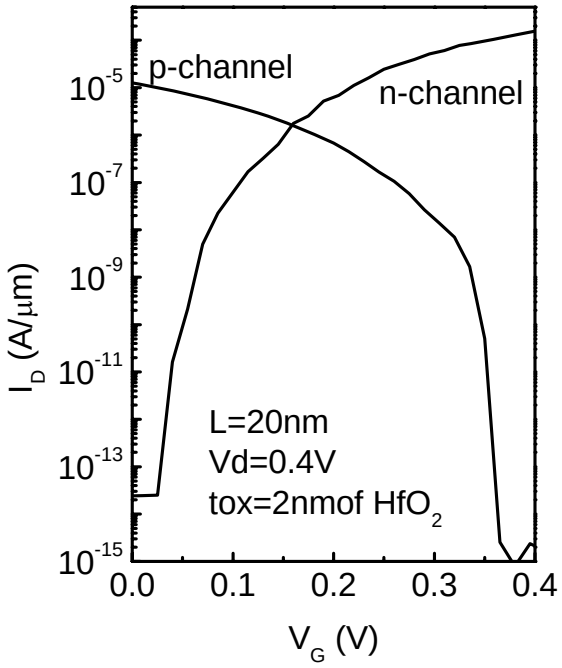


Figure 4.3 Optimized Transfer characteristics for n-channel and p-channel HT-FET for 0.4 V supply voltage inverter

As discussed in earlier chapters HT-FETs show very low subthreshold slope, which can be further reduced by EOT scaling. Low subthreshold slope allows supply voltage scaling for HT-FETs. Unlike subthreshold logic, where ON and OFF conditions are defined in the subthreshold region, for HT-FET ON condition is defined in the region where drain current saturates with the gate voltage ($V_G > Vt$). This reduces the sensitivity of the drain current on process variations. T-FET currents show very small dependence on temperature. Fig. 4.3 shows the transfer characteristics for n-channel and p-channel HT-FETs optimized for L = 20 nm and supply voltage of 0.4 V. Here we have used HfO_2 as a gate dielectric of 2 nm thickness. Ge content is 30% for p-channel and 50% for n-channel HT-FET.

4.3 Summary

In this chapter we studied the possible digital CMOS implementation of HT-FET for LSTP applications and ultra low power supply applications.

Chapter 5
Conclusion and future work

5.1 Conclusion

In this thesis, a basic understanding of the working of T-FETs and an understanding of the electrical parameters is developed with the help of two-dimensional device simulations. For n-channel T-FETs, two different band gap engineering optimization schemes have been studied and we have shown that the heterojunction tunnel FET (HT-FET) gives better performance. Effect of different parameters on HT-FET performance is investigated. We have shown that HT-FETs satisfy ITRS low standby power and high performance logic requirements for 20 nm gate length. The device design space for n-channel HT-FETs is provided with EOT and SiGe bandgap as device design parameters. This device design space indicates that the HT-FET provides freedom of using higher EOT values than ITRS targets. We have also shown that n-channel HT-FETs can be scaled down below 20 nm gate lengths.

In Chapter 3 we proposed a novel device architecture to enhance p-channel performance (p-channel HT-FET). It is seen that p-channel HT-FETs show remarkable improvement in subthreshold slope and ON current. Scalability of this device was studied. It showed that p-channel HT-FETs have characteristics which are almost independent of gate length scaling. Finally in Chapter 4 we studied a CMOS implementation of HT-FET. We have also seen that HT-FETs with their extremely low subthreshold slope can be used for ultra low power applications.

Extremely low subthreshold slope and OFF current, ON currents satisfying ITRS requirements for future technology nodes and scaling independent device characteristics makes the HT-FET the most promising candidate for future technology nodes.

5.2 Future work

This work was aimed at optimizing the n-channel and p-channel T-FET performance. The next step will be investigating circuit applications using these optimized devices. However for circuit applications one needs to calibrate the models for low V_{DS}. As stated in Chapter 4, HT-FETs can be very useful for ultra low power supply applications.

Appendix

I. Two-dimensional device simulations

Choice of device simulator

T-FET device simulation was tried using Sentaurus device simulator. We tried different band to band tunneling models; however none of them show the match with experimental results. Same thing has been experienced by other groups working on tunnel FET. MEDICI device simulator shows good match with experimentally verified results. Typical MEDICI simulation file for generating DC transfer characteristics is given below.

For generating simulation structure

```
COMMENT Specify a rectangular mesh
 MESH    SMOOTH=1
X.MESH x.min=0.0 x.max=0.04 h1=0.001 h2=0.001
X.MESH x.min=0.04 x.max=0.06 h1=0.0006 h2=0.0006
X.MESH x.min=0.06 x.max=0.12 h1=0.001 h2=0.001
Y.MESH  y.min=-0.005 y.max=0.0 h1=0.0003 h2=0.0003
Y.MESH  y.min=0.00 y.max=0.002 h1=0.0003 h2=0.0003
Y.MESH  y.min=0.002 y.max=0.02 h1=0.0005 h2=0.0005
Y.MESH  y.min=0.02 y.max=0.2 h1=0.003 h2=0.003

COMMENT Specify region
region Silicon
region name=gate_oxide SiO2 x.min=0.048 x.max=0.072 y.min=-0.001  y.max=0.0
COMMENT for HT-FET
$region name=source sige x.mole=0.5 x.min=0.0 x.max=0.05 y.min=0.0  y.max=0.02
region name=box oxide x.min=0.0 x.max=0.12 y.min=0.02  y.max=0.06
COMMENT Spacers
region name=sl oxide x.min=0.043 x.max=0.048 y.min=-0.05  y.max=0.0
region name=sr oxide x.min=0.072 x.max=0.077 y.min=-0.05  y.max=0.0


COMMENT Electrode definition
ELECTR  NAME=S x.min=0.0 x.max=0.043 y.min=-0.005 y.max=0.0 void
ELECTR  NAME=D   X.MIN=0.077 X.MAX=0.12 y.min=-0.005 y.max=0.0 void
ELECTR  NAME=G    X.MIN=0.048 X.MAX=0.072  y.min=-0.005 y.max=-0.001 void

COMMENT         Specify doping profiles
PROFILE  P-TYPE N.PEAK=1E20  X.MIN=0.0 X.MAX=0.05 Y.MIN=0.0 Y.MAX=0.02
UNIFORM  OUT.FILE=A
PROFILE  N-TYPE N.PEAK=1E15 X.MIN=0.05 X.MAX=0.07 Y.MIN=0.0 Y.MAX=0.02
UNIFORM
PROFILE  N-TYPE N.PEAK=1E16 X.MIN=0.07 X.MAX=0.12  Y.MIN=0.0 Y.MAX=0.02
UNIFORM
```

```
PLOT.2D GRID TITLE=”Example1_igrid” FILL SCALE

COMMENT Specify physical models to use
models srh btbt bt.model=2   fermi bgn incomple auger

COMMENT Symbolic factorization
SYMB    CARRIERS=2
METHOD  ICCG DAMPED

SOLVE
REGRID  POTEN IGNORE=OXIDE RATIO=.1 MAX=1 SMOOTH=1
+       IN.FILE=A
+       OUT.FILE=mesh_info

COMMENT band diagram for given bias conditions
PLOT.2D GRID TITLE=”regrd” FILL SCALE

COMMENT Solve using the refined grid, save solution for later use
SYMB    CARRIERS=2
SOLVE V(G)=0
SOLVE V(D)=1
SOLVE   OUT.FILE=structure.tiff

COMMENT Impurity profile plots
PLOT.1D DOPING X.START=0.0 X.END=0.15 Y.START=0.0 Y.END=0.0
+       Y.LOG POINTS BOT=1E15 TOP=2E21 COLOR=2
+       TITLE=”ATINTERFACE”
PLOT.1D DOPING X.START=0.0 X.END=0.15 Y.START=0.0 Y.END=0.01
+       Y.LOG POINTS BOT=1E15 TOP=1E20 COLOR=2
+       TITLE=”ImpurityProfile”
PLOT.2D BOUND TITLE=”ImpurityContours” FILL SCALE
CONTOUR DOPING LOG MIN=16      MAX=20  DEL=.5 COLOR=2
CONTOUR DOPING LOG MIN=-16 MAX=-15 DEL=.5 COLOR=1 LINE=2


COMMENT band diagram for given bias conditions
 PLOT.1D X.START=0.02 X.END=0.1 Y.START=0.00001 Y.END=0.00001 COND NEG
TITLE="CB" TOP=1.2 BOT=-2.5 LINE=1 COLOR=1
PLOT.1D X.START=0.02 X.END=0.1 Y.START=0.00001 Y.END=0.00001 VAL UNCH
NEG TOP=1 BOT=-2.5 LINE=1 COLOR=1
```

……

For simulating DC transfer characteristics

```
TITLE MEDICI Simulatiopn file
COMMENT Calculate transfer Characteristics

 COMMENT Read in simulation mesh
 MESH IN.FILE=mesh_info

COMMENT Read in saved solution
```

```
 LOAD IN.FILE=structure.tiff

COMMENT Use Newtons method for the solution
 SYMB NEWTON CARRIERS=2

 COMMENT Setup log file for IV data
 LOG OUT.FILE=idvg.plt

COMMENT Solve for Vds=1 and then ramp gate voltage
 SOLVE V(D)=1
SOLVE V(G)=0.0  ELEC=G  VSTEP=0.015 NSTEP=90

COMMENT Plot Ids vs. Vgs
 PLOT.1D Y.AXIS=I(D) X.AXIS=V(G) Y.LOG COLOR=2
 + TITLE=Gate_Characterist
```

……

Simulation in MEDICI

For solving convergence problem, start with extremely dense meshing at tunneling junction and keep on making it coarse such that simulation converges. Typically with 0.5 nm meshing at tunneling junction simulation converges. If you don't use any gate overlap on source side for n-channel T-FET, you will get notch (kink) in transfer characteristic, so use overlap of 1-2nm to get smooth transfer characteristic. If you are trying new device structures based on band to band tunneling, first make sure that the current you are getting is tunneling current. This can be done by turning OFF the band to band tunneling model.

II. Issues with circuit simulation

When we tried to do circuit simulation using T-FET following things were experienced.

DC analysis does not converge, however transient analysis converges. If you do transient analysis for inverter it shows output characteristics greater than Vdd and less than 0. This is due to MEDICI models do not show good match with experimental data for lower V_{DS}. Calibration of models for low V_{DS} is required.

List of publications

1 Viswanath Nikam, Krishna Bhuwalka and Anil Kottantharayil, “Optimization of n-channel tunnel FET for the sub-22 nm gate length regime”, *accepted for presentation at Device Research Conference, UCSB, CA, June 23-25, 2008.*

2 Vishwanath Nikam, Krishna K. Bhuwalka, Anil Kottantharayil, “Optimization of N- and P-channel Heterojunction Tunnel FETs for sub-22 nm Gate Lengths”, *sumitted to IEEE Transactions on Electron Devices*.

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[2] Daniel Connelly, Carl Faulkner, D. E. Grup, and J. S. Harris, “A New Route to Zero-Barrier Metal Source/Drain MOSFETs,” *IEEE Trans. Electron Devices, vol. 3, no. 1, pp. 98–103, 2004.*

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