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Consistent input/output partitions in acausal systems

Jitesh Jha, Sandeep Kumar and Madhu N. Belur

***Abstract*— Many physical systems do not come with a natural input/output partition of the system variables: we call them *acausal* systems. There are advantages in studying acausal systems using approaches that do not need a partition of the system variables into inputs and outputs. It is also well-acknowledged that viewing subsystems as input/output blocks helps in our understanding of such systems. In view of this, it is helpful to count the number of input/output partitions that one can assign in a 'consistent' way such that acausal systems can be analyzed and simulated using input/output approaches/tools. We introduce a notion of 'consistent' input/output partitioning and provide a count for various networks made up of simple 2-terminal electrical blocks (resistors, inductors and capacitors) with one source. We relate the count for the ladder networks to the Fibonacci series. When the 2-terminal building blocks impose their own natural input/output partition, depending on the properness of the transfer function, then this count reduces suitably. This paper formulates and answers such enumeration questions for various common electrical networks. We use techniques from graph theory: of the type used in KCL/KVL/electrical-networks and matching theory in bipartite graphs. Using these techniques we convert a circuit topology into signal flow graphs (SFG) familiar in systems and control theory.**

Keywords: causal models, consistency, perfect matchings, permanent, bipartite graph

1. Introduction

Many physical complex systems are comprised of simpler subsystems, and the interconnection is not necessarily through an apriori distinction of the shared variables into inputs and outputs amongst the subsystems. A simple example is that of a resistor, where there is no apriori need to classify the variables (voltage and current) into inputs and outputs. We call such systems 'acausal' systems. There are advantages of studying a system without partitioning system variables into inputs and outputs: see the behavioral approach in [Wil97], [PW98] for example. The extensive benefits of the bond-graph way of modelling complex systems is well-known too: see [Kar92] for example. On the other hand, the insight into understanding systems due to viewing them as 'signal-processors', namely, input/output systems is also beyond debate. This paper focusses on obtaining a count on the number of input/output partitions that one can obtain from an acausal system. In order to study this, we propose a notion of 'consistency' of an input/output partitioning of the variables. This notion of consistency formalizes that when studying variables shared across multiple subsystems, each given variable can be an output of only one subsystem, but can be input to several other subsystems. Definition 2.3 below makes this precise. We motivate the need to enlist all consistent input/output partitions in acausal systems below.

The transfer function and state space approach view the system as a 'signal-processor' that takes in an input (the cause), processes the input accordingly, and gives an output (the effect). This type of model is used in *causal* modelling simulators such as Matlab-Simulink, Scilab-Xcos Scicos etc. By 'causal' we mean that the model has blocks with a clear cause-and-effect, i.e. input-and-output demarcation. The cause/input goes into the block in a causal model and the effects/outputs come out of the block. In a causal modelling paradigm one effect/output cannot come from two different independent blocks.

A causal approach is both elegant and explicitly described and as a result such an approach is easy to understand and has helped in development of control theory. We can formulate transfer function of the dynamical system from such a model pretty easily, which can be further used in system analysis using Bode plot, filter designing and controller design.

I/O approach, although very useful, is a very restrictive one. Most physical systems cannot be reduced into such form as they do not have a clear input or output separation and the variable might be shared. Such systems do not have a preferred direction of signal flow. The behavioral approach to the study of dynamical systems builds on this and see [Wil97], [PW98] for more discussion on this. In this paper we find all the possible ways in which signal flows and convert an acausal model to a causal form. We call these different possible directions as consistent assignments. When simulating/solving a network, the flexibility of choosing the input/output partition from any of the consistent assignments can be used, for example, to get faster solutions and/or more accurate solutions, in particular when certain i/o partitions result in ill-conditioned problems.

The number of consistent i/o assignments possible for a system is the number of ways that the network can be solved for the system-variables using the system equations. For a simple electrical network we have different ways to find the potential and the currents entering a node for each node. One uses mesh (loop) analysis, nodal analysis or KCL-KVL directly to solve the network. The choice of method to solve gives one the number of variables the system has, for example, mesh analysis would have mesh currents as variables which may reduce the number of variables compared to KCL-KVL.

In order to develop a model for such a network which defines cause and effect for each device (resistance, capacitance etc.) one needs the device equation, i.e. the relation between the current flowing through the device and the voltage across it. For two terminal devices such as resistor, the relations are $V_R = I_R R$, for capacitor

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$I_C = C\frac{d}{dt}V_C$, for inductor $V_L = L\frac{d}{dt}I_L$.

For a resistance device, the voltage across can be cause, and the current flowing through it is the effect or vice-versa: one can assign whichever causal relationship as required. However, when the same device is part of a larger network this freedom is not always there since there could be an inconsistent assignment elsewhere where one variable ends up being an output of two or more subsystems. Further for capacitive and inductive networks, we do not have a choice as we had in purely resistance networks, capacitors and inductors have their own natural causal direction. A capacitor transfer function is proper when the current is input and voltage is output, inductor transfer function is proper when the voltage is input and current is output. In this paper we discuss electrical networks but the same results hold for mechanical systems too.

The following types of graphs and the relevant graph theory play a key role in this paper.

- The circuit topology, allowing KCL/KVL related graph theoretic techniques.
- Bipartite graph (equation and variables separated), allowing matching theory techniques.
- Undirected bipartite graph (signal flow version) as shown in Figure 5 for example.
- Consistent directed graph (signal flow graph (SFG)) as shown in Figure 6, bridging matching theory and signal digraph literature in control theory.

Further, many of the graphs use the following symbols for easier separation of nodes into variables and equations, with equation nodes marked as below.

This paper is organized as follows. Section 2 contains preliminaries and introduces the nodes and edge terminology for the bipartite graph representation of system. Terms such as consistent directed graph, consistent number and rules for consistency are also defined in this section. Section 3 contains our main results where we prove that the number of consistent assignments of input/output partition for a resistance ladder network is the Fibonacci series (using the number of rungs in the index). This is proved by induction and also pursued in a few examples. Section 4 studies how the number of consistent assignments falls when one of the resistors in the ladder is replaced by a capacitor. Section 5 contains concluding remarks and directions for further work.

2. Preliminaries and 'consistency'

This section contains some graph theoretic preliminaries and we introduce the notion of a *consistent* input/output partition of variables.

A. Nodes and edges

We use two different types of nodes.

- **Equation nodes:**, which can be algebraic equation, differential/integral equation with multiple variables,
- **Variable nodes:**, which as the name suggests are variables of the system.

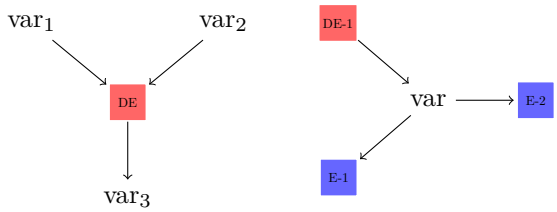

Figure 1: Variable and equation nodes

No two nodes of the same type are connected directly to each other, so we have a bipartite graph with the node set as equation nodes and variable nodes.

Definition 2.1: A graph is called bipartite if its set of vertices can be written as a disjoint union of two sets, say U and V, such that no two graph vertices within the same set are adjacent. We use $G(U,V,E)$ to denote the bipartite graph with E being the set of edges. In this paper, the bipartite graph is constructed as follows. U is the set of equation nodes, V is the set of variable node and E is the set of edges between these two sets of nodes: edge e in E between u_i and v_j means that the variable v_j occurs in the equation u_i.

One such bipartite graph for resistance network can be seen in Figure 4. In our work we show a device equation node as a rectangular/diamond block and variable node as a point as shown in figure 1.

Equation nodes are of two types,

- **Device equation (DE)**: This is the relation between the variables of a *device*: cause and effect could be defined for each device.For a directed graph, when a variable node has an edge directed towards a device equation node then the variable is cause for that device and variable node that has an edge directed towards it from a device equation node are effect of that device.
- **Correspondence equation (CE)**: This is the relation between variables due to the *interconnection* of devices. In electrical networks, these are nodal or mesh/loop equations and they comprise of circuit topology equations.

This brings us to the definition of a consistent input/output partition: this captures the requirement that when the system is solvable then in any consistent i/o partition each system variable is an output of only one subsystem and can be input to many subsystems. This notion is defined using the bipartite graph.

An assignment of edges in a bipartite graph is called *consistent* if:

1) Only one edge is directed *into* a *variable* node.
2) Only one edge is directed *out of* an *equation* node.

This can be seen in Figure 1 where device equation node is shown in red and correspondence equation node is shown in blue color. It is not hard to see that when the bipartite graph has a perfect matching, there is a one-to-one correspondence between perfect matchings and consistent assignments.

Definition 2.2: **Source nodes** are variable nodes which are not dependent on the system and therefore all the edges from such a node are directed away from the source node.

Definition 2.3: **Consistent directed graph** is a directed bipartite graph $G(U,V,E)$ where U is the set of equation nodes, V is the set of variable nodes and V_s is the set of source node, such that $|U| = |V| - |V_s|$. Assignment of arrows of each edge is called **consistent** if the following conditions are satisfied.

a) For each variable node, $v \in V$, there is exactly one incoming edge.
b) For each equation node, $u \in U$, there is exactly one outgoing edge.

In this paper we consider $|V_s| = 1$, the result can be pursued for multiple source nodes. In Definition 2.3 it is also possible to consider the source also in the set of equation nodes U and this gives $|U| = |V|$, the results discussed in the following sections will be unaffected.

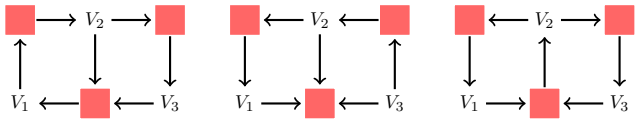

Figure 2: Consistent directed graph for ladder bipartite graph, there are three possible direction assignments that are consistent with the rules. Consistent number: 3

Definition 2.4: **Consistent number** C_N of a dynamical system is the total number of consistent directed graph $G(U,V,E)$ that can be constructed for a system.

Figure 2 shows an example for consistent directed graph for a ladder type bipartite graph. By assigning direction as per the rules we see that 3 such consistent graphs can be drawn, thus the consistent number for such a graph is $C_N = 3$.

3. Resistance ladder network

First we discuss the case of purely resistive circuits with single voltage source and $2n$ resistors. In purely resistive ladder network as shown in Figure 3 we are free to assign the direction to the device as per the rule discussed in Section 2.

Example 3.1: We consider a resistance ladder circuit with 3-rungs with a voltage source and construct its consistent directed graph and compute its consistent number C_N.

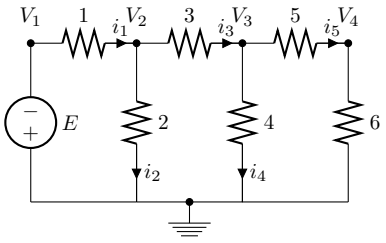

Figure 3: Resistance ladder 3-rung

Figure 3 is the resistance ladder with 3-rungs. We perform **nodal analysis** to solve the network. There are four node voltages V_1, V_2, V_3, V_4 and five current variables i_1, i_2, i_3, i_4, i_5 flowing through each resistor. In order to solve for this network and get value of each variable we need eight equations for nine variables, where V_1 is source. There are six resistors (devices) which gives us six device equations.

$$V_1 - V_2 = i_1 R_1 \quad \text{(DE-1)} \qquad V_2 = i_2 R_2 \quad \text{(DE-2)}$$
$$V_2 - V_3 = i_3 R_3 \quad \text{(DE-3)} \qquad V_3 = i_4 R_4 \quad \text{(DE-4)}$$
$$V_3 - V_4 = i_5 R_5 \quad \text{(DE-5)} \qquad V_4 = i_5 R_6 \quad \text{(DE-6)}$$

KCL equations: $i_1 = i_2 + i_3$ (KCL-1) and $i_3 = i_4 + i_5$ (KCL-2), source variable/equation $V_1 = E$, and node equations:

$$\frac{V_2 - V_1}{R_1} + \frac{V_2 - V_3}{R_3} + \frac{V_2}{R_2} = 0 \qquad \text{(Node-2)}$$
$$\frac{V_3 - V_2}{R_3} + \frac{V_3 - V_4}{R_5} + \frac{V_3}{R_4} = 0 \qquad \text{(Node-3)}$$

The corresponding separated bipartite graph for this network is as in Figure 4.

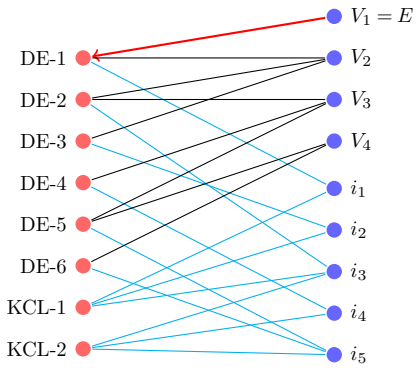

Figure 4: Separated bipartite graph (equation-variable separated)

One can solve the network for all its variable using the equations above. A bipartite graph, Figure 4, is made with DE-1 to DE-6 and KCL-1, KCL-2 on one side as equation nodes and the nine variable nodes on the other side.

Device equation nodes have edges connecting variable nodes of current and voltage type for each device, whereas correspondence equation node have edges connected to variable nodes of either only currents or only voltages but not both.

By restructuring the bipartite graph in Figure 4, we get the *ladder network* in Figure 5. In both graphs, variable node V_1 is a source node and the edge is directed away from the node.

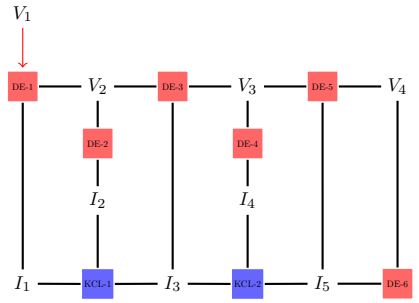

Figure 5: Undirected bipartite ladder graph

A. Assigning direction

We use this example to show how to assign direction according to the rules specified in Definition 2.3 and shown in Figure 1. Start from the source node, i.e. V_1

in Figure 5, assign an arbitrary direction to the edges connected to node DE-1. If we take the direction as shown in Figure 6, i.e. $(I_1) \longrightarrow$ (DE-1) $\longrightarrow (V_2)$, then this orientation sets I_1 as cause and V_2 as the effect for device-1 (R_1). As V_2 variable is an effect of DE-1, the only possible direction for other edges connected to V_2 is away from V_2:
(DE-3) $\longleftarrow (V_2) \longrightarrow$ (DE-2). This is shown in Figure 6.

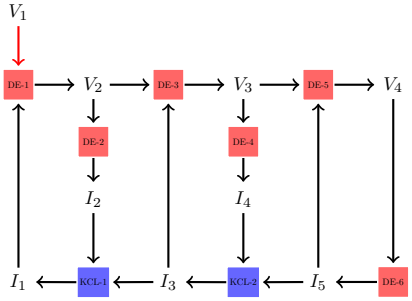

Figure 6: Consistent directed graph (signal flow graph (SFG)) for Example. 3.1: nodal analysis

Then assign direction to edge connected to I_1 and so on. Keep doing until all the edges have directions assigned to them and they follow the rules specified in Definition 2.3. One such complete graph is shown in Figure 6, it is consistent with the rules hence is called a *consistent directed graph*.

Any variable node other than the source has a directed path connected to every other node. The variable node V_3 is connected to every other variable node and there is a directed cycle loops back to itself, this gives a feedback path for every node. The total number of such consistent directed graphs possible for a ladder network with 3-rungs is 13, i.e. *consistent number* $C_N = 13$.

B. Mesh analysis

Example 3.1 (contd) 1: Another way to solve the same network is by mesh/loop analysis. Consider the circuit shown in Figure 7, there are 3 current variable and 4 voltage variables.

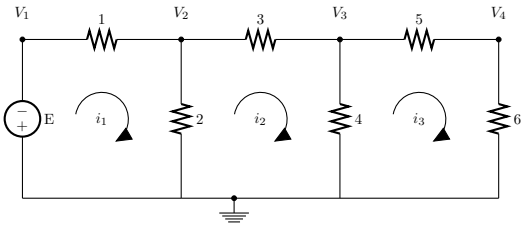

Figure 7: Resistance ladder 3-rung: mesh analysis

The consistent directed graph for mesh analysis is shown in Figure 8, the structure of graph is similar to that of Figure 6 and the consistent number is also the same: $C_N = 13$.

C. Consistent number

The symmetric structure in the undirected bipartite graphs corresponding to the ladder networks play a key role in our results. Notice from Figure 9a, for example, that each rung in the ladder network adds 2 resistors into the network.

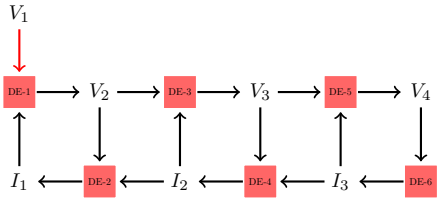

Figure 8: Consistent directed graph for mesh analysis of 3-rung resistance ladder of Example 3.1

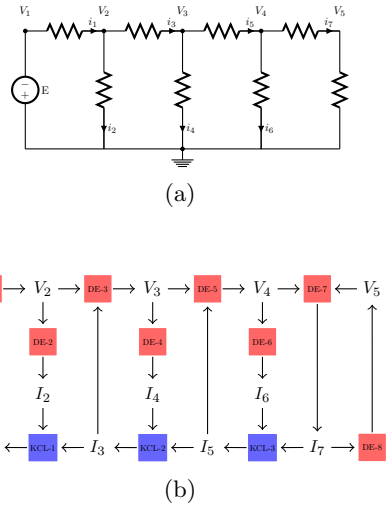

Figure 9: (a) Resistance ladder 4-rung, (b) Consistent directed graph 4-Rung

Figure 9a and Figure 10a show resistance ladder for 3 and 4 rungs, while Figure 9b and Figure 10b show the corresponding directed consistent graph. The consistent number (C_N) is 34 for Figure 9b and 89 for Figure 10b. We see from the structure in the graphs that each addition of a rung into the ladder network adds 2 rungs in the graph for nodal analysis and mesh analysis graph. This brings us to the main result of this paper: a count on the number of input/output consistent assignments in a ladder network and the link with Fibonacci series.

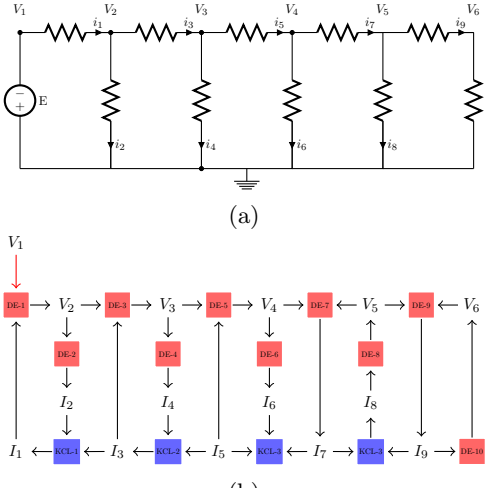

Figure 10: (a) Resistance ladder 5-rung, (b) Directed consistent graph 5-Rung

Theorem 3.2: For a resistance ladder network with 1 source, m inner-loops and $2m$ resistors.

a) The consistent number C_N is same for both **nodal analysis** and **mesh analysis**.
b) Let F_m be the Fibonacci series, with $F_1 := 1$, $F_2 := 1$ and $F_{m+1} := F_m + F_{m-1}$. Then C_N, the number of consistent directed bipartite graphs for resistance ladder, satisfies

$$\boxed{C_N(m) = F_{2m+1}}$$

Of course, Statement (a) of the theorem is not unexpected. We prove both claims below, in which claim (b) is proved by induction on the number of rungs.

Proof of Theorem 3.2: Notice that although the number of variables are different in mesh analysis and nodal analysis, the structure of the graph is same. Figures 6 and 8 reveal a general structure between nodal and mesh analysis that the extra nodes are always each of degree 2 and do not change the consistent number. Hence each degree 2 node with its two adjacent edges can be all replaced by one edge making the directed graphs the same. Though this proof used a specific example's figure, this argument helps deduce claim (a).

We prove claim (b) of the theorem by induction. We use mesh analysis as the number of variables in mesh analysis is same as the number of devices. We denote the graph as a matrix with rows denoting the device equations and columns for variables, for example we can denote the bipartite graph for 3-rung ladder network shown in figure 7 by matrix A.

$$A = \begin{array}{c} \\ DE_1 \\ DE_2 \\ DE_3 \\ DE_4 \\ DE_5 \\ DE_6 \end{array} \begin{array}{c} \begin{array}{cccccc} I_1 & V_2 & I_2 & V_3 & I_3 & V_4 \end{array} \\ \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix} \end{array}$$

The consistent number for the ladder network is equal to the permanent of the matrix A.

$$C_N = Permanent(A) = 13$$

We can see that there is a pattern in the matrix A as rungs are added in a ladder network. For each rung added 2 nos. of devices are added (2 DE and 2 Variable). The individual matrices for each rung is as denoted by partitions.

$$A = \left[\begin{array}{cc|cc|cc|cc} 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ \hline 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ \hline 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \end{array}\right]$$

A is a tridiagonal matrix with order $2m$, where m is the number of rungs in the resistance ladder network with $2m$ resistors. The tridiagonal matrices are well studied and permanent of such matrix can be given by the Fibonacci numbers [JP92]. Permanent of order k tridiagonal matrix A is given by:

$$Permanent(A_k) = F_{k+1}$$

Therefore, the consistent number of $m-$rung resistance ladder network with $2m-$ resistors can be given as:

$$C_N(m) = Permanent(A_{2m}) = F_{2m+1} \qquad \square$$

The proof is illustrated in Figure 11. The following section considers the case when one resistor is replaced by a capacitor, i.e. a nonstatic device which brings a natural i/o partition with it. This expectedly reduces the total number of consistent i/o partitions.

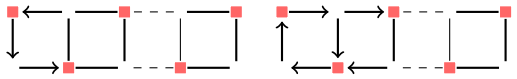

Figure 11: For $k+1$ loops in ladder graph, when the right most rung is directed anticlockwise we have k undirected loops with $C_N = F_{k+2}$, when it is clockwise we have $k-1$ undirected loops with $C_N = F_{k+1}$

4. Resistance ladders with one capacitor

In purely resistance circuits we were able to assign directions with ample choice: this section studies the case with one capacitor in a resistance ladder network.

Example 4.1: Resistance ladder with capacitance

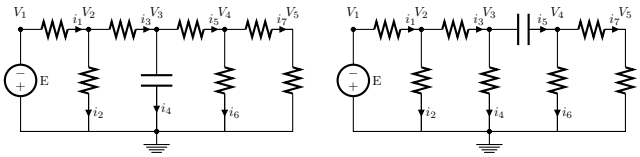

Figure 12: (a) A 5-rung resistance ladder with capacitor in parallel, (b) the capacitor in series.

In the case of a capacitor, by imposing an i/o partition such that the transfer function is proper, we obtain that the current variable is an input and the voltage is the output. Capacitive device node is depicted by a red diamond node as shown in Figure 13.

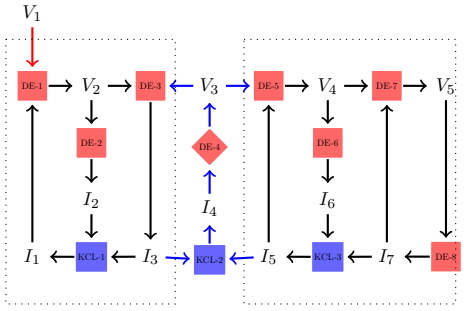

Figure 13: Directed consistent graph for Example 4.1: the capacitor divides the graph into two parts. The left block has $C_N = F_4 = 3$ and right block has $C_N = F_5 = 5$, for the complete graph $C_N = 3 \times 5 = 15$

We summarize the steps involved in assigning directions in the presence of devices like capacitors which have a natural i/o partition.

Steps to assign direction in presence of nonstatic devices (like capacitors):

a) Start at the source end, i.e. V_1 in Figure 13, till we reach the first nonstatic device.
b) Assign the natural direction of cause and effect to each such device.
d) Assign direction to rest of the devices.

One such consistent directed graph is shown in Figure 13.

Adding a capacitor in parallel divides the network into two parts and consistent number is the product of consistent number of the two parts. For circuit in Figure 13, the right part has 4 rungs with consistent number $C_N = F_5 = 5$ the left part has 3 rungs with consistent number $C_N = F_4 = 3$. Then the consistent number for complete graph is $C_N = 3 \times 5 = 15$.

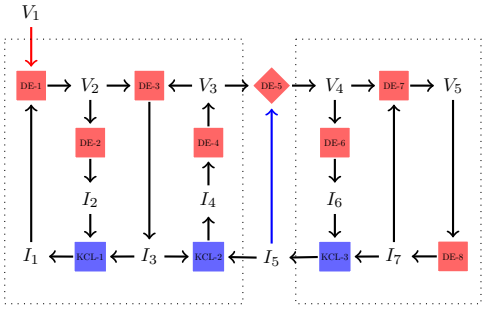

Figure 14: Directed consistent graph Example 4.1, capacitor in series removes one rung. The left block has $C_N = F_5 = 5$ and right block has $C_N = F_4 = 3$, for the complete graph $C_N = F_4 \times F_4 + F_5 \times F_3 = 19$, where F_n is Fibonacci series.

Adding a capacitor in series removes a rung from the graph. For a n rung ladder graph consistent number is $C_N = F_{n+1}$, for capacitor in series with n rungs in right and m rung in left then the consistent number of complete graph is $C_N = (F_n \times F_{m+1}) + (F_{n+1} \times F_m)$. For circuit in Figure 14, the left part has 4 rungs with consistent number $C_N = F_5 = 5$ the right part has 3 rungs with consistent number $C_N = F_4 = 3$. Then for the complete graph $C_N = F_4 \times F_4 + F_5 \times F_3 = 19$.

5. Concluding remarks and future directions

In this paper we introduced the notion of consistent partitioning of shared system variables into inputs and outputs and also obtained explicit formulae for the consistent number (C_N) count. We showed that for the resistor ladder network with a voltage source, the consistent number is exactly the Fibonacci series. Resistors being acausal in the full sense, i.e. no natural i/o restriction due to a static relation between the system relation, causes a high C_N. When some resistors are replaced by capacitors or inductors, the count decreases and we considered some examples. Due to space constraints, we skipped proving that for the case of an LC network, the consistent number is 1, i.e. the consistent i/o partition is unique. While this is expected, it is interesting to obtain this using bipartite graph matching techniques.

The methods used in our work crucially used the graph topology of the circuit, and proceeded to construct an equation/variable undirected bipartite graph, and then an undirected signal-flow version of bipartite graph, and finally the consistent directed graph (closest to the signal-flow digraph studied in the theory of systems and control). The equations comprised of the KCL/KVL 'correspondence' equations and the device equations, while the variables comprised of the voltage across each device and the current through each device. Thus our analysis holds for 2-terminal mechanical/flow devices too, and perhaps more generally to devices whose variables come in pairs of the type: through/flow type variable and an across/potential-drop type of variable. A matter of future research is to analyze the case of 3-terminal devices like transistors and higher terminal devices (like op-amps and transformers). A topological model of such a network has been studied in [CDK87], for example.

An important independent area of research is the notion of 'permanent' of a square matrix: this notion is related closely to that of perfect matchings in a bipartite graph. Exploring further links between this area and that of consistency number proposed in Definition 2.2 is important for further research.

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