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Low-Voltage Current-Mode Analog Cells

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Abstract

This seminar report discusses the low-voltage current-mode analog circuits and their various aspects. The need of high speed, high performance, low power circuits because of the advent of the portable electronic and mobile communication systems and difficulties faced in achieving that in today's scenario are presented. Current mode circuits are the best suited candidates for the above. Their advantages are discussed here and a comparison with the conventional voltage mode circuits has been presented. The principle and the implementation of the most common current mode circuits i.e. the current conveyors, has been described. The basic device level techniques also play important role in the design of smarter and efficient circuits. Some of those techniques have also been discussed here. For illustration of these techniques, low power V-I converter using current mirrors and a low-voltage power efficient operational amplifier cell topology is presented.

1 Introduction

With the advent of the portable electronic and mobile communication system low-voltage and low-power mixed mode circuit design has gained importance. For the operation of such systems like hearing aids, implantable cardiac pacemakers, cell-phones and hand held multimedia terminals etc. battery is the main source of power. They require low power dissipation so as to have reasonable battery life and weight. Battery adds volume and weight as so there is search for the alternatives and the alternatives are solar power, fuel cells etc. But the problem is with the voltage levels of these sources. The voltage of a single solar cell is about 0.5 V and integrated circuits require much higher voltages for their operation [1]. Obtaining higher voltages on chip by voltage multiplication which is nothing but DC-DC conversion is noisy and not compatible with the analog circuits. It can be done either using inductors or without using inductors [2]. Also in analog design the issue of Power Supply Rejection Ratio should be taken care of [3].

As the feature size of CMOS processes reduces, the supply voltage has to be reduced for the reduction of power dissipation per cell. Supply voltage reduction guarantee the reliability of devices as the lower electrical fields inside layers of a MOSFET produces less risk to the thinner oxides, which results from device scaling. However, the reduction in supply voltage leads to degraded circuit performance in terms of available bandwidth and voltage swing. Scaling down the threshold voltage of the MOSFETs reduces the performance loss (degraded bandwidth, low voltage swing etc.) somewhat but it has its own disadvantages i.e. the increase in the static power dissipation. The performance of digital circuits is improved by scaling but the analog cells, benefit marginally because minimum size transistors cannot be used due to noise and offset requirements.

In today's design techniques the aim is to achieve high speed, and high integration on chip with a large dynamic range. One of the factors, which affect these parameters, is power dissipation in the circuit. There are three major sources of power dissipation [4].

- Dynamic power consumption caused by charging and discharging of (usually parasitic) capacitance;
- Static power consumption due to non-zero current of MOSFETs in OFF state in digital circuits or the biasing current in the analog circuits.
- Short-circuit power consumption due to the current flowing during the lapse of time when both PMOS and NMOS transistors are in the on state.

The dynamic power dissipation has been increasing quickly along with the progress in the CMOS processing technology, which raises the ambient temperature and degrades the device performance and the circuit performance is less stable. Lowering power supply voltage is the most efficient method in reducing power dissipation of a chip. The dynamic power dissipation is given by

$$P = \alpha \, . \, C_L \, . \, V^2_{DD} \, . \, f_{CLK}, \tag{1}$$

where α is the probability of the logic gate output to change from 0 to1 and hence its value ranges from 0 to 1 and is called the switching activity.

C_L is the load capacitance, and

f_{CLK} is the clock frequency.

Due to increased demands on the system performance, the clock frequency increases. Power dissipation can be reduced by reducing the switching activity and the output load capacitance. The former can be reduced via proper circuit and system designs and the latter can be reduced by an advanced CMOS technology or by reducing device dimensions. But the reduction in power dissipation is most effective when V_{DD} is lowered.

The static power consumption depends on the OFF state current (I_{off}) and equals

$$P_{static} = I_{off} \, V_{DD} \tag{2}$$

For conventional CMOS technologies with high threshold voltages, this contribution is too low. However, in analog circuits it is the main contributor for power dissipation as the devices are biased permanently in saturation modes.

During switching in CMOS, both NMOS and PMOS are simultaneously active for a short period of time and an instantaneous short-circuit current (I_{SC}) flows from the power supply directly to ground. The power consumption due to I_{SC} is given by

$$P_{SC} = I_{SC} \, V_{DD} \tag{3}$$

This term can be neglected if the signals have short rise and fall times as compared to duration of the signal. Thus, the total power consumption is given as

$$P_{total} \approx N C_{eq} \, V^2_{DD} + I_{off} \, V_{DD} \tag{4}$$

Lowering power dissipation is also important for a high-performance system. Increase in power dissipation, increases the ambient temperature which worsens the electro-migration reliability problems. The low voltage and low power operation complicates the design of the circuits. Simple topologies requiring less number of MOSFETs can give better performance due to lower device and stray capacitances [5].

For the low voltage high performance analog circuit design current mode design technique, which offer voltage independent high bandwidth analog circuit, is a good alternative. In current mode design the designer is more concerned with current levels for the operation of the circuits. The voltage levels at various nodes are immaterial [1].

All conventional analog circuits are voltage mode circuits (VMCs) where the circuit performance is determined in terms of voltage levels at various nodes including the input and the output nodes example operational amplifier. But all these circuits suffer from the following disadvantages

- output voltage can not change instantly when there is a sudden change in the input voltage due to stray and other circuit capacitances.
- bandwidth of the op amp based circuits is usually low because of finite unity gain bandwidth.
- slew rate is dependent on the time constants associated with the circuit.
- circuits do not have high voltage swings.
- require higher supply voltages for better SNR.

Therefore, VMCs are not suitable for use in high frequency applications.

In current mode circuits (CMCs) the complete circuit response is determined by the currents and the input/output signals are primarily currents. The voltage levels are irrelevant in determining the circuit performance. The nodes inside CMCs are low impedance nodes, where the resultant voltage swings are also small. The low impedance transforms them into low time constant circuits and the bandwidth is quite high. The slew rate is also high if the rate of output changing is high. CMCs have simple architecture and their operations do not depend on the supply voltages. The analog circuits should have rail-to-rail input and output voltage swing capability for high SNR, which can be received using the CMCs. Most common CMC structure is current conveyor (CC).

2 Current Conveyors

The current conveyors have been classified in three classes viz, CCI, CCII, and CCIII. All the three have similar structures but their characteristics are different. Current conveyors are commercially available (e.g., AD 844 from Analog Devices) [1].

Fig. 1 [7] shows the black box representation of the current conveyor

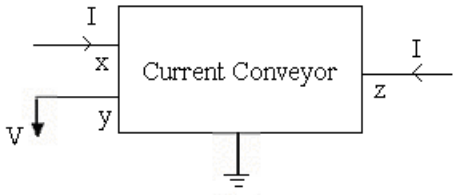

Fig. 1 Black box representation of the basic current conveyor.

Port x is a hybrid port and functions as input port for current signals and output port for voltage signals at the same time. Port y is a voltage input port and port z is a current output port, which can either sink or source current equal to the current injected into port x. If port y is connected to a potential v an equal voltage will appear on the port x and if a current I is forced through port x, an equal current will flow through port y (depending upon the nature of the CC, see Eqn. 5). The same current I, the sign of which is governed by the current transfer characteristics (see Eqn 5), is also conveyed and supplied through output port z at a high impedance level in the manner of a current source and so the output current remains unaffected

by the load. The potential at port x is independent of the current I forced into x and the current I through port y is independent of the voltage v applied to y. Thus the device exhibits a virtual short circuit input characteristic at port x and a dual virtual open-circuit input characteristic at port y [7].

The relation between the currents and voltages at various ports can be summarized as

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & a & 0 \\ 1 & 0 & 0 \\ 0 & b & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad (5)$$

where $i_x(v_x)$, $i_y(v_y)$, and $i_z(v_y)$ are the currents(voltages) at ports x, y, and z respectively. b characterizes their current transfer from x to z and a is related to the nature of the conveyor.

- b > 0, the circuit is a positive transfer conveyor (CC+)
- b < 0, the circuit is a negative transfer conveyor(CC-).
- a = 1, the circuit is a first generation current conveyor (CCI)
- a = 0, the circuit is a second generation current conveyor (CCII)
- a = -1, the circuit is a third generation current conveyor (CCIII) [6].

It is desired that a CC should have large bandwidth and consume low quiescent power. Ideally a CC should have

- Infinite input impedance (R_{in}) at port y
- Zero input impedance (R_x) at port x for current inputs
- Infinite output impedance (R_{out}) at port z
- Unity voltage transfer gains between port y and x
- Unity current transfer gain between port x and z
- Infinite bandwidth

2.1 First generation current conveyors (CCI)

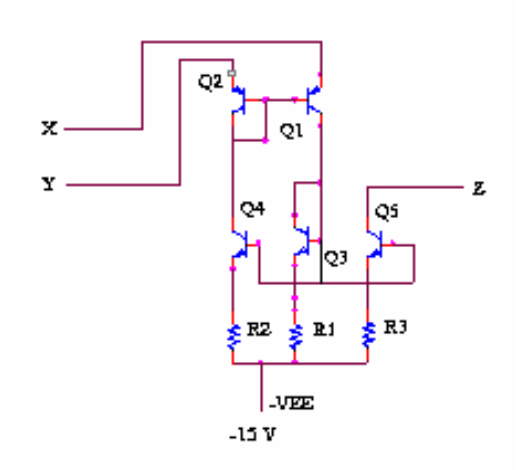

Fig. 2 Implementation of the CCI using BJT

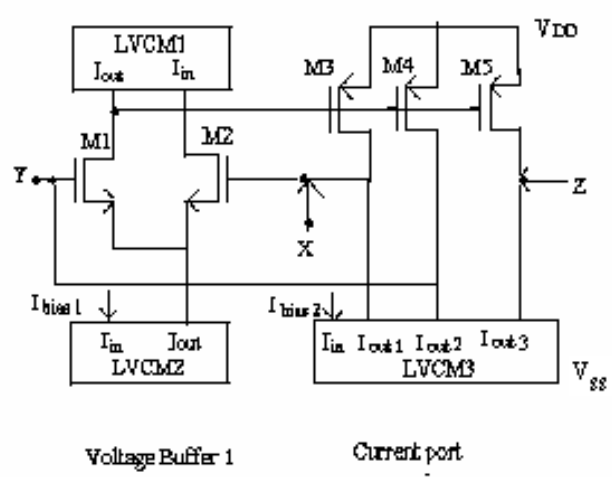

Fig. 3 Implementation of CCI using MOSFET

Fig. 2 [7] is a circuit implementation of the current conveyor. If we assume that all the correspondingly transistors and resistors are matched and that all transistors have high common-base current gain (both dc and incremental), then all transistors carry the same current, I. Thus, it follows that x and y tracks each other in potential. If the linear operation of the transistors is considered throughout the operating range then the operation is independent of the absolute values of resistors and supply voltage.

Another implementation for CCI using MOSFETs is shown is Fig. 3 [1]. The input section is the voltage buffer1 [1] with an additional current port. The input voltage (V_y) applied at port Y gets transferred to port X by the voltage buffer. The current transfer takes place by the action of low voltage current mirror (LVCM). The output and input swings of the structures are near rail-to-rail.

In CCI the current is duplicated with unity gain at high impedance on output Z and therefore this circuit is useful when it is desired to measure the current coming from very low impedances. The transfer characteristic between ports x and z is that of a current-controlled current source with several special applications in instrumentation and communication systems [7].

2.2 Second generation current conveyor (CCII)

Fig.4 [8] shows the implementation for the CCII current conveyor. Transistors M_2, M_3, M_4, and M_6 form the current mirror so as to have equal current in the first (one containing the input Y) and the second branch. M_1 form the source follower for the voltage input. M3, M5, and M7 form the cascode current mirror to transfer the current i_x flowing into the node X to the node Z.

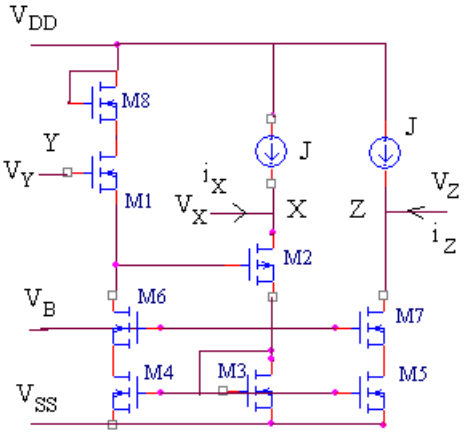

Fig. 4 Circuit diagram for CCII implementation

Consider that the transistors M_3, M_4, and M_5 are matched. So we can see that

$$i_z = i_x \tag{6}$$

The same current also flows through M_1. Therefore,

$$g_{m1}(v_y - v_s) = g_{m2}(v_x - v_s) = -v_x/R_x \tag{7}$$

where g_{m1} and g_{m2} are transconductances of M_1 and M_2, respectively, v_s is the source voltage of M_1, and R_x is the resistor connected between the node X and ground. From eqn. 7

$$v_x = (g_{m1}g_{m2}R_x v_y)/(g_{m1} - g_{m2} + (g_{m1}g_{m2}R_x)) \quad (8)$$

is obtained.
Now $v_x = v_y$ if $g_{m1} = g_{m2}$ or $g_{m1}g_{m2}R_x >> g_{m1} - g_{m2}$. No current flows through the node Y, and $i_y = 0$. The output impedance at the node is so high, due to the cascode current mirror, that i_z is not affected by the load. For the direction of the current i_z shown in the Fig. 4 we get CCII+ and if the direction is reversed we get CCII- implementation. CCII is a device which is useful for the implementation of continuous-time analog circuits in both linear and non-linear applications.

2.3 Third generation current conveyor (CCIII)

The circuit for the implementation of CCIII is shown in Fig. 5 [1]. The implementation consists of a CCII circuit and an inverting current mirror (ICM). The output of the ICM is fed back to port Y. The performance of the CCIII is similar to the parent CCII.

This conveyor is useful to take out the current flowing through a floating branch of a circuit. It may also be used with advantage as the input cell of probes and current measuring devices [6]. CCIII can also be implemented using two CCII [6]. Considered between ports X and Y, the CCIII acts as a positive-impedance converter having unity voltage and current gains.

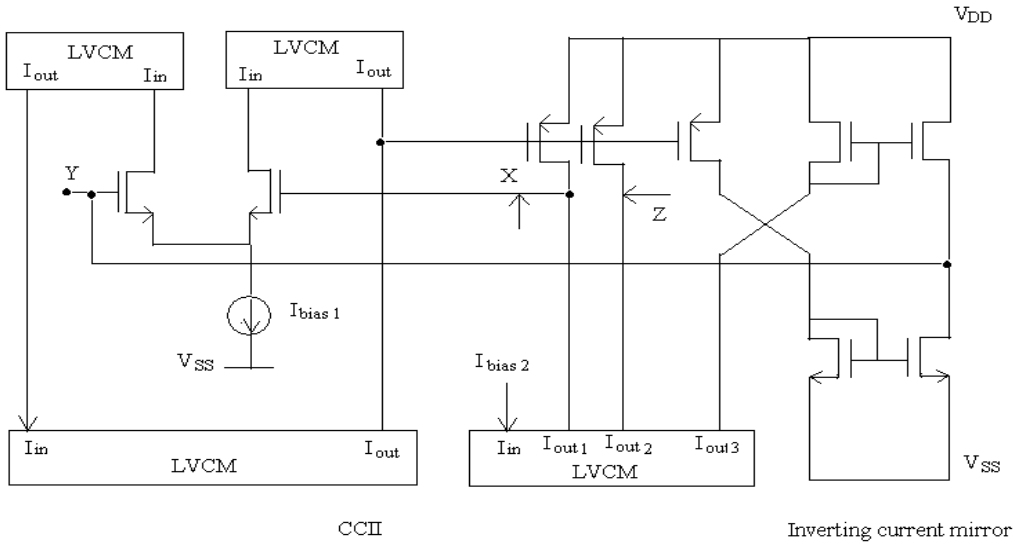

Fig. 5 Circuit Diagram for CCIII

3 Current-mode low-voltage design

In any current mode analog circuit, a current mirror (CM) and voltage buffers (VB) are integral parts and their properties affect the operation of low voltage circuits. The low voltage current mirrors (LVCMs) provide the high voltage swing capability at the output terminal, but they do not have high input swing capability. They require a margin of at least one threshold

voltage ($V_T \approx 0.8$) for proper operation, which is quite large for a supply voltage of 1.0 V. The VB must provide rail-to-rail output voltage swings with low output impedance.

At low voltage, the main constraints faced are the device noise level and V_T. Reduction in V_T is dependent on the device technology. Higher V_T gives better noise immunity and the lower V_T reduces the noise margin to result in poor SNR and result in very complex circuits. So there is a need for simpler, smarter and efficient circuits. Many new design techniques for the low voltage analog circuits are available viz., MOSFETs operation in (a) sub-threshold region, (b) bulk-driven transistors, (c) self-cascode structures, (d) floating gate approach and (e) level shifter techniques.

3.1 Sub-threshold technique

The drain characteristics for MOSFET are given by

$$I_{DS} = \beta[(V_{GS} - V_T) - (V_{DS} / 2)]V_{DS} \qquad V_{DS} \geq V_T \qquad (9)$$

$$I_{DS} = 0 \qquad V_{DS} < V_T \qquad (10)$$

where $\beta = \mu C_{OX} (W/L)$ and is called the trans-conductance parameter.

This relation exists for the small values (both positive and negative) of V_{DS}, which correspond to ohmic region of operation. The drain current is assumed to be zero for $V_{GS} < V_T$ and nonzero for $V_{GS} \geq V_T$. In a physical device, such an abrupt change does not occur. The drain current (I_{DS}) is, however, much smaller for $V_{GS} < V_T$ than for $V_{GS} \geq V_T$. I_{DS} is attributed to diffusion in the region ($V_{GS} < V_T$, known as the sub-threshold region) and the device is said to operate in "week inversion". In sub-threshold region I_{DS} is given by

$$I_{DS} = (2K'W)/L\ [nkT/qe]^2 \exp[q(V_{GS} - V_{TN})/\eta kT] \qquad (11)$$

where η lies between 1.2 and 2. Parameters q, k, V_{TN} and T represent the electronic charge, Boltzmann constant, threshold voltage of N channel MOSFET and temperature, respectively. Low voltage circuits in biomedical engineering and mobile communication etc. require that current levels be extremely small and supply voltage should also be low.

In sub-threshold region, MOSFETs have low saturation voltages ($\approx$ 100 mV). It gives larger voltage swings at low-supply voltage even in cascoded MOSFET structures due to exponential dependence of I_{DS} upon V_{GS}.

There are several limitations of devices operating in sub-threshold region.

- frequency response of devices is poor.
- drain and source substrate currents associated with the reverse biased diffusion-substrate junction are not necessarily negligible compared to sub-threshold drain current.
- linearity is quite poor for $V_{DS} < 3V_{ther}$ ($V_{ther} = kT/q$). This makes the low-voltage circuit design quite complicated.
- for obtaining higher gain conditions, the device of larger width or low drain current are required and this limits the speed of the sub-threshold circuits.

3.2 Bulk – Driven MOSFETs [10]

MOSFET is biased in saturation mode by applying a dc voltage on gate. The drain is connected normally and the source is grounded and the signal is applied between the bulk and the source. The current flowing in the channel is modulated by the reverse bias on the bulk-channel

junction. The result is a junction field-effect transistor with the bulk as the signal input (gate). Consequently, a high-input impedance depletion-mode device results i.e. V_T gets modulated. Circuit diagram of a current mirror, which utilizes the bulk driven n-type MOSFETs, is shown in Fig. 6. The signal modulates I_{DS} (saturation mode) and the modulation gets transferred to the other circuit ports through the coupling between the ports.

3.2.1 Advantages:

- removes the threshold voltage requirements and the device can be operated at low supply voltages. Due to depletion characteristics zero, negative, and even small positive values of bias voltage can be applied to get the desired dc currents.
- Bulk-driven MOSFETs can work even at 0.9 V (for $V_T \approx 0.8$) and we can use conventional gate to modulate the bulk-driven MOSFETs i.e. the on-off ratio of bulk-driven MOSFET modulated by the gate is very large as the gate can totally shutoff the channel. Moreover experiments show that latch-up problem has not appeared.
- the small-signal transconductance, g_{mb} can be larger than the MOSFET's transconductance, g_m if $V_{BS} \geq .5V$. But there will be appreciable current flowing in bulk-source junction under these conditions.

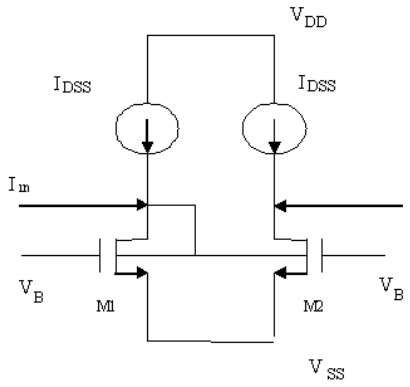

Fig. 6 Current mirror based on bulk-driven N channel MOSFET

3.2.2 Disadvantages

- all the MOSFETs require isolated bulk terminals.
- the capacitance of the bulk-driven MOSFET cause problems. The gate-driven MOSFET's frequency response capability is described by its transitional frequency, f_T

$$f_{T,gate\text{-}driven} \approx g_m/(2\pi C_{gs}) \qquad (12)$$

where C_{gs} is the gate-to-source capacitance. At, frequencies beyond f_T, the device no longer provides signal gain. For the bulk-driven MOSFET

$$f_{T,bulk\text{-}driven} \approx g_{mb}/(2\pi(C_{bs} + C_{bsub})) = \eta g_m/(2\pi(C_{bs} + C_{bsub})) \qquad (13)$$

where η is the ratio of g_{mb} to g_m and is in the range of 0.2 to 0.4, C_{bs} is the bulk-to-source capacitance, and C_{bsub} is the well-to substrate capacitance. For saturated strong inversion

MOSFET operation and using some approximations the transitional frequency relation is given by

$$f_{T,\text{bulk-driven}} \approx (\eta/3.8)\, f_{T,\text{gate-driven.}} \quad (14)$$

- The polarity of the bulk-driven MOSFETs is process related. For P-well process, only N-channel bulk-driven MOSFETs are available, and for N-well process, only P-channel MOSFETs are available. Thus, bulk-driven MOSFETs cannot be used in CMOS structures where both N channel and P channel MOSFETs are required.
- Bulk-driven MOSFETs are fabricated in differential wells to have isolated bulk terminal and the matching between bulk-driven MOSFETs in differential wells suffers. Thus the analog circuit with tight matching between MOSFETs is difficult to fabricate.
- Noise is also a problem for the bulk-driven MOSFET.

3.3 Self-cascode technique

As the device sizes are shrinking fast, the output impedance of the MOSFET is also reducing due to the channel length modulation and these short channel MOSFETs cannot provide high gain structures. To have high output impedance and thereby high gains, cascoding is done. The regular cascode structures are avoided as their use increases the gain of the structure, but decreases the output signal swing. Self-cascode is the new technique, which does not require high compliance voltages at output nodes. It provides high output impedance to give high output gain and so it is useful in low-voltage design.

A self-cascode is a 2-transistor structure [1] (Fig. 7 a), which can be treated as a single composite transistor (Fig. 7 b). The composite structure has much larger effective channel length and the effective output conductance is much low. The lower transistor M1 is equivalent to a resistor, whose value is input dependent.

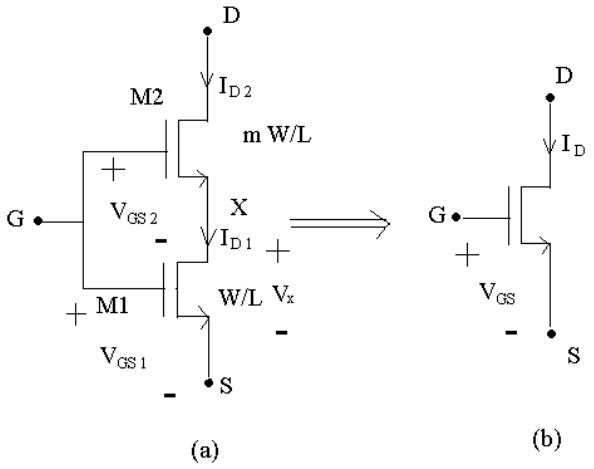

Fig. 7 (a) Self-cascode NMOS transistor (b) Equivalent NMOS transistor

For optimal operation, the W/L ratio of M2 is kept larger than that of M1, i.e., m>>1. The effective g_m for the composite transistor is approximated as

$$g_m \text{ (effective)} = (g_{m2}/m) = g_{m1} \quad (15)$$

For the composite transistor to be in saturation region M2 have to be in saturation and M1 in linear region. For these transistors, the currents I_{D1} and I_{D2} are given as

$$I_{D1} = \beta_1(V_{in} - V_{TN} - (V_X/2))V_X \quad \text{(Ohmic region)} \tag{16}$$

$$I_{D2} = (\beta_2/2)(V_{in} - V_X - V_{TN})^2 \quad \text{(Saturation region)} \tag{17}$$

and from this we get

$$I_{D2} = [(\beta_2\ \beta_1)/(2(\beta_2 + \beta_1))][V_{in} - V_{TN}]^2 \tag{18}$$

$$\beta_{effective} = (\beta_2\ \beta_1)/(\beta_2 + \beta_1) \tag{19}$$

for

$$\beta_2 = m\ \beta_1 \tag{20}$$

$$\beta_{effective} = [m/(m+1)]\ \beta_1 = [1/(m+1)]\ \beta_2 \tag{21}$$

and for $m >> 1$,

$$\beta_{effective} \approx \beta_1 \tag{22}$$

M1 operates in linear region, while M2 operates in saturation or linear region. Hence voltage between source and drain of M1 is small. There is no appreciable difference between the V_{Dsat} of composite and simple transistors and a self-cascode can be used in low voltage operation. For a self-cascode

$$V_{Dsat} = V_{Dsat\text{-}M2} + V_{DS\text{-}M1} \tag{23}$$

or

$$V_{Dsat} = V_{Dsat\text{-}M2} + I_{D2}\ R_{M1} \tag{24}$$

where

$$R_{M1} = 1/(\mu\ C_{OX}\ (V_{in} - V_{TN})\ W/L) \tag{25}$$

The operating voltage of regular cascode is much higher than that of self-cascode and hence a self-cascode structure can be used in the low voltage design. The advantage offered by self-cascode structure is that it offers high output impedance similar to a regular cascode structure while output voltage requirements are similar to that of a single transistor. However, these structures do not provide any benefit at the input node.

3.4 Floating gate MOSFETs

The gate of the FG MOSFET is normally floating on which an electrical charge resides, this charge leaks away very slowly because of very good insulation properties of SiO_2. When the floating gate transistor is bathed in UV light for some time, the charge on the floating gate disappears.

For low voltage analog circuits, FG is assumed to have no charge accumulation. A multi-input floating gate (MIFG) MOSFETs, as shown in Fig 8 [1], is used for analog circuit\s design. For a 2-input MIFG MOSFET a higher dc voltage (V_b) is applied at one gate (i.e. bias gate) and the signal is applied at second gate (signal gate). The V_T for the MOSFET adjusts itself to a new value V_T (equivalent) given by the following

$$V_T(\text{equivalent}) = (V_T - V_b\, k_1)/k_2 \tag{26}$$

where k_1 and k_2 are given as

$$k_1 = C_{G1}/C_{total} \tag{27}$$

$$k_2 = C_{G2}/C_{total} \tag{28}$$

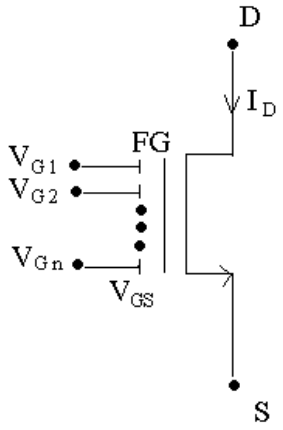

Fig. 8 Multi-input floating gate transistor

C_{G1} and C_{G2} are capacitances between floating gate and control gates respectively. C_{total} is the sum of all the capacitances between control gates and floating gates, capacitance between floating gate to drain, capacitance between floating gate to source and capacitance between floating gate to bulk. The V_T (equivalent) is decided by V_b, k_1, and k_2 and can be made less than V_T. Effective trans-conductance ($g_{m(effective)}$) of the combined structure is given by

$$g_{m(effective)} = k_2\, g_{m(FG)} \tag{29}$$

where $g_{m(FG)}$ is the trans-conductance seen from the floating gate. Here, $g_{m(effective)}$ is less than $g_{m(FG)}$ by a factor of k_2. As there is a DC and AC feedback from drain to floating gate through C_{gd}, the output impedance is less than that of MOSFET working in the same biasing condition. The output conductance (g_0) of the floating gate MOSFET is

$$g_{o(effective)} = (C_{gd}/C_{total})g_m + g_o \tag{30}$$

where C_{gd} and g_o represent the gate to drain capacitance and output conductance of a MOSFET.

So we see that the floating-gate technology can be used in low voltage analog design. Since the output impedance of a floating gate transition is lower and only low gain structures can be realized. This technique also requires fabrication of the floating gates, and hence the conventional technology cannot be used, and results in increased cost.

3.5 Level shifter technique

In this technique, MOSFETs are either operating in saturation or in sub-threshold region. We consider the case of current mirror as shown in the Fig. 9, in which the input current I_{in} flowing through M1 is given by

$$I_{in} = I_{D1} = (K'W/2L)(V_{GS1} - V_T)^2 \tag{31}$$

$$V_{in} = V_{GS} \tag{32}$$

Where W, L, K′, V_{GS1}, V_T have their usual meanings and V_{in} is the input voltage.

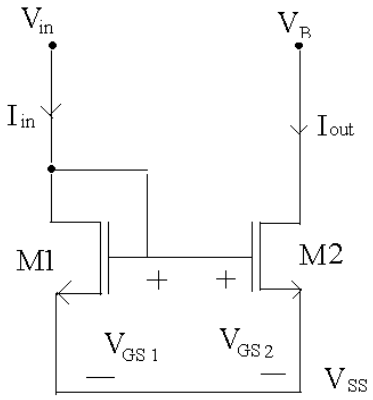

Fig. 9 Simple current mirror

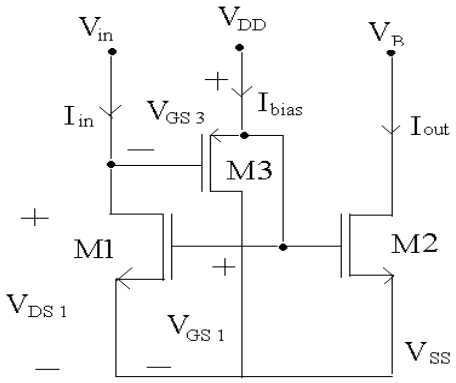

Fig. 10 Level shifter based current mirror

The minimum voltage required at the input has to be more than V_T for the operation of this circuit. So it is not possible to use these mirrors for input voltage levels less than one V_T. The modified version of this circuit is shown in Fig. 10 in which the input voltage requirements of one V_T can be removed.

The input voltage (Vin) is equal to

$$V_{in} = V_{GS1} - V_{GS3} \tag{33}$$

where V_{DS1} is the drain to source voltage for M1, V_{GS1} is the gate to source voltage for M1 and V_{GS3} is the gate to source voltage for M3.

The major drawback offered by this circuit is the offset current flowing into the output transistor for the zero input current. The effect of the offset current is more pronounced when the input current is of the order of the offset circuit. Here with the increase in the number of transistors the power dissipation will also increase.

However the advantages that we obtain are the higher bandwidth at low voltages. The input resistance is also low, which is desirable for current mode circuits. These circuits have the capability for rail-to-rail operation, both at input and output ends.

4 Low-voltage V-I converter

V-I converter is an important circuit block in current code amplifier design. In the circuit shown below Fig. 11 [1] it is assumed that transistors M1 and M2 operate in saturation region.

The drain currents I_{D1} and I_{D2} are given by

$$I_{D1} \approx (\beta_{n1}/2)(V_{in1} - V_{TN})^2 \tag{34}$$

$$I_{D2} \approx (\beta_{p2}/2)(V_{in1} - V_{TP})^2 \tag{35}$$

where

$$V_{in1} = V_{in} - V_{SS} \tag{36}$$

$$V_{in2} = V_{in} - V_{DD} \quad (37)$$

assuming $\beta_{n1} = \beta_{p2} = \beta$, supply voltage $|V_{DD}| = |V_{SS}|$, the output current is given as

$$I_{out} = I_{D1} - I_{D2} \quad (38)$$

$$= 2\beta V_{DD}(V_{in} - V_{TN}) \quad (39)$$

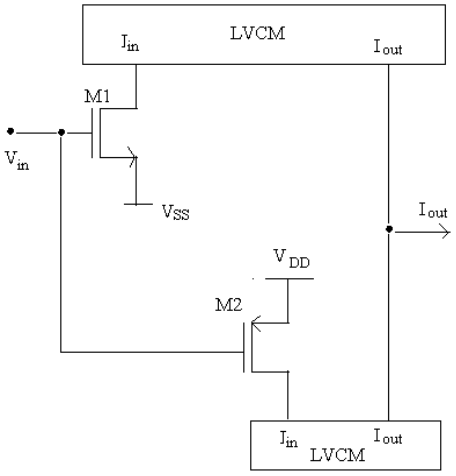

Fig. 11 V-I Converter

From eqn. 39 it is clear that the trans-conductance of this circuit is linearly related to β and V_{DD}. The output current is proportional to input voltage. The circuit has rail-to-rail input voltage swing capability

5 Applications of Current Conveyors

5.1 Current Amplifier

The block diagram for the Current Amplifier is given in Fig. 12). The operation of the current amplifier can be explained from the following equations. If I_{in} denotes the input current then since for CCII the current in the port Y is zero so

$$V_y = I_{in} * R_2 \quad (40)$$

$$V_x = V_y \quad (41)$$

$$V_x = I_x * R_1 \quad (42)$$

$$I_{out} = I_x \quad (43)$$

From above eqns. we conclude that

$$I_{out} = (R_2/R_1)I_{in}. \quad (44)$$

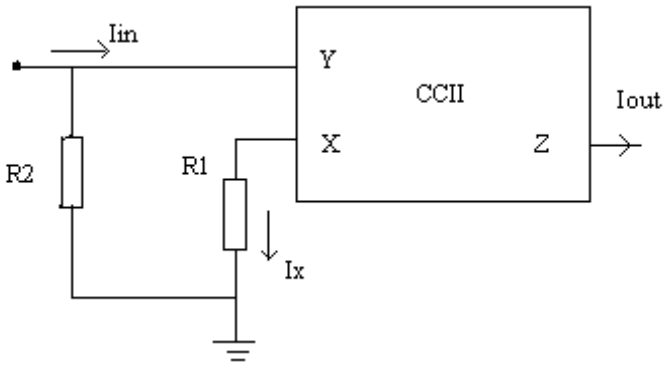

Fig.12 Current Amplifier

5.2 Capacitance Multiplication

Fig. 13 shows the circuit diagram for the capacitance multiplication using current conveyors followed by a current amplifier A_I. It can be shown that the ideal input capacitance is given by $C_{EQ} = A_I C_s$.

$$V_{in} = I_{in} Z_{EQ} \tag{45}$$

$$V_{in} = V_X = I_X /.sC_S = I_Z / sC_S \tag{46}$$

$$I_Z = I_X = I_{in} / A_I = V_{in} / (Z_{EQ} A_I) = I_Z / (Z_{EQ} A_I sC_S); \tag{47}$$

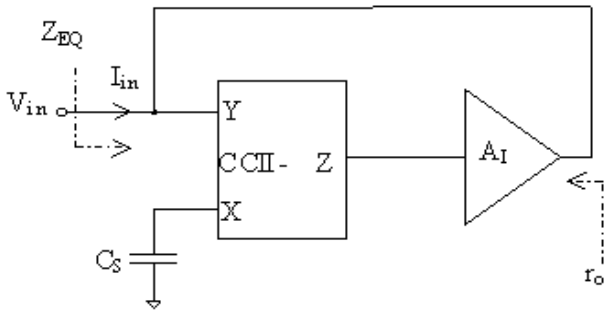

Fig.13 Capacitance multiplication topology

Hence $$1/Z_{EQ} = sC_{EQ} = A_I sC_S; \tag{48}$$

$$C_{EQ} = A_I C_s. \tag{49}$$

6 Low-Voltage Power-Efficient Operational Amplifier Cells

The basic topology of a low-voltage compact op-amp is shown in Fig. 14 [5]. The amplifier consists of a P-channel (PMOS) input stage $M_{20,}$ M_{22}, a current mirror M_8, M_{10} with cascode M_4, $M_{6,}$ and a rail-to-rail output stage M_1, M_2. A PMOS input stage allows the common-mode voltages driven to and below the negative supply rail. The current mirror is needed to sum the opposite-phase signals of the difference input stage in order to drive the gates of the rail-to-rail output stage in phase. The cascades provide the necessary level shift between input and output stage. M_6 provides gain by leaving the high input impedance of the gates of the output stage intact. The output stage is biased in class AB using the voltage source V1, this makes efficient use of the supply current. To set the quiescent current, the sum of the gate-source voltages of the output stage can be controlled in such a way that it is equal to the sum of a reference PMOS gate-source voltage $V_{GS,P}$ and an N-channel NMOS source voltage $V_{GS,P}$, which is obtained by giving V_{AB} the value

$$V_{AB} = V_{DD} - V_{SS} - V_{GS,P} - V_{GS,N} \tag{50}$$

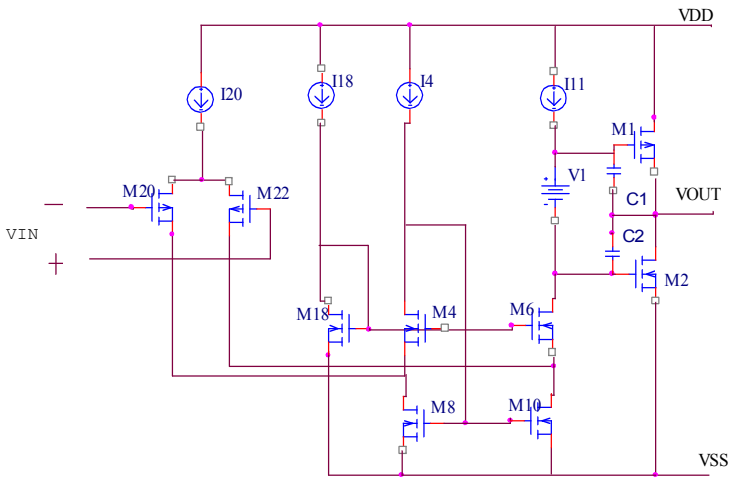

Fig. 14 Compact low-voltage operational amplifier principle

V_{AB} can be negative at low supply voltage and, depending on the type of class-AB behavior, V_{AB} is signal dependent. A smooth switchover from one transistor to the other is obtained, avoiding gross crossover distortion. Due to M_6 the signal contributes to the output voltage (V_{out}) independent of which transistor is active. Two miller capacitors M_1 and M_2 are connected across each output transistor. Miller compensation is sufficient to compensate the op-amp. There is a limit to the minimum supply voltage because output stage has to drive large output currents that will require large gate-source voltages (V_{GS}). The supply voltage of the output stage is equal to the sum of the VGS of M_1, the voltage V_{AB}, and the V_{GS} of M_2. V_{AB} can be negative so theoretically the minimum supply voltage needed by the output stage can be very small. The gate of an output transistor is always connected to the supply rails via a current source in order to obtain sufficient gain in only two stages and the current source should not deteriorate the impedance and must be cascoded. The transistors of the current source should be biased at the edge of the triode region, resulting in a minimum supply voltage limited by a gate-source voltage and two saturation voltages.

7 Conclusion

The present report is the literature survey of the low-voltage current-mode analog cells. Low voltage current mode circuits are essential for the mobile communication devices and portable electronic systems because low voltage reduces the problem related to power dissipation and reliability issues, while the current mode design techniques offer voltage independent high bandwidth analog circuits which are useful in high frequency circuit design applications. The most simple and useful current mode circuits are the current conveyors. They have wide applications in signal processing areas and the fields where mixed circuit design is gaining importance. Voltage mode circuits that were used in the past can now be implemented using current conveyors. Also along with the use of CMCs it is desired to have simple design as they are expected to give better results due to less complexity and so there is effort for circuits that employ simple topologies. The use of current mode circuits will gain more and more importance as the development in portable electronics will advance.

References

1. S. S. Rajput, "Low-voltage current-mode analog circuit structures and their applications", *PhD thesis., Indian Institute of Technology, Delhi.*, Aug. 2001.
2. http://www.maxim-ic.com/appnotes.cfm/appnote_number/725, 29, Dec. 2000.
3. http://www.maxim-ic.com/appnotes.cfm/appnote_number/883, 13, Dec. 2001.
4. N. Weste and K. Eshraghian, "Principles of CMOS VLSI design", *Second Edition, Addison Wesley Longman (Singapore) Pte. Ltd.*
5. K. Langen and J.H. Huijsing, "Compact low-voltage power efficient operational amplifier cells for VLSI", *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1483-1496, Oct. 1998.
6. A. Fabre, "Third generation current conveyor: A new helpful active element", *Electron. Lett.*, vol. 31, no. 5, pp. 338-339, March. 1995.
7. K. C. Smith and A. Sedra, "The current conveyor – a new circuit building block", *Proc. IEEE*, vol. 56, pp. 1368-1369, Aug. 1968.
8. H.W. Cha and K. Watanabe, "Wide band CMOS current conveyor", *Electron. Lett.,* vol. 32, no. 14, pp. 1245-1246, July 1996.
9. http://space.tin.it/scienza/pidelaur/current_conveyor/cap_mult.htm.
10. B.J. Blalock, P.E. Allen and G.A. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology", *IEEE Trans. Circuits and Systems – II*, vol. 45, No. 7, pp. 769-779, July 1998.
11. A. Sedra and K.C. Smith, "A second generation current conveyor and its applications", *IEEE Trans. Circuits Theory*, pp. 132-133, Feb. 1970.
12. M. Ismail and T. Fiez, "Analog VLSI signal and information processing", *McGraw-Hill, Inc.* 1994
13. B.Razavi, "Design of analog CMOS integrated circuits", *McGraw-Hill, Inc.* 2001