

AJITx1x1x32 Processor

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1 Overview

The AJITx1x1x32 is single core processor in the AJIT family of processors. The single core contains a single execution thread, and this thread implements the SPARC-V8 instruction set architecture.

2 Instruction execution thread characteristics

The SPARC-V8 ISA has the following features:

- compact 32-bit RISC instruction set.
- 64-bit/32-bit/16-bit/8-bit load/store instructions.
- 64-bit/32-bit IEEE 754 floating point arithmetic: including divide and square-root.
- Co-processor instruction mappings provide extensibility to the ISA.

The execution thread is a single-issue, in-order, 7-stage pipeline.

- The thread uses branch prediction, and includes a 256 entry branch history table, which remembers the last taken status of up to 256 branches.
- All exceptions are handled precisely.
- 15 interrupt levels are available.
- A full floating point unit is included. This supports single and double precision add, subtract, multiply, divide and square-root operations in hardware.

3 Memory subsystem in a processor core

The processor includes 4-way set associative, write-through (allocate), 32KB data and instruction caches. The caches are virtually indexed and virtually tagged, with a hit access time of two clock cycles.

The processor also includes an implementation of the SPARC V8 reference MMU specification. The MMU includes a 256 entry TLB.

4 Debug support

Each execution pipeline in the processor core has a hardware debug support unit which allows remote debugging using a GDB remote client.

Access to both pipelines is currently provided by a single UART interface.

5 Reference evaluation system

The AJITx1x1x32 processor has been prototyped on an FPGA card (Xilinx KC705), with DDR3 DRAM and the following peripherals: UARTx2, SPI-master, SPI-flash, Timer and Interrupt-controller.

6 Contact

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