1. 3D capacitance extractor for VLSI interconnect analysis (currently being used in Industry). This uses a Monte Carlo technique and is available as open-source software. The project was sponsored by Intel Corp.

2. Conceptualization and development of a network packet classification ASIC. The project was sponsored by RIMO technologies (later SwitchOn Networks, acquired by PMC-Sierra).

3. Founding partner in Powailabs (an IIT-Bombay incubated company). The company has developed an FPGA based simulation accelerator which can be used in a seamless manner to accelerate the simulation of VLSI designs described in VHDL/Verilog (see http://www.powailabs.com for more details).

4. FPGA based fault-simulator: Mapped the differential fault simulation algorithm to an FPGA based system, demonstrated on industrial circuits. The project was sponsored by Intel Corp.

5. A complete C-to-RTL flow which takes as its input a C program and produces a VHDL netlist which implements this program. This is available as open source software for general use. This work has led to funding of projects from Ericsson, Seagate, DeiTy.

6. FPGA based reconfigurable-computing system: write algorithms in C and get implementations in FPGA. Funded by Powailabs Technologies Pvt. Ltd.

7. 32-bit processor (code-name AJIT) implementation with development tools, Linux port and FPGA prototype: project sponsored by DeiTY/Powailabs under a matching grants scheme. AJIT is a part of the indigenous processor development effort championed by DeiTY. A proof-of-concept implementation of the AJIT processor in Silicon has been implemented at SCL Chandigarh in a 180nm technology.

8. A digital SOC for implementing an IRNSS receiver (NAVIC) using an embedded AJIT processor has been implemented in 65nm CMOS technology, and is functional!

9. An extension of the AJIT 32-bit processor to include 64-bit instructions and multi-core implementations. A four core, eight thread processor has been implemented and is being used to implement a network router.