

Some of my publications, categorized into different areas.

0.1 Design Automation

1. M.P. Desai, I. Hajj, "On the convergence of block relaxation methods for circuit simulation", IEEE Transactions on Circuits and Systems, July 1989.
2. M.P. Desai, J. Jensen, R. Cvijetic, "Sizing of clock distribution networks for high performance CPU chips", Proceedings of the 33rd annual conference on Design automation, 1996.
3. Madhav P. Desai, Y.T. Yen "A systematic technique for verifying critical path delays in a 300MHz Alpha CPU design using circuit simulation", Proceedings of the 33rd annual conference on Design automation, Las Vegas 1996.
4. Nevine Nassif, Madhav P. Desai, Dale H. Hall, Robust Elmore delay models suitable for full chip timing verification of a 600MHz CMOS microprocessor, Proceedings of the 35th annual conference on Design Automation, San Francisco, 1998.
5. Rupesh S. Shelar, Madhav P. Desai, H. Narayanan, Decomposition of Finite State Machines for Area, Delay Minimization, Proceedings of the 1999 IEEE International Conference on Computer Design (ICCD99), 1999.
6. B.N.V.M. Gupta, H. Narayanan, M.P. Desai, A State Assignment Scheme Targeting Performance and Area, Proceedings of the International Conference on VLSI Design, 1999.
7. R. Shelar, H. Narayanan, M. Desai, Orthogonal partitioning and gated clock architecture for low power realization of FSMs, Proceedings of the 13th Annual IEEE International ASIC/SOC Conference, 2000.
8. Batterywala, S.H. Desai, M.P. Variance reduction in Monte Carlo capacitance extraction, Proceedings of the 18th International Conference on VLSI Design, 2005.
9. S. Sahasrabuddhe, H. Raja, K. Arya, M.P. Desai, AHIR: A Hardware Intermediate Representation for Hardware Generation from High-level Programs, Proceedings of the 20th International Conference on VLSI Design, 2007.
10. S. Sahasrabuddhe, S. Sreenivasan, K. Ghosh, K. Arya, M.P. Desai, A C-to-RTL flow as an energy efficient alternative to the use of embedded processors in digital systems, Proceedings of the 13th EUROMICRO Conf. on Digital System Design, 2010.
11. T. Rinta-Aho, M. Karlsted, M.P. Desai, "The Click2Netfpga Toolchain, USENIX ATC-2012, Boston, 2012.

12. N. Karanjkar, Madhav Desai, Shalabh Bhatnagar, "A Simulation Based Technique for Continuous Space Embedding of Discrete Parameter Queueing Systems," Proceedings of the 32nd annual European Simulation and Modelling Conference 2018 (ESM'2018).
13. N. Karanjkar, M. Desai, "Sitar: A Cycle-based Discrete-Event Simulation Framework for Architecture Exploration", Proceedings SIMULTECH 2022 (Best paper award).

0.2 Probability, algorithms and graph theory

1. Madhav P. Desai, Vasant B. Rao On the convergence of reversible Markov chains, SIAM Journal on Matrix Analysis and Applications Volume 14, Issue 4 (October 1993).
2. M.P. Desai, V.B. Rao, A characterization of the smallest eigenvalue of a graph, Journal of Graph Theory Volume 18, Issue 2 (March 1994).
3. M Desai, S Kumar, PR Kumar, Quasi-Statically Cooled Markov Chains, Probability in the Engineering and Informational Sciences, 1994.
4. M.P. Desai, VB Rao, Finite-Time Behavior of Slowly Cooled Annealing Chains, Probability in the Engineering and Informational Sciences 1997.
5. M.P. Desai, Some results characterizing the finite time behaviour of the simulated annealing algorithm, Sadhana, vol. 24, pp. 317-337, 1999.
6. Desai, M. Manjunath, D. On the connectivity in finite ad hoc networks, IEEE Communications Letters, Oct 2002.
7. Madhav Desai, D. Manjunath On Range Matrices and Wireless Networks in d Dimensions, Proceedings of the Third International Symposium on Modeling and Optimization in Mobile, Ad Hoc, and Wireless Networks (WiOpt05), 2005.
8. Madhav P. Desai, On Cycles in Random Graphs, Arxiv arXiv:1009.6046, 2010.
9. M.P. Desai, V.R. Sule, Generalized cofactors and decomposition of Boolean satisfiability problems, arXiv:1412.2341v1, 2014.

0.3 Devices and Circuits

1. N. Mohapatra, M. Desai, S. Narendra, V. R. Rao, Impact of High-K Gate Dielectrics on Sub 100 nm CMOS Circuit Performance, Proceedings of the 31st European Solid-State Device Research Conference, 2001.

2. A. P. Nair, A. Gupta, M. Desai, An On-Chip Coupling Capacitance Measurement Technique, Proceedings of The 14th International Conference on VLSI Design, 2001.
3. M.S. Baghini, M.P. Desai Impact of technology scaling on metastability performance of CMOS synchronizing latches, Proceedings of the 15th International Conference on VLSI Design 2002.
3. P. Sivaram, B. Anand, M. Desai, Silicon film thickness considerations in SOI-DTMOS, IEEE Electron Device Letters, 2002.
4. Mohapatra, N.R., Desai, M.P., Narendra, S.G., Rao, V.R. The effect of high-K gate dielectrics on deep submicrometer CMOS device and circuit performance, IEEE Transactions on Electron Devices, 2002.
5. N. Mohapatra, M. Desai, S. Narendra, V.R. Rao, Modeling of parasitic capacitances in deep submicrometer conventional and high-K dielectric MOS transistors, IEEE Transactions on Electron Devices, April 2003.
6. Prasad, V. Desai, M.P. Interconnect delay minimization using a novel pre-mid-post buffer strategy, Proceedings of the 16th International Conference on VLSI Design, 2003.
7. G.T. Hazari, M.P. Desai, A. Gupta, and S. Chakraborty, A novel technique towards eliminating the global clock in VLSI circuits, Proceedings of the 17th International Conference on VLSI Design, 2004.
9. B. Anand, M.P. Desai, V.R. Rao Silicon film thickness optimization for SOI-DTMOS from circuit performance considerations, IEEE Electron Device Letters, 2004.
8. Narasimhulu, K. Desai, M.P. Narendra, S.G. Rao, V.R. The effect of LAC doping on deep submicrometer transistor capacitances and its influence on device RF performance, IEEE Transactions on Electron Devices, 2004.
9. V. Prasad, M. Desai, On buffering schemes for long multi-layer nets, Proceedings of the 17th IEEE International Conference on VLSI Design, 2005.
10. N. Rao, M. Desai, "A detailed characterization of errors in logic circuits due to single-event transients", Proceedings EUROMICRO Conference on Digital System Design, 2015.
11. P. Adhikari, M. Desai, M. Chandorkar, "A method for seamless tracking of capacitance voltages in a Modular Multilevel Converter", International Conf. on Power Electronic Drives and Energy Systems for Industrial Growth, 2016.

0.4 VLSI Systems

1. M. Desai, R. Gupta, A. Karandikar, K. Saxena, V. Samant, Reconfigurable finite-state machine based IP lookup engine for high-speed router, IEEE Journal on Selected Areas in Communications, May 2003.

2. A. Mittal, M. Desai, A distributed and pipelined controller for a modular and scalable hardware emulator, Proceedings of the 17th International Conference on VLSI Design, 2004.
3. G. Hazari, H. Kasture, M.P. Desai, On the Impact of Address Space Assignment on Performance in Systems-on-Chip, Proceedings of the 20th International Conference on VLSI Design, 2007.
4. P. Kumar, M.P. Desai, Learning based address mapping for improving the performance of memory subsystems, Proceedings of MASCOTS 2009, 2009.
5. G. Hazari, S. Gangam, M.P. Desai, Bottleneck Identification Techniques Leading to Simplified Performance Models for Efficient Design Space Exploration in VLSI Memory Systems, Proceedings of the 23rd International Conference on VLSI Design, 2010.
6. N. Karanjkar, M.P. Desai, An Approach to Discrete Parameter Design Space Exploration of Multi-core Systems Using a Novel Simulation Based Interpolation Technique, Proceedings of MASCOTS 2015, Atlanta, pp. 85-88.
7. K. Lakhotia, G. Caffarena, A. Gil, D. G. Marquez, A. Otero and M. P. Desai, Low-power, Low-latency Hermite Polynomial Characterization of Heartbeats using a Field-Programmable Gate Array, Proceedings IWB-BIO 2016, Granada, Spain.
8. M. P. Desai, G. Caffarena, R. Jvetic, D. Marquez, A. Otero, "A Low-Latency, Low-Power FPGA Implementation of ECG Signal Characterization Using Hermite Polynomials," Electronics 2021, 10(19).
9. M. P. Desai, A. Deshmukh, "An efficient reverse-lookup table based strategy for solving the synonym and cache coherence problem in virtually indexed, virtually tagged caches," arXiv preprint arXiv:2108.00444, 2021.