2nd IEEE International Workshop on Reliability Aware System Design and Test

(In conjunction with the International Conference on VLSI Design)

Chennai, India January 6-7, 2011

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Even as advances in CMOS technology come up against physical limits of material properties and lithography, raising many new challenges that must be overcome to ensure IC quality and reliability, there appears to be no obvious alternate technology that can replace End-of-Roadmap CMOS over the next decade. However, many reliability challenges from increasing defect rates, manufacturing variations, soft errors, wearout, etc. will need to be addressed by innovative new design and test methodologies if device scaling is to continue on track as per Moore's Law to 10nm and beyond. The key objective of this annual workshop, planned to be held in conjunction with the International Conference on VLSI Design, is to provide an informal forum for vigorous creative discussion and debate of this area. The aim is to encourage the presentation and discussion of truly innovative and "out-of-the-box" ideas that may not yet have been fully developed for presentation at reviewed conferences to address these challenges. Additionally, the workshop invites embedded talks and tutorials on cutting edge topics related to reliability aware design of CMOS and hybrid nanotechnology systems.

Representative topics include, but are not limited to:

- Design for test,
- Built-in self-test
- ATPG and defect oriented test
- Delay test
- Low power test
- Instruction-based self-test
- On-line test methodology
- Reliability of CMOS circuits
- Self checker circuits
- Self diagnosis methods
- Fault tolerant micro-architecture
- Self-healing system design
- Energy and performance aware fault - tolerant micro-architectures
- Device degradation and mitigation
- System validation methodology
- Secure system design
- Design for reliability, dependability, and verifiability

Submissions

Authors are invited to submit previously unpublished technical proposals. The proposals must be full papers not to exceed 6 pages. Each submission should include: title, full name and affiliation of all authors, a short abstract of 50 words, and 6 to 7 keywords. Also, identify a contact author and include a complete correspondence address, phone number, fax number, and e-mail address. Submit a copy of your proposal in PDF either online submission via workshop website http://www.serc.iisc.ernet.in/~viren/RASDAT11/ or via e-mail to : rasdat2011@easychair.org, **rasdat2011@serc.iisc.ernet.in**

Submissions are due no later than **October 10, 2010 (EXTENDED)**. Authors will be notified of the disposition of their presentation by **October 31, 2010** Authors of accepted presentations must submit the final paper by **December 1, 2010** for inclusion in the Workshop Proceedings, which will be provided to the attendees.

Website: http://www.serc.iisc.ernet.in/~viren/RASDAT11/

General Information

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