RASDAT 2016

IEEE International Workshop on Reliability Aware System Design and Test 2016

Technical Program

January 7, 2015 – Thursday

9:00 am – 9:50 am	Opening Ceremony & Keynote Address Speaker: Masahiro Fujita, Tokyo University
9:50 am – 10:45 am	Invited Talk – I Speaker: Debdeep Mukhopadhyay, IIT Kharagpur
10:45 am – 11:00 am	COFFEE BREAK
11:00 am – 12:45 pm	Technical Session -1 (S1) System Level Reliability
12:45 pm – 1:30 pm	LUNCH
1:30 pm – 2:00 pm	Invited Talk – II Speaker: Ansuman Banerjee, ISI Kolkata
2:00 pm – 3:30 pm	Technical Session –II (S2) Device Level Reliability
3:30 pm – 3:45 pm	COFFEE BREAK
3:45 pm – 4:15 pm	Invited Talk – III
4:15 pm – 5:30 pm	Technical Session – III (S3) Analysis
5:30 pm – 5:35 pm	Closing

Technical Sessions

S1: Technical Session – I (System Level Reliability Issues)

S1.1 A Novel Design of Reversible Cryptographic Circuit
Bikromadittya Mondal, Kushal Dey, Paramita Roy and Susanta Chakraborty (IIEST, Kolkata)
S1.2 ESR3D: Extended Segment Based Routing Algorithm for 3D NoCs
Priyanka Mitra (MNIT, Jaipur)
S1.3 On-chip True Random Number Generator using System Monitor and Linear Feedback Shift Register
Pravin Zode and Vivek Sakhare
S1.4 Bombay-Scan: A Low Power Reconfigurable Scan Architecture
Binod Kumar, Boda Nehru, Brajesh Pandey (IIT Bombay) and Jaynarayan Tudu (IISc, Bangalore)
S1.5 BER Test Time Optimization
Suhas Shinde and Jan Knudsen (Intel Duetschland, Germany)

S2: Technical Session – II (Device Level Reliability Issue)

S2.1 A Novel Mixing Technique for Low Cost Sample Preparation in Digital Microfluidic Biochip
Chandan Das, Sarit Chakraborty and Susanta Chakraborty (IIEST, Kolkata)
S2.2 Golden Chip Free HT Detection and Diagnosis Using Power Signature Analysis
Sree Ranjani, Nirmala Devi, M. Jayakumar, and P.K. Maneesh (Amrita University)
S2.3 Analysis of FinFET based SRAM Cell Stability under Work Function Variability
Mitesh Limachhia, Rajesh Thakker, and Nikhil Kothari (DD University)
S2.4 Reliability of Silicon Carbide based Double-gate Junctionless Transistor for High Temperature Applications
Ratul Kumar Baruah (Tezpur Univ.) and R.P. Paily (IIT Guwahati)

S3:Technical Session – III (Analysis)

S3.1 Mathematical Modeling and Analysis of New Modified Glitch Free Adiabatic Inverter Circuit with Trapezoidal Power Supply
Alak Majumder and Rahul Kaushik (NIT Arunachal Pradesh)
S3.2 Experimental Study of A Novel Variant of Fiduccia Mattheyses(FM) Partitioning Algorithm
Rakesh Mohanty, Suchismita Pattanai (VSSUT) and Prachi Puravi Tripathy (SUIIT)
S3.3 Pattern analysis and transmission of sleep apnea ECG signal using bi-phase modulation technique
Chandan Das, Sarit Chakraborty (IIEST) and Chandramallika Paul (IPGMER)