

EE101: JFET operation and characteristics



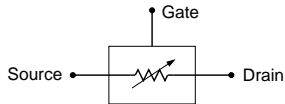
M. B. Patil

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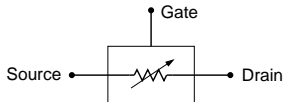
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Department of Electrical Engineering
Indian Institute of Technology Bombay

Field-effect transistors

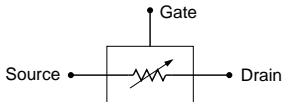


Field-effect transistors



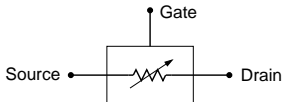
- * A Field-Effect Transistor (FET) has a gate (G) terminal which controls the current flow between the other two terminals, viz., source (S) and drain (D).

Field-effect transistors



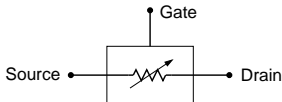
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- * In simple terms, a FET can be thought of as a resistance connected between S and D, which is a function of the gate voltage V_G .

Field-effect transistors



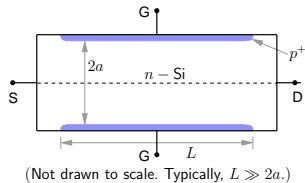
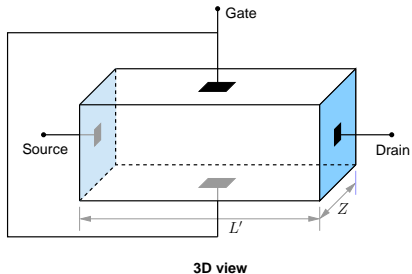
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- * The mechanism of gate control varies in different types of FETs, e.g., JFET, MESFET, MOSFET, HEMT.

Field-effect transistors

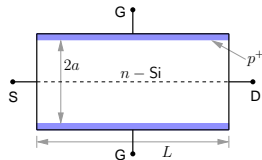


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- * The mechanism of gate control varies in different types of FETs, e.g., JFET, MESFET, MOSFET, HEMT.
- * FETs can be used for analog and digital applications. In each case, the fact that the gate is used to control current flow between S and D plays a crucial role.

Junction Field-effect transistors (JFET)

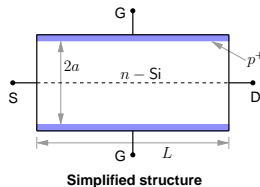
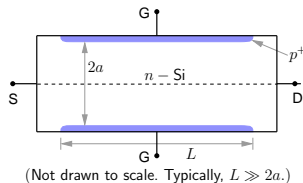
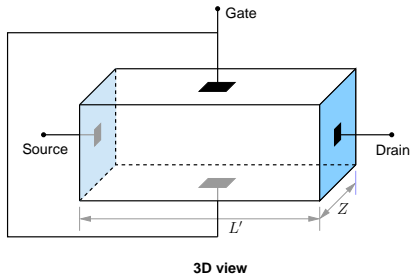


Cross-sectional view



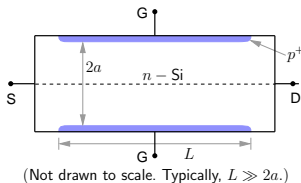
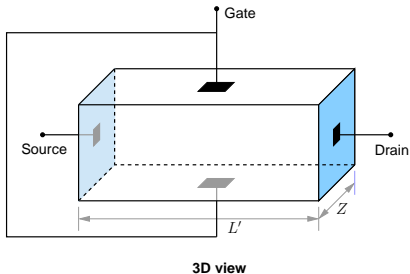
Simplified structure

Junction Field-effect transistors (JFET)

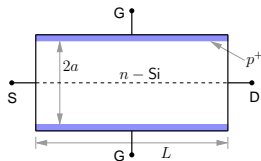


- * The n -type region between the top and bottom p^+ regions offers a resistance to current flow. The resistance depends on V_G .

Junction Field-effect transistors (JFET)



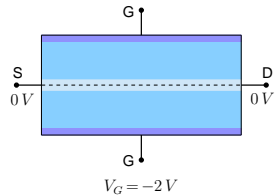
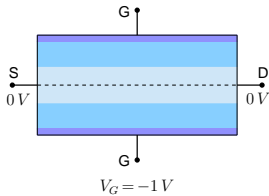
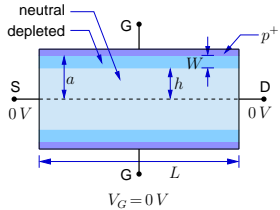
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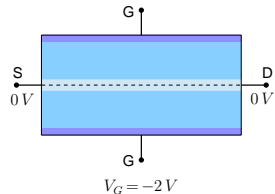
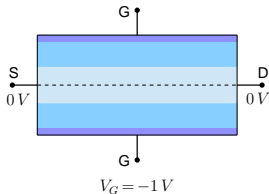
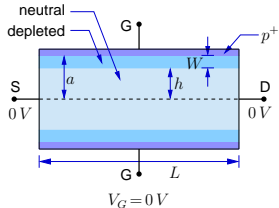
Simplified structure

- * The n -type region between the top and bottom p^+ regions offers a resistance to current flow. The resistance depends on V_G .
- * We will first consider the case, $V_D = V_S = 0 \text{ V}$.

JFET with $V_S = V_D = 0\text{ V}$

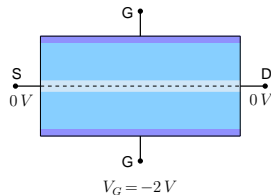
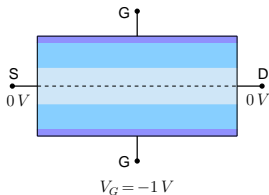
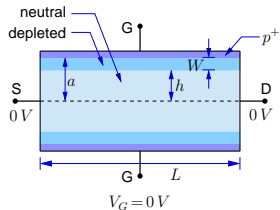


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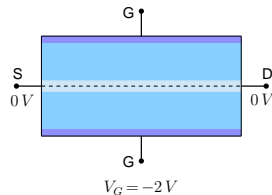
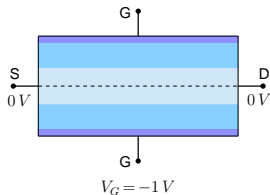
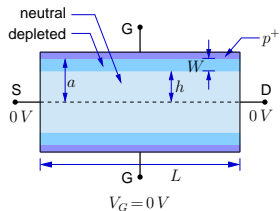
- * The bias across the p - n junction is $(V_G - V_S)$, i.e., V_G , since $V_S = V_D = 0\text{ V}$.

JFET with $V_S = V_D = 0\text{ V}$



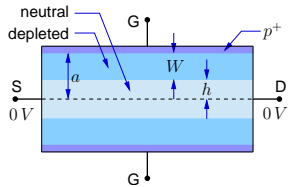
- * The bias across the p - n junction is $(V_G - V_S)$, i.e., V_G , since $V_S = V_D = 0\text{ V}$.
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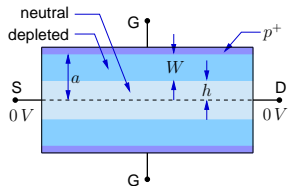


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- * As the reverse bias across the junction is increased (by making V_G more negative), the depletion region widens, and the resistance offered by the n -region increases.
- * When the reverse bias becomes large enough, the depletion region consumes the entire n -region. The corresponding V_G is called the "pinch-off" voltage.

JFET: pinch-off voltage

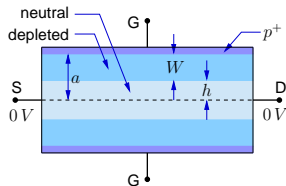


JFET: pinch-off voltage



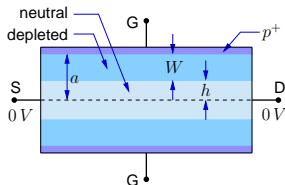
* $V_P = V_G$ for which $h = 0$, i.e., $W = a$.

JFET: pinch-off voltage



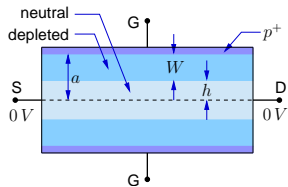
- * $V_P = V_G$ for which $h = 0$, i.e., $W = a$.
- * For a p^+-n junction, $W = \sqrt{\frac{2\epsilon(V_{bi} - V)}{qN_d}}$, where V_{bi} is the built-in potential of the junction.

JFET: pinch-off voltage

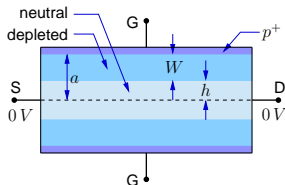


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- * For pinch-off, $W = a = \sqrt{\frac{2\epsilon(V_{bi} - V)}{qN_d}}$
 $\Rightarrow V_P = V_{bi} - \frac{qN_d a^2}{2\epsilon}$.

JFET: pinch-off voltage

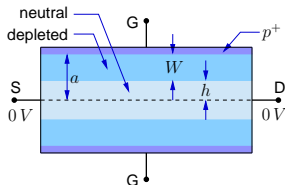


JFET: pinch-off voltage



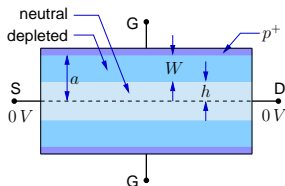
* For pinch-off, $W = a = \sqrt{\frac{2\epsilon(V_{bi} - V)}{qN_d}} \Rightarrow V_P = V_{bi} - \frac{qN_d a^2}{2\epsilon}$.

JFET: pinch-off voltage



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- * Example: $N_d = 2 \times 10^{15} \text{ cm}^{-3}$, $a = 1.5 \mu\text{m}$, $V_{bi} = 0.8 \text{ V}$.

JFET: pinch-off voltage

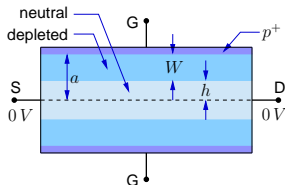


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$$W = 0.8 - \frac{(1.6 \times 10^{-19} \text{ Coul})(2 \times 10^{15} \text{ cm}^{-3})((1.5 \times 10^{-4})^2 \text{ cm}^2)}{2 \times 11.7 \times 8.85 \times 10^{-14} \text{ F/cm}}$$
$$= 0.8 - 3.48 \approx -2.7 \text{ V}.$$

JFET: pinch-off voltage



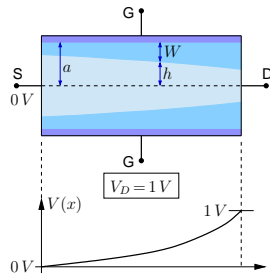
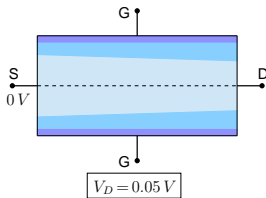
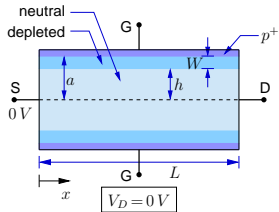
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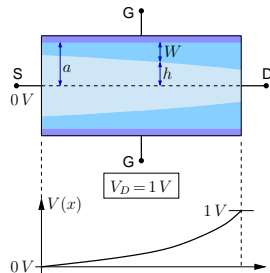
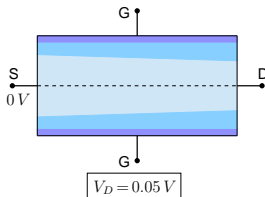
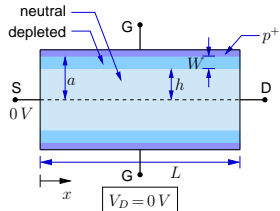
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$$= 0.8 - 3.48 \approx -2.7 \text{ V}.$$

\Rightarrow If a gate voltage $V_G = -2.7 \text{ V}$ is applied, the n-channel gets pinched off, and the device resistance becomes very large.

JFET with $V_G = \text{constant}$, $V_D \neq 0 V$

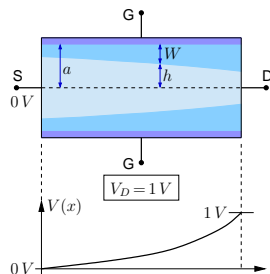
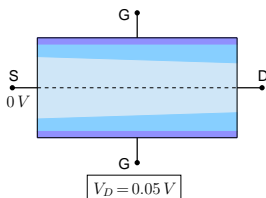
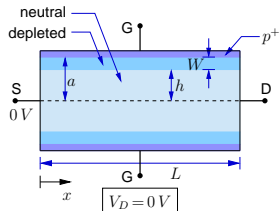


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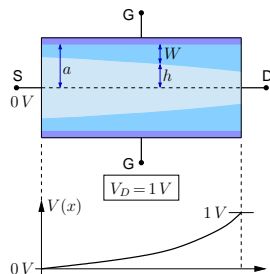
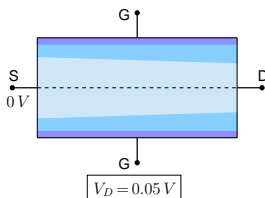
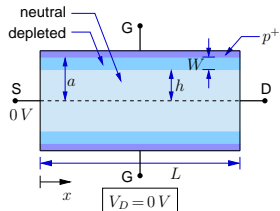
* Consider an n -JFET with V_G constant (and not in pinch-off mode).

JFET with $V_G = \text{constant}$, $V_D \neq 0 \text{ V}$



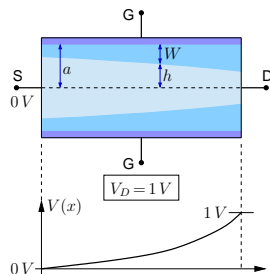
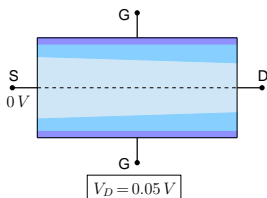
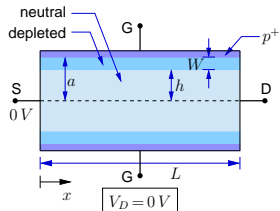
- * Consider an n -JFET with V_G constant (and not in pinch-off mode). If a positive V_D is applied, the potential $V(x)$ inside the channel from S to D (along the dashed line) increases from 0 V to V_D .

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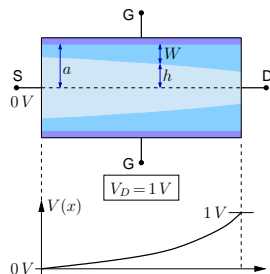
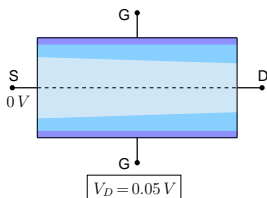
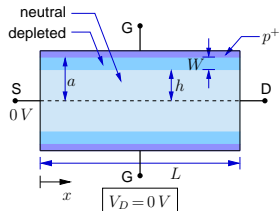
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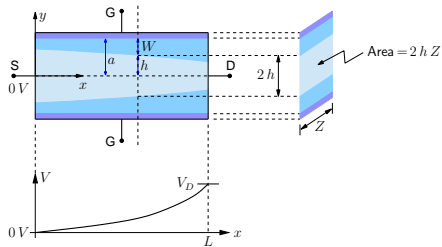
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- Since the p - n junction bias at a given x is $(V_G - V(x))$, the drain end of the channel has a larger reverse bias than the source end.

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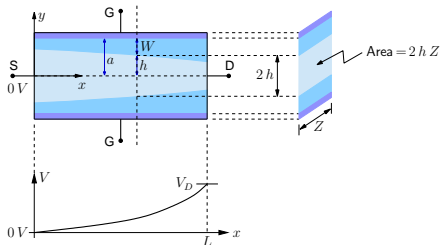


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- Since the p - n junction bias at a given x is $(V_G - V(x))$, the drain end of the channel has a larger reverse bias than the source end.
 \Rightarrow the depletion region is wider at the drain.

JFET: derivation of I_D equation



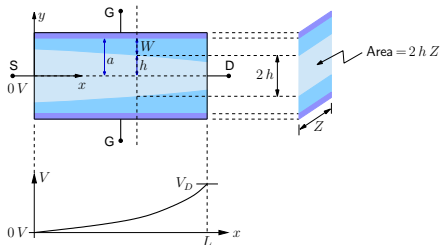
JFET: derivation of I_D equation



Consider a slice of the device. The current density at any point in the neutral region is assumed to be in the x direction, and given by,

$$J_n = q\mu_n nE + qD_n \frac{dn}{dx} \approx q\mu_n nE = q\mu_n N_d \frac{dV}{dx} ,$$

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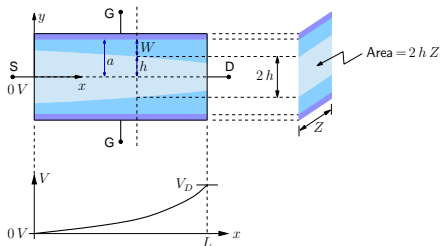


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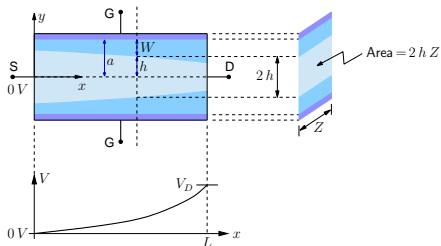
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Note that only the neutral part of the n -Si conducts since there are no carriers in the depletion regions.

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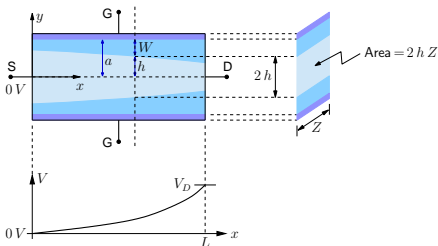
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At a given x , the current I_D is obtained by integrating J_n over the area of the neutral channel region (see figure on the right). Since J_n is constant over this area,

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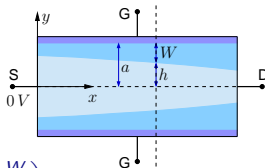
Note that only the neutral part of the n -Si conducts since there are no carriers in the depletion regions.

At a given x , the current I_D is obtained by integrating J_n over the area of the neutral channel region (see figure on the right). Since J_n is constant over this area,

$$I_D(x) = \iint J_n dx dz = 2hZ \times \left(q\mu_n N_d \frac{dV}{dx} \right) = 2qZ\mu_n N_d a \frac{dV}{dx} \left(1 - \frac{W}{a} \right),$$

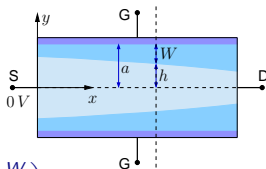
where we have used $h = a - W$, i.e., $h = a(1 - W/a)$.

JFET: derivation of I_D equation



$$I_D(x) = 2 q Z \mu_n N_d a \frac{dV}{dx} \left(1 - \frac{W}{a} \right).$$

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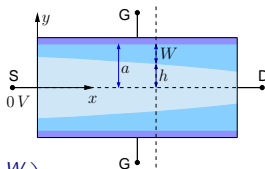
Since $I_D(x)$ is constant from $x=0$ to $x=L$, we get,

$$\int_0^L I_D dx = I_D L = 2qZ\mu_n N_d a \int_0^{V_D} \left(1 - \sqrt{\frac{2\epsilon}{qN_d a^2}} \sqrt{V_{bi} - (V_G - V)} \right) dV,$$

where we have used, for the depletion width W ,

$$W(x) = \sqrt{\frac{2\epsilon}{qN_d} [V_{bi} - (V_G - V)]}.$$

JFET: derivation of I_D equation



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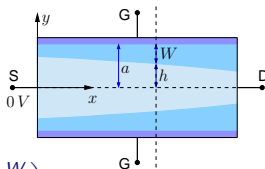
$$W(x) = \sqrt{\frac{2\epsilon}{qN_d} [V_{bi} - (V_G - V)]}.$$

Evaluating the integral and using $V_{bi} - V_P = \frac{qN_d a^2}{2\epsilon}$, we get (do this!)

$$I_D = G_0 \left\{ V_D - \frac{2}{3} (V_{bi} - V_P) \left[\left(\frac{V_D + V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} \right] \right\},$$

where $G_0 = 2qZ\mu_n N_d a/L$.

JFET: derivation of I_D equation



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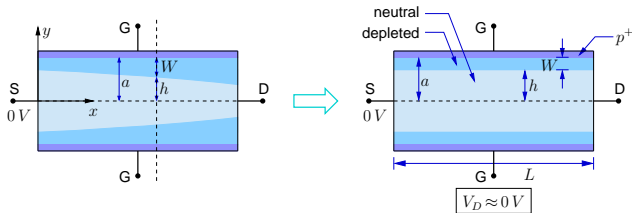
Evaluating the integral and using $V_{bi} - V_P = \frac{qN_d a^2}{2\epsilon}$, we get (do this!)

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where $G_0 = 2qZ\mu_n N_d a / L$.

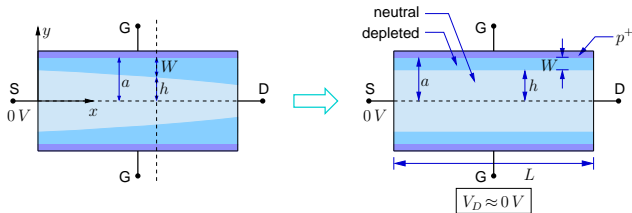
Note that G_0 is the channel conductance if there was no depletion, i.e., if $h(x) = a$ throughout the channel.

Special case: $V_D \approx 0\text{ V}$



$$I_D = G_0 \left\{ V_D - \frac{2}{3} (V_{bi} - V_P) \left[\left(\frac{V_D + V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} \right] \right\}$$

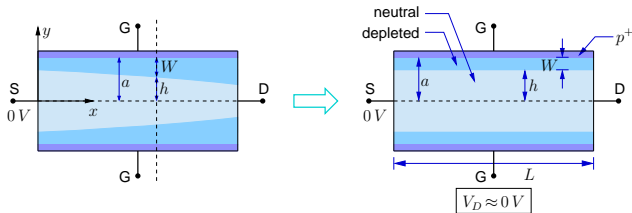
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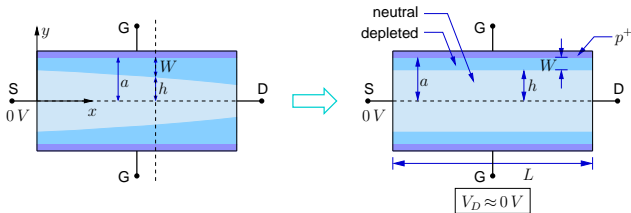
$$\approx G_0 \left\{ V_D - \frac{2}{3} (V_{bi} - V_P)^{-1/2} \left[\frac{3}{2} V_D (V_{bi} - V_G)^{1/2} \right] \right\} \quad (\text{using Taylor's series})$$

Special case: $V_D \approx 0 V$



$$\begin{aligned}
 I_D &= G_0 \left\{ V_D - \frac{2}{3} (V_{bi} - V_P) \left[\left(\frac{V_D + V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} \right] \right\} \\
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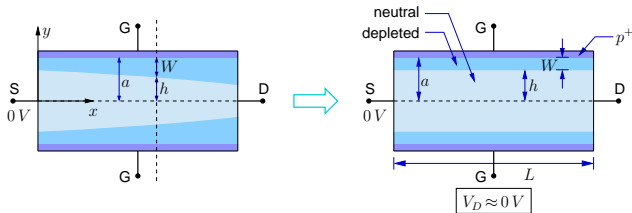
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Since $W = \frac{2\epsilon}{qN_d} (V_{bi} - V_G)^{1/2}$, and $a = \frac{2\epsilon}{qN_d} (V_{bi} - V_P)^{1/2}$, we get

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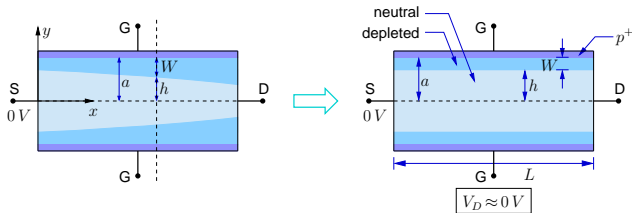


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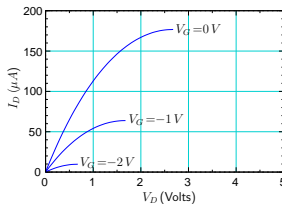
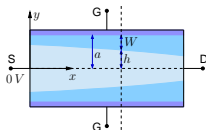
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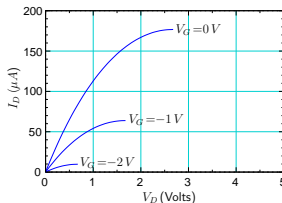
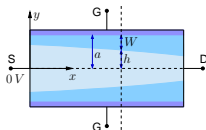
This simply shows that the channel conductance reduces linearly with W (as seen before the $V_S = V_S = 0 \text{ V}$ condition), and for $V_G = V_P$ (i.e., $W = a$), the conductance becomes zero.

JFET: pinch-off near drain



$$I_D = G_0 \left\{ V_D - \frac{2}{3} (V_{bi} - V_P) \left[\left(\frac{V_D + V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} \right] \right\}.$$

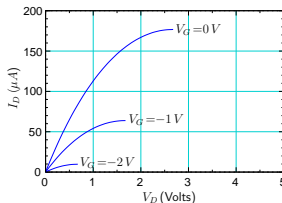
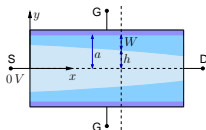
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For a given V_G , I_D reaches a maximum at $V_D = V_G - V_P$ (show this by differentiating the above equation).

JFET: pinch-off near drain

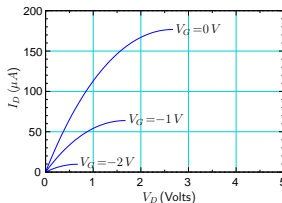
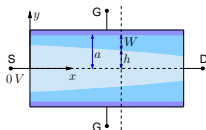


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At this value of V_D , the bias across the p - n junction at the drain end is $V_G - V_D = V_P$.

JFET: pinch-off near drain

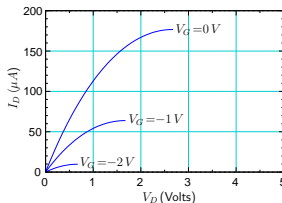
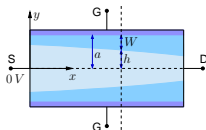


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At this value of V_D , the bias across the p - n junction at the drain end is $V_G - V_D = V_P$. In other words, the drain end of the channel has *just* reached pinch-off.

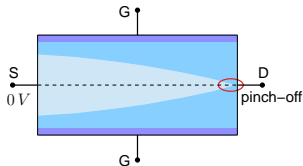
JFET: pinch-off near drain



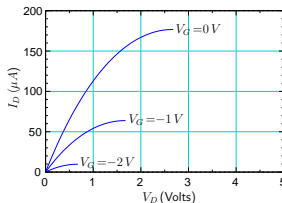
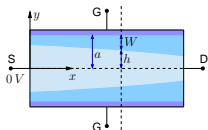
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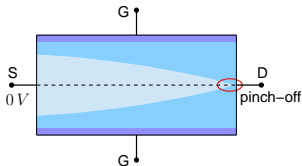
JFET: pinch-off near drain



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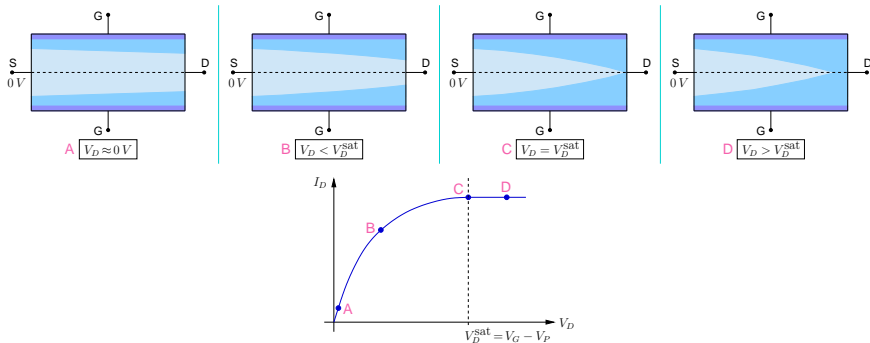
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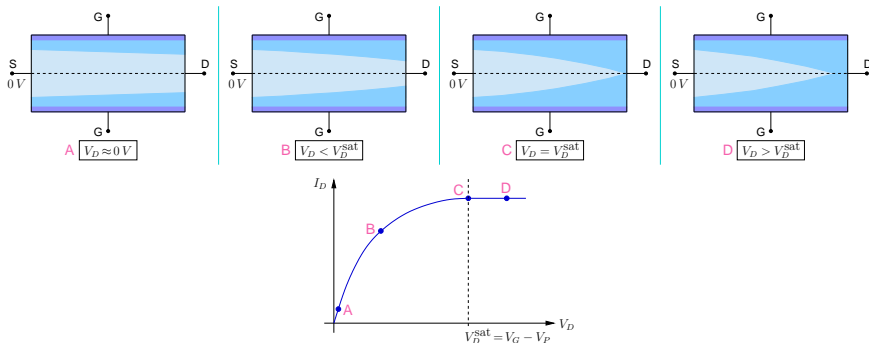
What happens if V_D is increased further?

JFET: saturation



Consider a fixed V_G with V_D varying from $\sim 0V$ to a value beyond condition C.

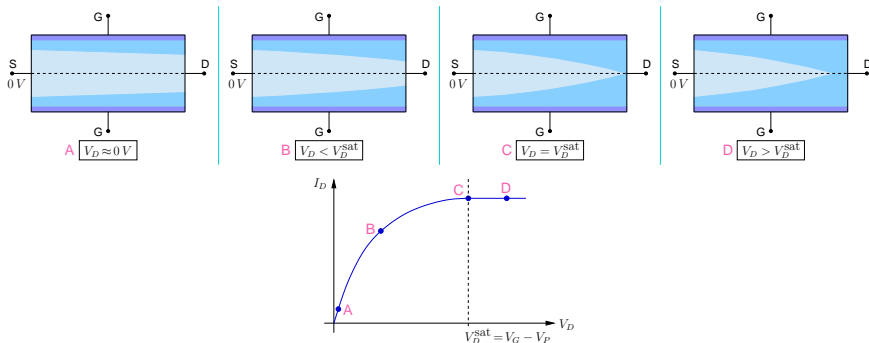
JFET: saturation



Consider a fixed V_G with V_D varying from $\sim 0\text{ V}$ to a value beyond condition C.

In this situation, i.e., $V_D > V_D^{\text{sat}}$, a *short* high-field region develops near the drain end, and the "excess" voltage, $V_D - V_D^{\text{sat}}$ drops across this region.

JFET: saturation

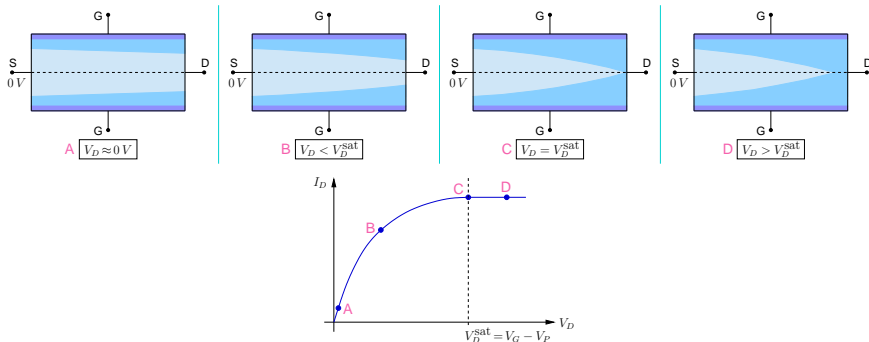


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Because the high-field region is confined to a very small distance, the conditions in the device are almost identical in C and D.

JFET: saturation



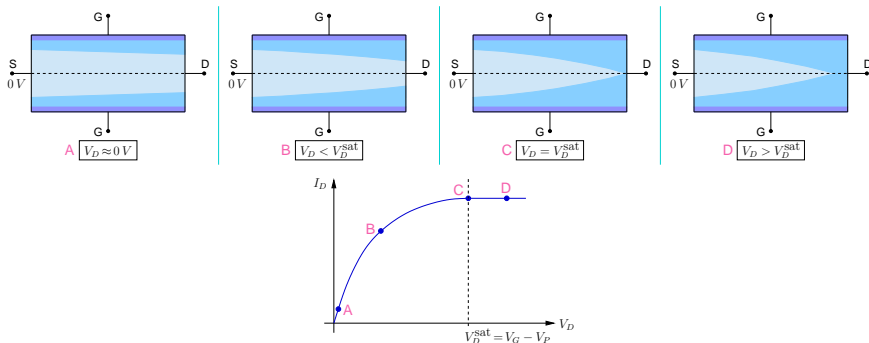
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Because the high-field region is confined to a very small distance, the conditions in the device are almost identical in C and D.

\Rightarrow The current in case D is almost the same as that for case C.

JFET: saturation



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In this situation, i.e., $V_D > V_D^{\text{sat}}$, a *short* high-field region develops near the drain end, and the “excess” voltage, $V_D - V_D^{\text{sat}}$ drops across this region.

Because the high-field region is confined to a very small distance, the conditions in the device are almost identical in C and D.

\Rightarrow The current in case D is almost the same as that for case C.

The region $V_D > V_D^{\text{sat}}$ is therefore called the “saturation region.”

JFET: example

An n -channel silicon JFET has the following parameters (at $T = 300\text{ K}$): $a = 1.5\text{ }\mu\text{m}$, $L = 5\text{ }\mu\text{m}$, $Z = 50\text{ }\mu\text{m}$, $N_d = 2 \times 10^{15}\text{ cm}^{-3}$, $V_{bi} = 0.8\text{ V}$, $\mu_n = 300\text{ cm}^2/\text{V-sec}$.

- (a) What is the pinch-off voltage?
- (b) Write a program to generate I_D - V_D characteristics for $V_G = 0\text{ V}$, -0.5 V , -1 V , -1.5 V , -2 V .
- (c) For each of the above V_G values, compute V_D^{sat} , and show it on the I_D - V_D plot. The part of an I_D - V_D corresponding to $V_D < V_D^{\text{sat}}$ is called the “linear” region, and that corresponding to $V_D > V_D^{\text{sat}}$ is called the “saturation” region.

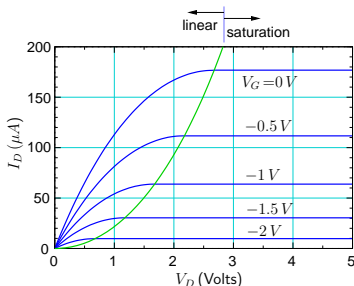
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Answer:

- (a) $V_P = -2.68\text{ V}$.
- (b)



JFET: simplified model for saturation

$$I_D = G_0 \left\{ V_D - \frac{2}{3} (V_{bi} - V_P) \left[\left(\frac{V_D + V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} \right] \right\}.$$

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At saturation, $V_D^{\text{sat}} = V_G - V_P$, giving

$$I_D^{\text{sat}} = G_0 \left\{ V_D - \frac{2}{3} (V_{bi} - V_P) \left[1 - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} \right] \right\}.$$

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The following approximate model is found to be adequate in circuit design:

$$I_D^{\text{sat}}(V_G) = I_{DSS} (1 - V_G/V_P)^2, \text{ where } I_{DSS} = I_D^{\text{sat}}(V_G = 0 \text{ V}).$$

JFET: simplified model for saturation

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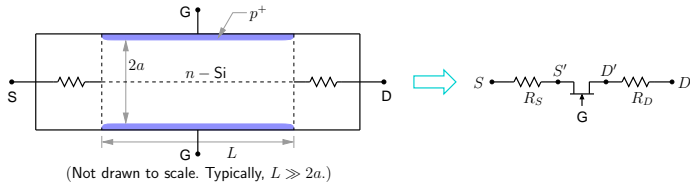
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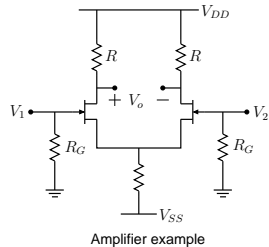
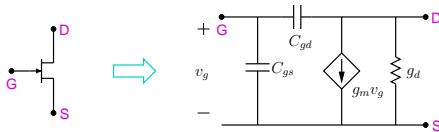
$$\text{where } g_{m0} = -2I_{DSS}/V_P = g_m(V_G = 0 \text{ V}).$$

JFET: source/drain resistances



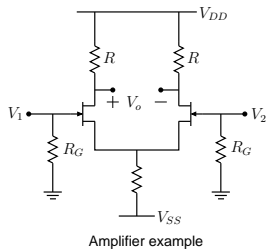
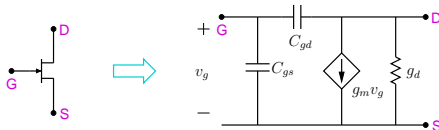
Cross-sectional view

JFET: small-signal model



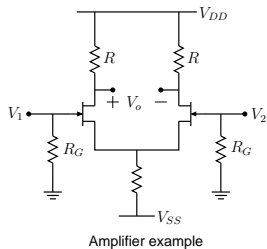
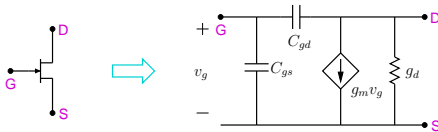
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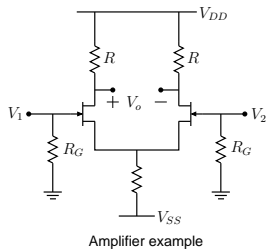
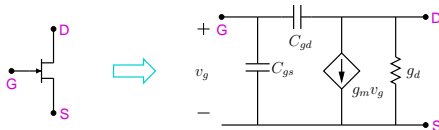
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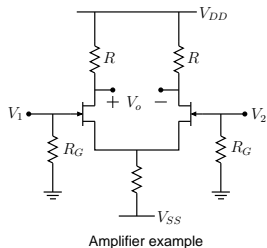
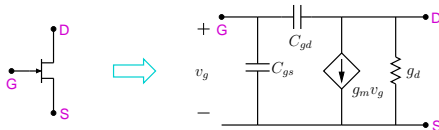
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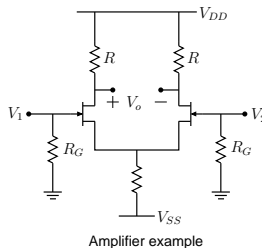
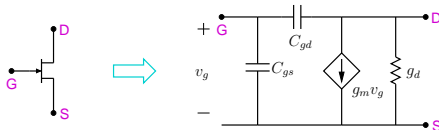
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