EE101: JFET operation and characteristics

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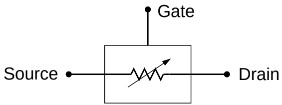
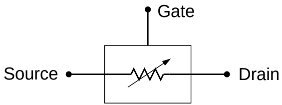
Field-effect transistors





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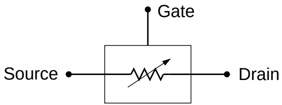

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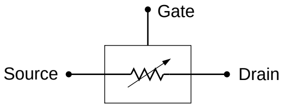
* In simple terms, a FET can be thought of as a resistance connected between S and D, which is a function of the gate voltage V_G.



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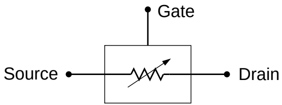

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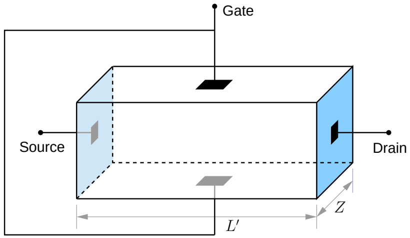
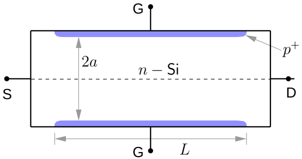
* The mechanism of gate control varies in different types of FETs, e.g., JFET, MESFET, MOSFET, HEMT.
* FETs can be used for analog and digital applications. In each case, the fact that the gate is used to control current flow between S and D plays a crucial role.

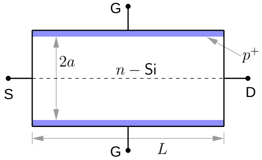


3D view



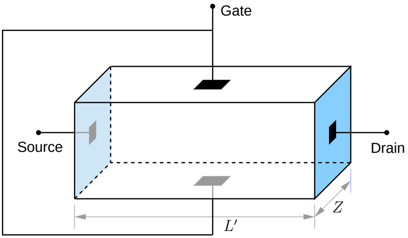
(Not drawn to scale. Typically, $L \gg 2a$.)

Cross−sectional view



Simplified structure

Junction Field-effect transistors (JFET)



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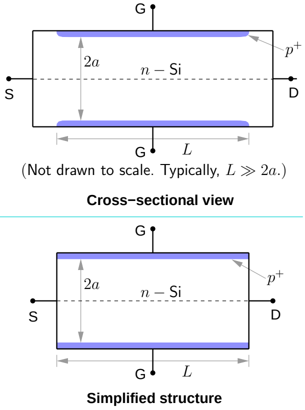
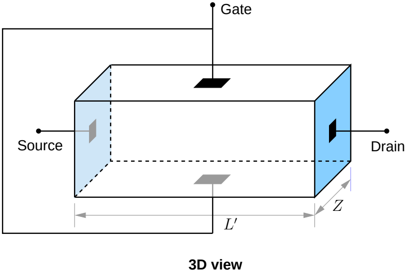
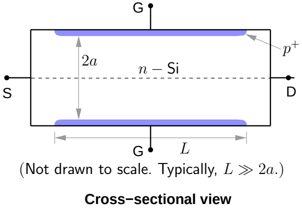
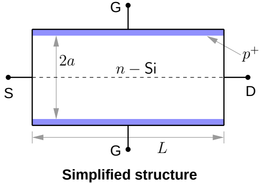


* The n-type region between the top and bottom p^+ regions offers a resistance to current flow. The resistance depends on V_G.

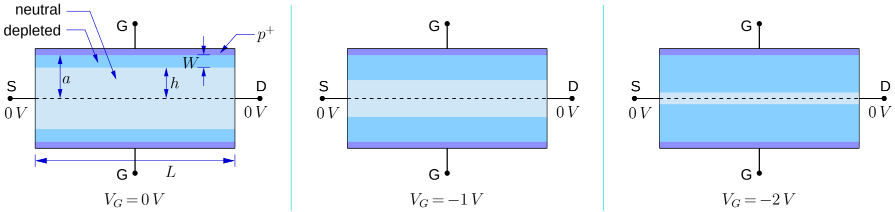






* The n-type region between the top and bottom p^+ regions offers a resistance to current flow. The resistance depends on V_G.
* We will first consider the case, $V_D = V_S = 0\ V$.

JFET with $V_S = V_D = 0\ V$



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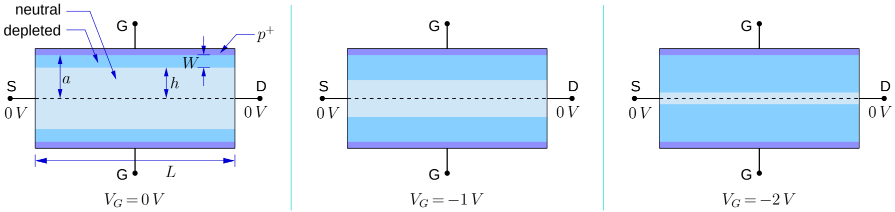
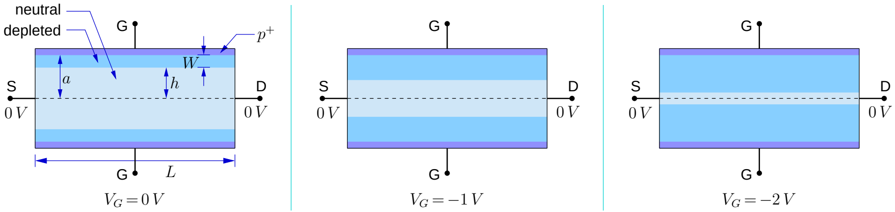


* The bias across the *p*-*n* junction is $(V_G - V_S)$, i.e., V_G, since $V_S = V_D = 0\ V$.



* The bias across the *p*-*n* junction is $(V_G - V_S)$, i.e., V_G, since $V_S = V_D = 0\ V$.
* As the reverse bias across the junction is increased (by making V_G more negative), the depletion region widens, and the resistance offered by the *n*-region increases.

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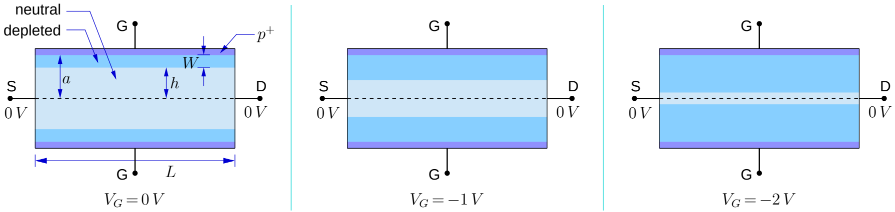
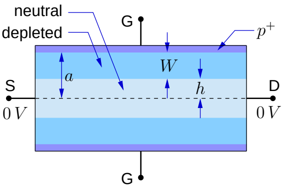
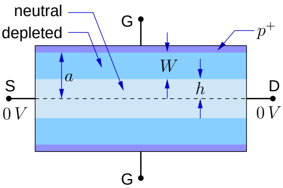


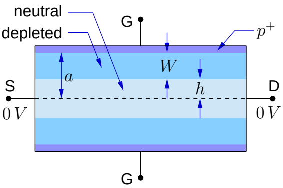
* The bias across the p-n junction is $(V_G - V_S)$, i.e., V_G, since $V_S = V_D = 0\ V$.
* As the reverse bias across the junction is increased (by making V_G more negative), the depletion region widens, and the resistance offered by the n-region increases.
* When the reverse bias becomes large enough, the depletion region consumes the entire n-region. The corresponding V_G is called the "pinch-off" voltage.

JFET: pinch-off voltage



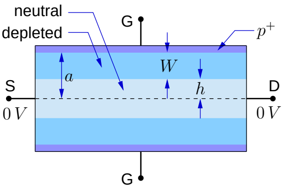


* $V_P = V_G$ for which $h = 0$, i.e., $W = a$.



* $V_P = V_G$ for which $h = 0$, i.e., $W = a$.
* For a p^+-n junction, $W = \sqrt{\dfrac{2\,\epsilon\,(V_{\text{bi}} - V)}{q\,N_d}}$, where V_{bi} is the built-in potential of the junction.

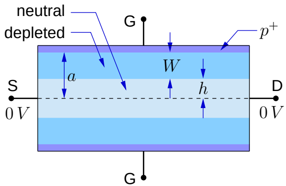
JFET: pinch-off voltage



- $V_P = V_G$ for which $h = 0$, i.e., $W = a$.
- For a p^+-n junction, $W = \sqrt{\dfrac{2\,\epsilon\,(V_{bi} - V)}{q\,N_d}}$, where V_{bi} is the built-in potential of the junction.
- For pinch-off, $W = a = \sqrt{\dfrac{2\,\epsilon\,(V_{bi} - V)}{q\,N_d}}$

$$\Rightarrow V_P = V_{bi} - \frac{q\,N_d\,a^2}{2\,\epsilon}\,.$$

JFET: pinch-off voltage



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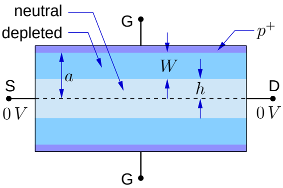

$*$ For pinch-off, $W = a = \sqrt{\dfrac{2\,\epsilon\,(V_{\text{bi}} - V)}{q\,N_d}} \Rightarrow V_P = V_{\text{bi}} - \dfrac{q\,N_d\,a^2}{2\,\epsilon}\,.$

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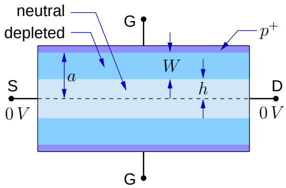
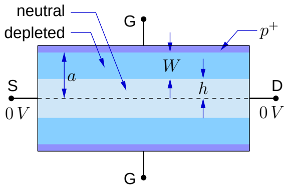


* For pinch-off, $W = a = \sqrt{\dfrac{2\,\epsilon\,(V_{\rm bi} - V)}{q\,N_d}} \Rightarrow V_P = V_{\rm bi} - \dfrac{q\,N_d\,a^2}{2\,\epsilon}$.
* Example: $N_d = 2 \times 10^{15}\,{\rm cm}^{-3}$, $a = 1.5\,\mu{\rm m}$, $V_{\rm bi} = 0.8\,V$.



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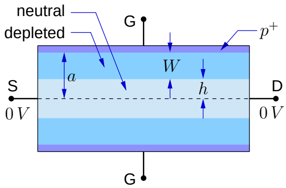
* Example: $N_d = 2 \times 10^{15}\,\text{cm}^{-3}$, $a = 1.5\,\mu\text{m}$, $V_{bi} = 0.8\,V$.

$$W = 0.8 - \frac{(1.6 \times 10^{-19}\,\text{Coul})(2 \times 10^{15}\,\text{cm}^{-3})((1.5 \times 10^{-4})^2\,\text{cm}^2)}{2 \times 11.7 \times 8.85 \times 10^{-14}\,F/\text{cm}}$$

$$= 0.8 - 3.48 \approx -2.7\,V\,.$$



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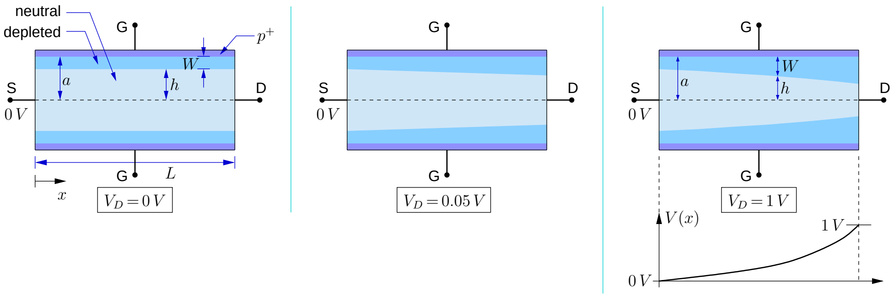
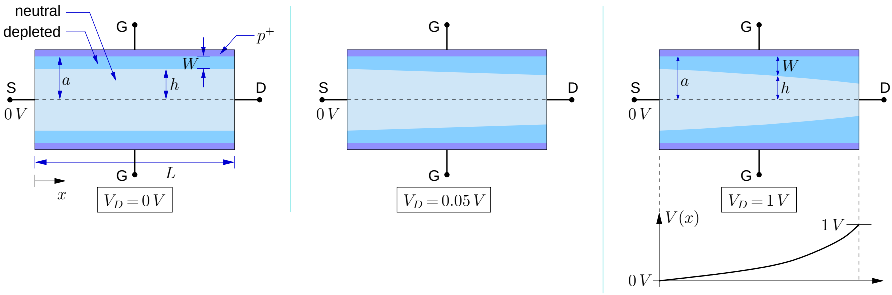
$\Rightarrow$ If a gate voltage $V_G = -2.7\,V$ is applied, the n-channel gets pinched off, and the device resistance becomes very large.

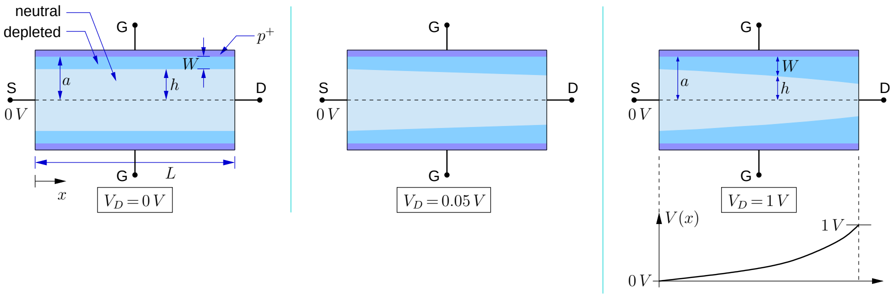
JFET with $V_G =$ constant, $V_D \neq 0\ V$



JFET with $V_G = \text{constant}$, $V_D \neq 0\ V$

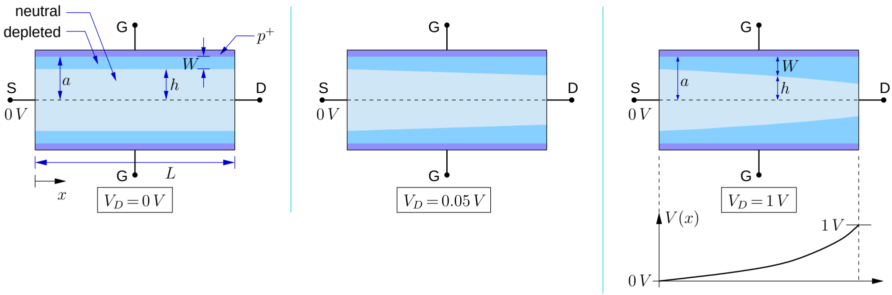


* Consider an *n*-JFET with V_G constant (and not in pinch-off mode).



* Consider an n-JFET with V_G constant (and not in pinch-off mode).
  If a positive V_D is applied, the potential $V(x)$ inside the channel from S to D (along the dashed line) increases from $0\,V$ to V_D.

JFET with $V_G = \text{constant}$, $V_D \neq 0\ V$



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  Note that W and h are now functions of x such that, $W(x) + h(x) = a$.

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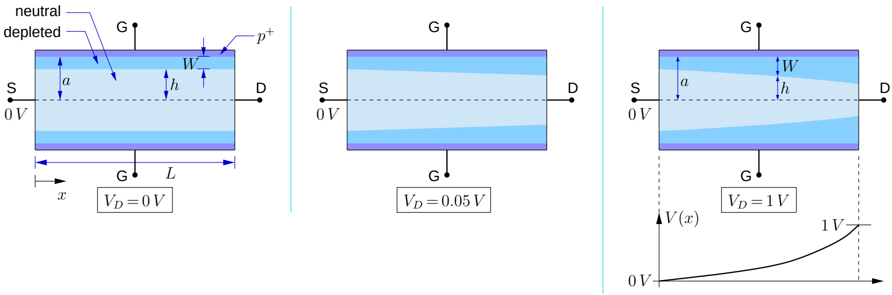

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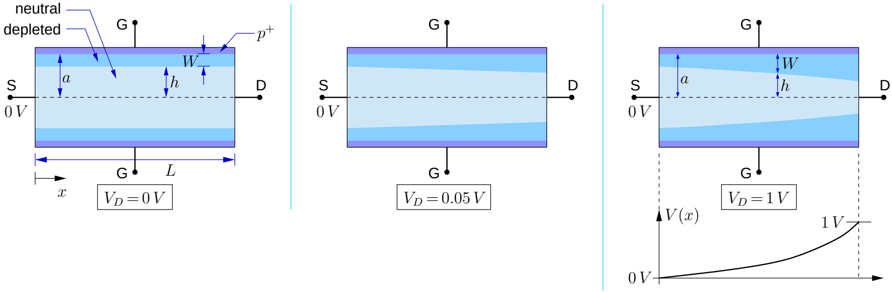
  Note that W and h are now functions of x such that, $W(x) + h(x) = a$.
* Since the *p*-*n* junction bias at a given x is $(V_G - V(x))$, the drain end of the channel has a larger reverse bias than the source end.

JFET with $V_G =$ constant, $V_D \neq 0\ V$



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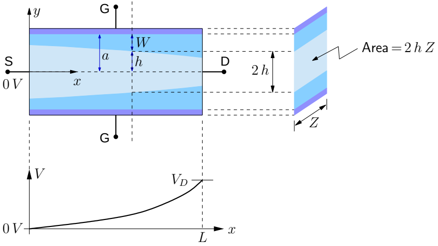
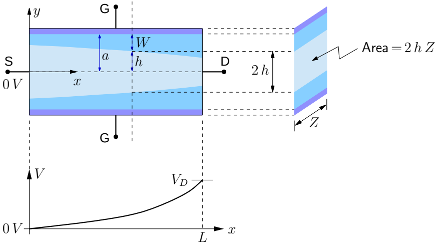
  Note that W and h are now functions of x such that, $W(x) + h(x) = a$.
* Since the p-n junction bias at a given x is $(V_G - V(x))$, the drain end of the channel has a larger reverse bias than the source end.
  $\Rightarrow$ the depletion region is wider at the drain.

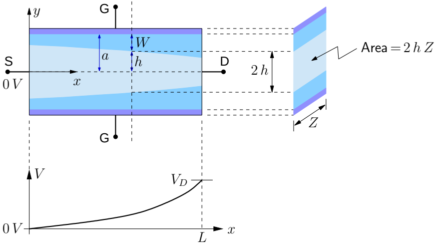
JFET: derivation of I_D equation





Consider a slice of the device. The current density at any point in the neutral region is assumed to be in the x direction, and given by,

$$J_n = q\mu_n nE + qD_n \frac{dn}{dx} \approx q\mu_n nE = q\mu_n N_d \frac{dV}{dx} \ ,$$



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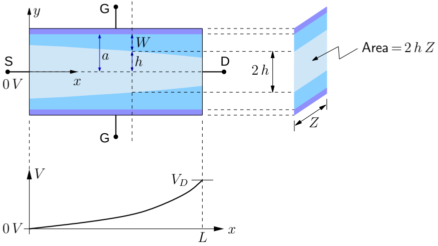

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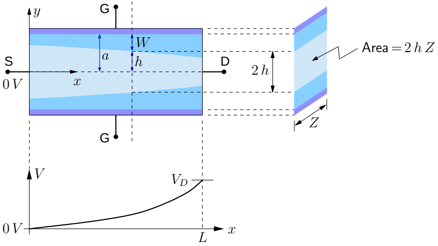
Note that only the neutral part of the n-Si conducts since there are no carriers in the depletion regions.



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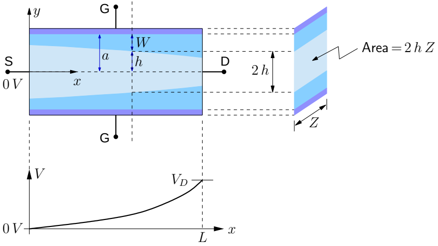
At a given x, the current I_D is obtained by integrating J_n over the area of the neutral channel region (see figure on the right). Since J_n is constant over this area,



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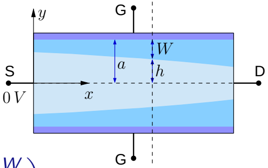
At a given x, the current I_D is obtained by integrating J_n over the area of the neutral channel region (see figure on the right). Since J_n is constant over this area,

$$I_D(x) = \iint J_n dx\, dz = 2hZ \times \left(q\mu_n N_d \frac{dV}{dx} \right) = 2qZ\mu_n N_d a \frac{dV}{dx} \left(1 - \frac{W}{a} \right) ,$$

where we have used $h = a - W$, i.e., $h = a(1 - W/a)$.

JFET: derivation of I_D equation



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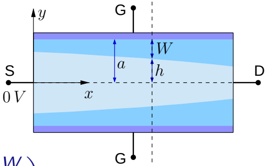


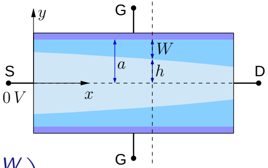
$$I_D(x) = 2\,q\,Z\,\mu_n\,N_d\,a\,\frac{dV}{dx}\,\left(1 - \frac{W}{a}\right).$$

Since $I_D(x)$ is constant from $x=0$ to $x=L$, we get,

$$\int_0^L I_D\,dx = I_D L = 2qZ\mu_n N_d a \int_0^{V_D} \left(1 - \sqrt{\frac{2\epsilon}{qN_d a^2}}\sqrt{V_{\mathrm{bi}} - (V_G - V)}\right) dV,$$

where we have used, for the depletion width W,

$$W(x) = \sqrt{\frac{2\epsilon}{qN_d}\left[V_{\mathrm{bi}} - (V_G - V)\right]}\,.$$



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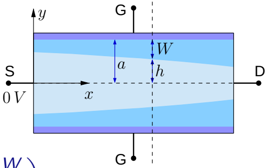
where we have used, for the depletion width W,

$$W(x) = \sqrt{\frac{2\epsilon}{qN_d}\left[V_{\rm bi}-(V_G-V)\right]}.$$

Evaluating the integral and using $V_{\rm bi}-V_P = \dfrac{qN_d a^2}{2\epsilon}$, we get (do this!)

$$I_D = G_0\left\{V_D-\frac{2}{3}(V_{\rm bi}-V_P)\left[\left(\frac{V_D+V_{\rm bi}-V_G}{V_{\rm bi}-V_P}\right)^{3/2}-\left(\frac{V_{\rm bi}-V_G}{V_{\rm bi}-V_P}\right)^{3/2}\right]\right\},$$

where $G_0 = 2qZ\mu_n N_d a/L$.



$$I_D(x) = 2\,q\,Z\,\mu_n\,N_d\,a\frac{dV}{dx}\left(1-\frac{W}{a}\right).$$

Since $I_D(x)$ is constant from $x=0$ to $x=L$, we get,

$$\int_0^L I_D\,dx = I_D L = 2qZ\mu_n N_d a\int_0^{V_D}\left(1-\sqrt{\frac{2\epsilon}{qN_d a^2}}\sqrt{V_{\mathrm{bi}}-(V_G-V)}\right)dV,$$

where we have used, for the depletion width W,

$$W(x) = \sqrt{\frac{2\epsilon}{qN_d}\left[V_{\mathrm{bi}}-(V_G-V)\right]}.$$

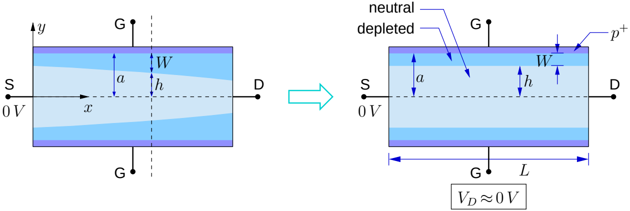
Evaluating the integral and using $V_{\mathrm{bi}} - V_P = \dfrac{qN_d a^2}{2\epsilon}$, we get (do this!)

$$I_D = G_0\left\{V_D - \frac{2}{3}(V_{\mathrm{bi}}-V_P)\left[\left(\frac{V_D+V_{\mathrm{bi}}-V_G}{V_{\mathrm{bi}}-V_P}\right)^{3/2} - \left(\frac{V_{\mathrm{bi}}-V_G}{V_{\mathrm{bi}}-V_P}\right)^{3/2}\right]\right\},$$

where $G_0 = 2qZ\mu_n N_d a/L$.

Note that G_0 is the channel conductance if there was no depletion, i.e., if $h(x)=a$ throughout the channel.

Special case: $V_D \approx 0\ V$



$$I_D = G_0 \left\{ V_D - \frac{2}{3}(V_{bi} - V_P) \left[\left(\frac{V_D + V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} \right] \right\}$$

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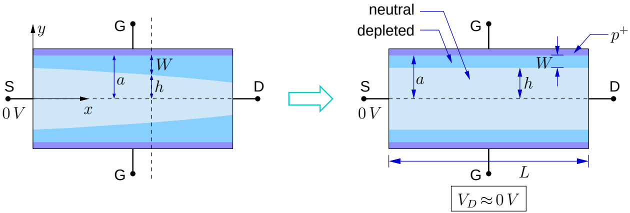
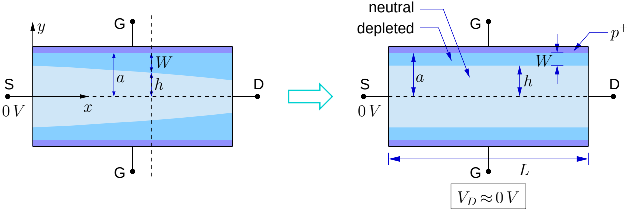


$$
\begin{aligned}
I_D &= G_0 \left\{ V_D - \frac{2}{3}\left(V_{\rm bi} - V_P\right) \left[\left(\frac{V_D + V_{\rm bi} - V_G}{V_{\rm bi} - V_P} \right)^{3/2} - \left(\frac{V_{\rm bi} - V_G}{V_{\rm bi} - V_P} \right)^{3/2} \right] \right\} \\
&\approx G_0 \left\{ V_D - \frac{2}{3}\left(V_{\rm bi} - V_P\right)^{-1/2} \left[\frac{3}{2}\, V_D \,\left(V_{\rm bi} - V_G\right)^{1/2} \right] \right\} \quad \text{(using Taylor's series)}
\end{aligned}
$$

Special case: $V_D \approx 0\ V$



$$I_D = G_0 \left\{ V_D - \frac{2}{3}(V_{\rm bi} - V_P)\left[\left(\frac{V_D + V_{\rm bi} - V_G}{V_{\rm bi} - V_P}\right)^{3/2} - \left(\frac{V_{\rm bi} - V_G}{V_{\rm bi} - V_P}\right)^{3/2}\right]\right\}$$

$$\approx G_0 \left\{ V_D - \frac{2}{3}(V_{\rm bi} - V_P)^{-1/2}\left[\frac{3}{2} V_D\,(V_{\rm bi} - V_G)^{1/2}\right]\right\} \quad \text{(using Taylor's series)}$$

$$= G_0\, V_D \left\{ 1 - \left(\frac{V_{\rm bi} - V_G}{V_{\rm bi} - V_P}\right)^{1/2}\right\}.$$

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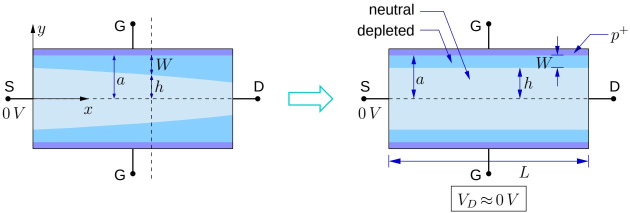

$$I_D = G_0 \left\{ V_D - \frac{2}{3}(V_{bi} - V_P)\left[\left(\frac{V_D + V_{bi} - V_G}{V_{bi} - V_P}\right)^{3/2} - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P}\right)^{3/2}\right]\right\}$$

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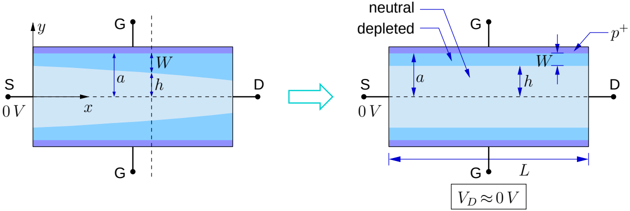
$$= G_0\, V_D \left\{ 1 - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P}\right)^{1/2}\right\}.$$

Since $W = \frac{2\epsilon}{qN_d}(V_{bi} - V_G)^{1/2}$, and $a = \frac{2\epsilon}{qN_d}(V_{bi} - V_P)^{1/2}$, we get

Special case: $V_D \approx 0\ V$



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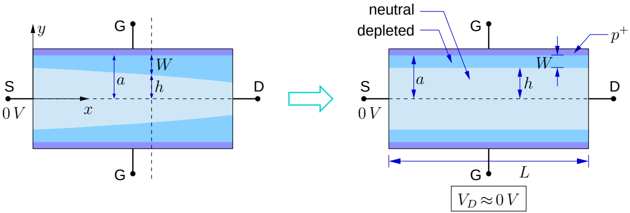

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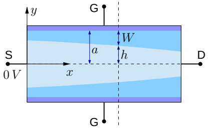
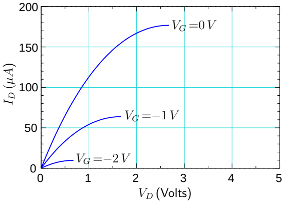
Since $W = \frac{2\epsilon}{qN_d}(V_{bi} - V_G)^{1/2}$, and $a = \frac{2\epsilon}{qN_d}(V_{bi} - V_P)^{1/2}$, we get

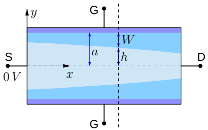
$$I_D = G_0 V_D \left\{ 1 - \frac{W}{a} \right\}.$$

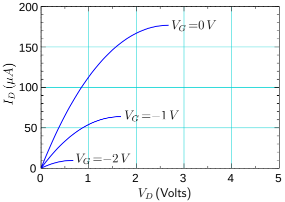
This simply shows that the channel conductance reduces linearly with W (as seen before the $V_S = V_S = 0\ V$ condition), and for $V_G = V_P$ (i.e., $W = a$), the conductance becomes zero.





$$I_D = G_0 \left\{ V_D - \frac{2}{3}\left(V_{\rm bi} - V_P\right) \left[\left(\frac{V_D + V_{\rm bi} - V_G}{V_{\rm bi} - V_P} \right)^{3/2} - \left(\frac{V_{\rm bi} - V_G}{V_{\rm bi} - V_P} \right)^{3/2} \right] \right\}.$$

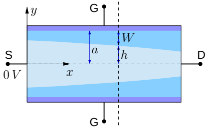


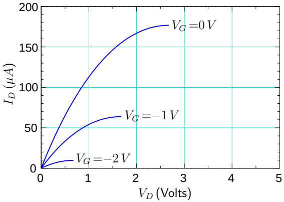


$$I_D = G_0 \left\{ V_D - \frac{2}{3}\left(V_{bi} - V_P\right)\left[\left(\frac{V_D + V_{bi} - V_G}{V_{bi} - V_P}\right)^{3/2} - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P}\right)^{3/2}\right]\right\}.$$

For a given V_G, I_D reaches a maximum at $V_D = V_G - V_P$ (show this by differentiating the above equation).

JFET: pinch-off near drain





$$I_D = G_0 \left\{ V_D - \frac{2}{3} (V_{bi} - V_P) \left[\left(\frac{V_D + V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} \right] \right\}.$$

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At this value of V_D, the bias across the p-n junction at the drain end is $V_G - V_D = V_P$.

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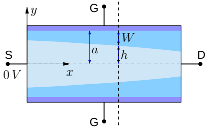

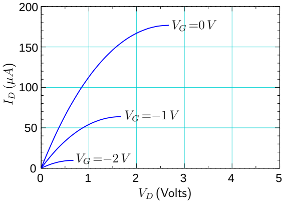

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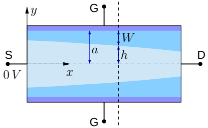
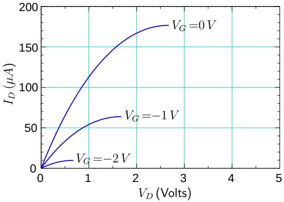
At this value of V_D, the bias across the *p*-*n* junction at the drain end is $V_G - V_D = V_P$.
In other words, the drain end of the channel has *just* reached pinch-off.





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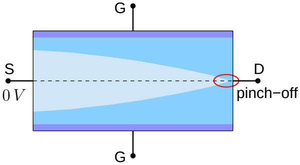

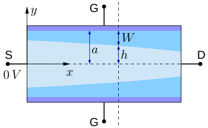

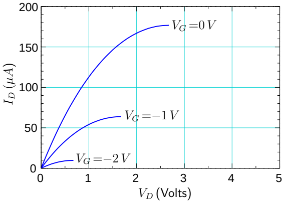

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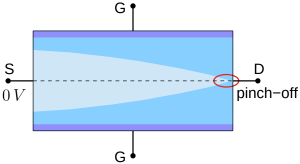
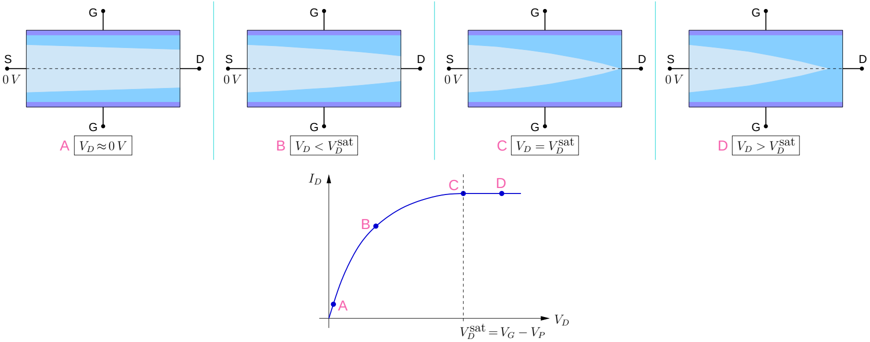


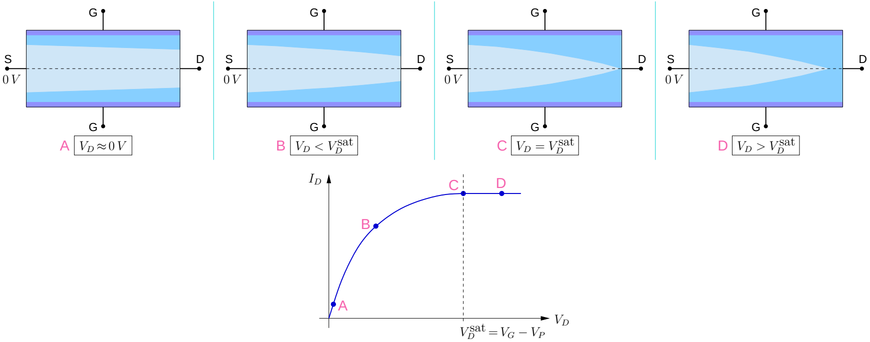
What happens if V_D is increased further?

JFET: saturation



Consider a fixed V_G with V_D varying from $\sim 0\ V$ to a value beyond condition C.

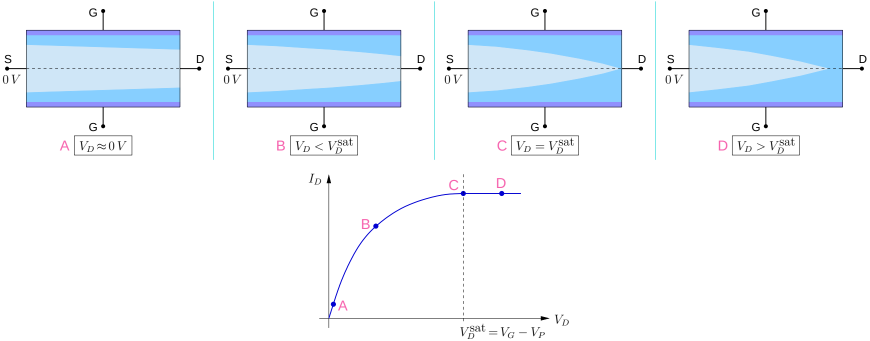
JFET: saturation



Consider a fixed V_G with V_D varying from $\sim 0\ V$ to a value beyond condition C.

In this situation, i.e., $V_D > V_D^{\text{sat}}$, a *short* high-field region develops near the drain end, and the "excess" voltage, $V_D - V_D^{\text{sat}}$ drops across this region.

JFET: saturation



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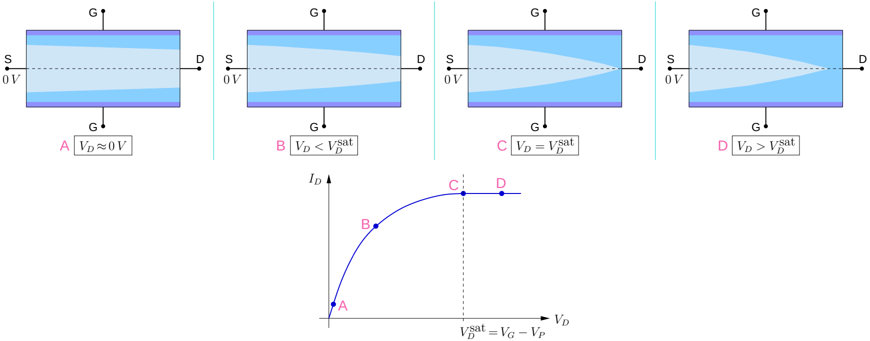
Because the high-filed region is confined to a very small distance, the conditions in the device are almost identical in C and D.

JFET: saturation



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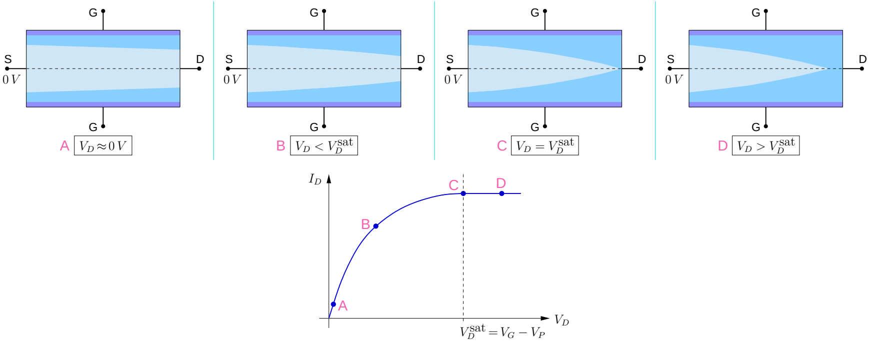
Because the high-filed region is confined to a very small distance, the conditions in the device are almost identical in C and D.

$\Rightarrow$ The current in case D is almost the same as that for case C.



Consider a fixed V_G with V_D varying from $\sim 0\ V$ to a value beyond condition C.

In this situation, i.e., $V_D > V_D^{\rm sat}$, a *short* high-field region develops near the drain end, and the "excess" voltage, $V_D - V_D^{\rm sat}$ drops across this region.

Because the high-filed region is confined to a very small distance, the conditions in the device are almost identical in C and D.

$\Rightarrow$ The current in case D is almost the same as that for case C.

The region $V_D > V_D^{\rm sat}$ is therefore called the "saturation region."

JFET: example

An n-channel silicon JFET has the following parameters (at $T = 300\,K$): $a = 1.5\,\mu$m, $L = 5\,\mu$m, $Z = 50\,\mu$m, $N_d = 2 \times 10^{15}\,\text{cm}^{-3}$, $V_{\text{bi}} = 0.8\,V$, $\mu_n = 300\,\text{cm}^2/V$-sec.

(a) What is the pinch-off voltage?

(b) Write a program to generate I_D-V_D characteristics for $V_G = 0\,V$, $-0.5\,V$, $-1\,V$, $-1.5\,V$, $-2\,V$.

(c) For each of the above V_G values, compute V_D^{sat}, and show it on the I_D-V_D plot. The part of an I_D-V_D corresponding to $V_D < V_D^{\text{sat}}$ is called the "linear" region, and that corresponding to $V_D > V_D^{\text{sat}}$ is called the "saturation" region.

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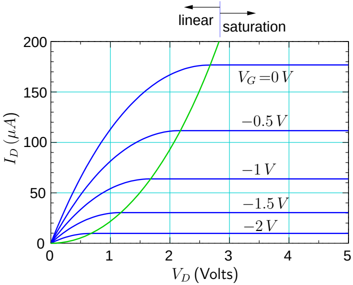
Answer:

(a) $V_P = -2.68\,V$.

(b)



JFET: simplified model for saturation

$$I_D = G_0 \left\{ V_D - \frac{2}{3}\left(V_{\text{bi}} - V_P\right)\left[\left(\frac{V_D + V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P}\right)^{3/2} - \left(\frac{V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P}\right)^{3/2}\right]\right\}.$$

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At saturtation, $V_D^{\text{sat}} = V_G - V_P$, giving

$$I_D^{\text{sat}} = G_0 \left\{ V_D - \frac{2}{3}\left(V_{\text{bi}} - V_P\right)\left[1 - \left(\frac{V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P}\right)^{3/2}\right]\right\}.$$

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The following approximate model is found to be adequate in circuit design:

$I_D^{\text{sat}}(V_G) = I_{DSS}\,(1 - V_G/V_P)^2$, where $I_{DSS} = I_D^{\text{sat}}(V_G = 0\ V)$.

JFET: simplified model for saturation

$$I_D = G_0 \left\{ V_D - \frac{2}{3}\,(V_{\text{bi}} - V_P) \left[\left(\frac{V_D + V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P} \right)^{3/2} - \left(\frac{V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P} \right)^{3/2} \right] \right\}.$$

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$$I_D^{\text{sat}} = G_0 \left\{ V_D - \frac{2}{3}\,(V_{\text{bi}} - V_P) \left[1 - \left(\frac{V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P} \right)^{3/2} \right] \right\}.$$

The following approximate model is found to be adequate in circuit design:

$I_D^{\text{sat}}(V_G) = I_{DSS}\,(1 - V_G/V_P)^2$, where $I_{DSS} = I_D^{\text{sat}}(V_G = 0\ V)$.

In amplifier design, we are interested in $g_m = \left.\dfrac{\partial I_D}{\partial V_G}\right|_{V_D=\text{constant}}$, which is obtained as:

JFET: simplified model for saturation

$$I_D = G_0 \left\{ V_D - \frac{2}{3}\,(V_{\rm bi} - V_P) \left[\left(\frac{V_D + V_{\rm bi} - V_G}{V_{\rm bi} - V_P} \right)^{3/2} - \left(\frac{V_{\rm bi} - V_G}{V_{\rm bi} - V_P} \right)^{3/2} \right] \right\}.$$

At saturtation, $V_D^{\rm sat} = V_G - V_P$, giving

$$I_D^{\rm sat} = G_0 \left\{ V_D - \frac{2}{3}\,(V_{\rm bi} - V_P) \left[1 - \left(\frac{V_{\rm bi} - V_G}{V_{\rm bi} - V_P} \right)^{3/2} \right] \right\}.$$

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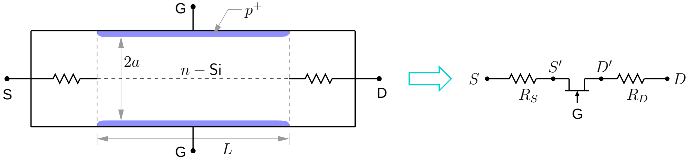
$g_m = g_{m0}\,(1 - V_G/V_P)$,

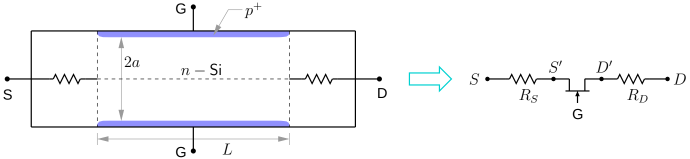
where $g_{m0} = -2I_{DSS}/V_P = g_m(V_G = 0\ V)$.

JFET: source/drain resistances



(Not drawn to scale. Typically, $L \gg 2a$.)

Cross−sectional view

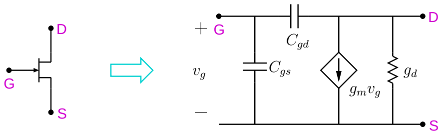


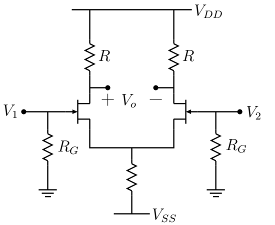
(Not drawn to scale. Typically, $L \gg 2a$.)

Cross−sectional view

In real JFETs, there is a separation between the source/drain contacts and the active channel.

The *n*-type semiconductor regions between the active channel and the source/drain contacts can be modelled by resistances R_S and R_D.

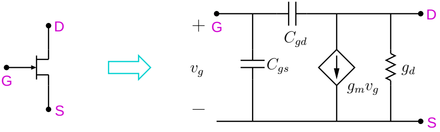


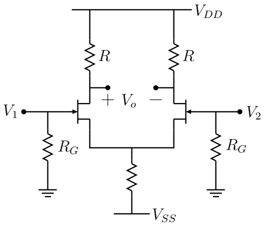


Amplifier example

* A small-signal model of a JFET is required in analysis of an amplifier.

JFET: small-signal model





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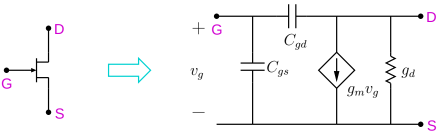
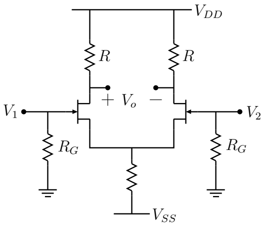
* The DC gate current, which is the reverse current of a *p-n* junction, is generally insignificant and is therefore ignored.





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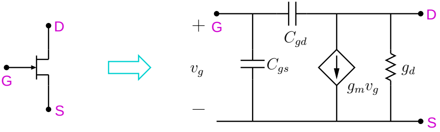

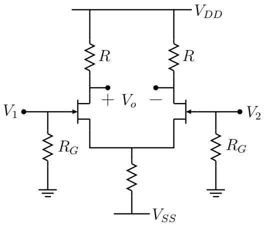

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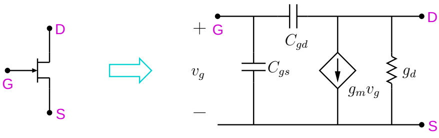

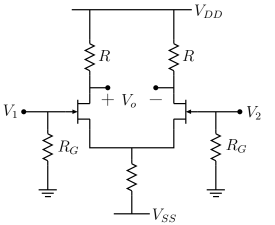

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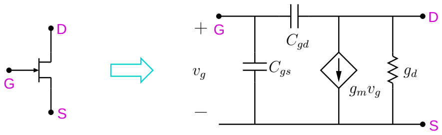
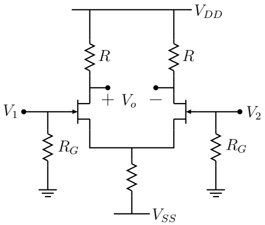
* g_m and g_d can be obtained by differentiating $I_D(V_G, V_D)$. Note that, in our simple model, short-channel effects have not been included; we would therefore obtain $g_d = 0\,\mho$ in saturation. However, a real device would show a small increase in I_D with an increase in V_D in saturation, giving rise to a non-zero g_d.

JFET: small-signal model





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* The capacitances C_{gs} and C_{gd} are depletion capacitances of the *p*-*n* junction.