Current Mode Interconnect

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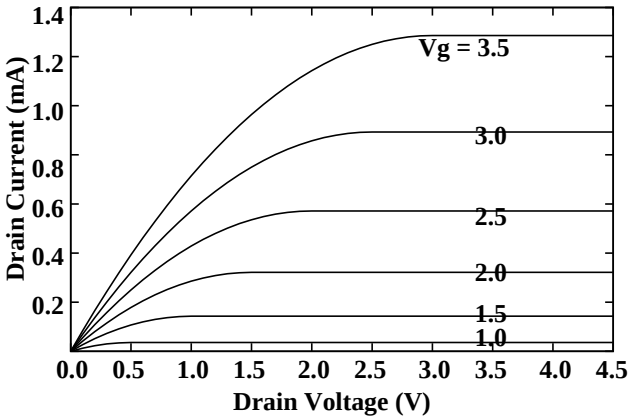
Scaling

- To increase packing density, we would like to reduce the size of transistors and passive components.
- In order to decrease lateral sizes, we have to reduce vertical sizes too.
- If dimensions are scaled down, voltages must also be reduced to avoid breakdown.

This is known as constant field scaling.

So what price do we have to pay to get denser, more complex circuits?

MOS model



$$K \equiv \mu C_{ox} \frac{W}{L}$$

$$C_{ox} \equiv \frac{\epsilon_{ox}}{t_{ox}}$$

(Gate capacitance C_{ox} is *per unit area*)

- For $V_{gs} \leq V_T$,
  $I_{ds} = 0$
- For $V_{gs} > V_T$ and $V_{ds} \leq V_{gs} - V_T$,
  $I_{ds} = K\left[(V_{gs} - V_T)V_{ds} - \frac{1}{2}V_{ds}^2\right]$
- For $V_{gs} > V_T$ and $V_{ds} > V_{gs} - V_T$,
  $I_{ds} = \frac{K}{2}(V_{gs} - V_T)^2$

Consequences of Scaling

All dimensions and voltages divided by the factor S(>1).

Device area	$\propto W \times L : (\downarrow S)(\downarrow S)$	$\downarrow S^2$
C_{ox}	ϵ_{ox}/t_{ox} : const$/(\downarrow S)$	$\uparrow S$
C_{total}	$\epsilon A/t : (\downarrow S^2)/(\downarrow S)$	$\downarrow S$
V_{DS}, V_{GS}, V_T	Voltages : $(\downarrow S)$	$\downarrow S$
I_d	$\mu C_{ox}(W/L)(\propto V^2)$: $(\uparrow S)(\text{const})(\downarrow S^2)$	$\downarrow S$
Slew Rate $\frac{dV}{dt}$	$I/C_{total} : (\downarrow S)/(\downarrow S)$	$const.$
Delay	$V/\frac{dV}{dt} : (\downarrow S)/(const)$	$\downarrow S$
Static Power	$V \times I : (\downarrow S)(\downarrow S)$	$\downarrow S^2$
dynamic power	$C_{total}V^2 f : (\downarrow S)(\downarrow S^2)(\uparrow S)$	$\downarrow S^2$
Power delay product	delay $\times$ power$(\downarrow S)(\downarrow S^2)$	$\downarrow S^3$
Power density	power/area : $(\downarrow S^2)/(\downarrow S^2)$	$const.$

Impact of scaling

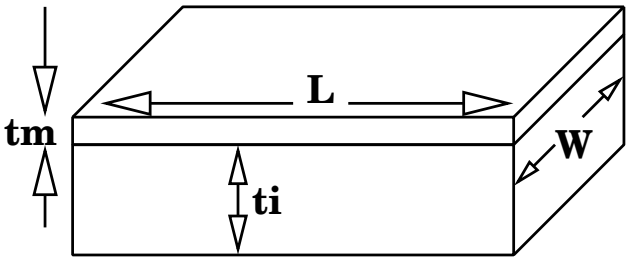
- Improved packing density: $\uparrow S^2$
- Improved speed: delay $\downarrow S$
- Improved power consumption: $\downarrow S^2$

However . . .
The above improvements apply to active circuits.

What about passive components?

Also, reduced voltages imply a lower signal to noise ratio.

Concern: Interconnect Delay

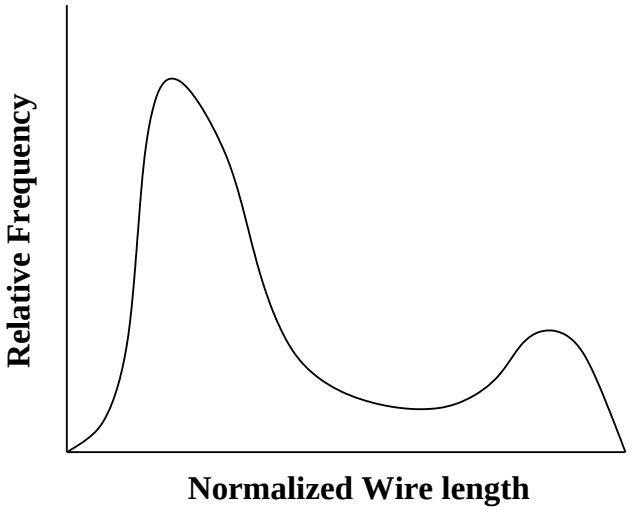


$$R = \rho \frac{L}{W t_m}, \qquad C = \epsilon \frac{LW}{t_i}$$

$$\text{Charge Time} \approx RC = \rho\epsilon \frac{L^2}{t_m t_i}$$

- Delay is independent of W. This is because increasing W reduces resistance but increses capacitance in the same ratio.
- Unfortunately W is the only parameter that the circuit designer can decide! (L is fixed by the distance between the points to be connected, ρ, ϵ, t_m and t_i are decided by the technology).

Concern: Interconnect Delay



- Local interconnects scale with device size.
- Global interconnects scale with die size.

Interconnect Delay = $\frac{\rho\epsilon}{t_m t_i} L^2 = AL^2$
For local interconnects, L scales the same way as t_m, t_i, so delay is invariant.

For Global Interconnects, L goes *up* with die size, while t_m and t_i scale down. This leads to a sharp increase in delay.

Buffer Insertion

Global Interconnect delay can be the determining factor for the speed of an integrated system.

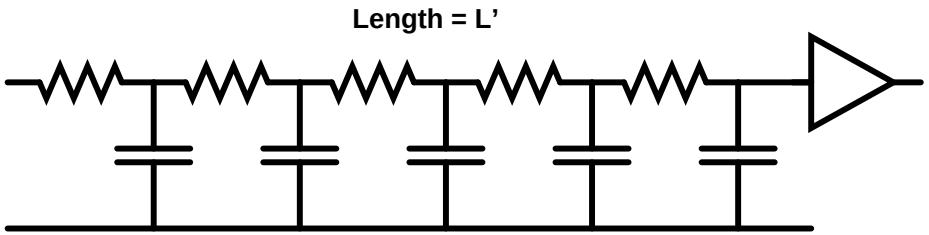
The L^2 dependence of interconnect delay is a source of particular concern.

This problem can be somewhat mitigated by buffer insertion in long wires.

We define some critical wire length and when a wire segment exceeds this length, we insert a buffer.

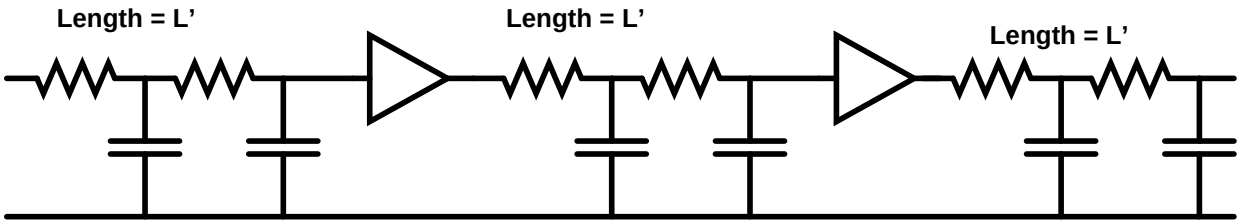
Optimal Repeater Insertion

We know that Wire Delay = $\rho\epsilon\frac{L^2}{t_m t_i} \simeq AL^2$
Suppose we insert a buffer after every wire segment length = L'.



Then Segment wire delay = AL'^2.
Let buffer delay = τ
For a total wire length of L, (assumed to be a multiple of L')
let n = L/L'
The wire will have n segments, with n-1 buffers.

Optimal Repeater Insertion



What is the optimum wire segment length L'?

$$\Delta = nAL'^2 + (n-1)\tau = \frac{L}{L'}AL'^2 + (\frac{L}{L'} - 1)\tau = ALL' + (\frac{L}{L'} - 1)\tau$$

Putting the derivative with respect to L' = 0 for optimisation,

$$AL - \frac{L}{L'^2}\tau = 0, \text{ so } AL'^2 = \tau$$

L' should be so chosen that the wire segment delay = τ.
Total delay is proportional to n and so, is linear in L.

Concern: Signal Integrity

As interconnect wire separation is reduced . . .

- There is a serious signal integrity problem because of electrostatic coupling between long wires.
- Inter-signal interference can lead to unpredictable delay variations.
- Grounded shielding wires must often be inserted to avoid interference.
- This leads to extra capacitance and CV^2f power loss.

Concern: Timing closure

- Global interconnects are placed *after* active circuit design and layout is complete.
- One has to anticipate the wire length, and then design the active circuits to meet total delay specifications.
- If the actual wire length is different from what was anticipated, one has to re-design the active circuits after layout.
- After a fresh layout, wire lengths and hence, delays are changed.
- This leads to a design-layout-redesign iteration known as Timing Closure. This iteration becomes longer and longer when total delays are dominated by interconnect delay.

Promise of current signaling

- Why not signal with current rather than voltage?
- Current rise time is limited by inductance rather than capacitance. Typically, inductive effects are much smaller than capacitive effects. (After all, $\epsilon \simeq 4, \mu = 1$ for insulators used in IC's). So electromagnetic coupling is lower than electrostatic coupling.
- Signal voltage swings are limited by scaled down supply voltages: this does not restrict current swings.
- In fact, we can use multiple current values to send more than one bit down the same wire!

A mixed mode circuit for Interconnects

If we hold the Voltage on the interconnect fixed
$\Delta V = 0$, while $\Delta I \neq 0 \Rightarrow$ Need low (near 0) input impedance receiver

- No voltage swing on the wire,
  $\Rightarrow$ **Dynamic power is negligible.**

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  $\Rightarrow$ **Higher Throughput.**
  $\Rightarrow$ **Lower interconnect area.**

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- Multiple current levels to transmit bits simultaneously
  $\Rightarrow$ **Higher Throughput.**
  $\Rightarrow$ **Lower interconnect area.**
- Advantages in Latency, Throughput and Power simultaneously!

Operation

Two Bit Four Level Current Interconnect System

- Four current levels used to signal two bits.
- Trade off between Signal to Noise Ratio and Power.
- No changes in rest of system design

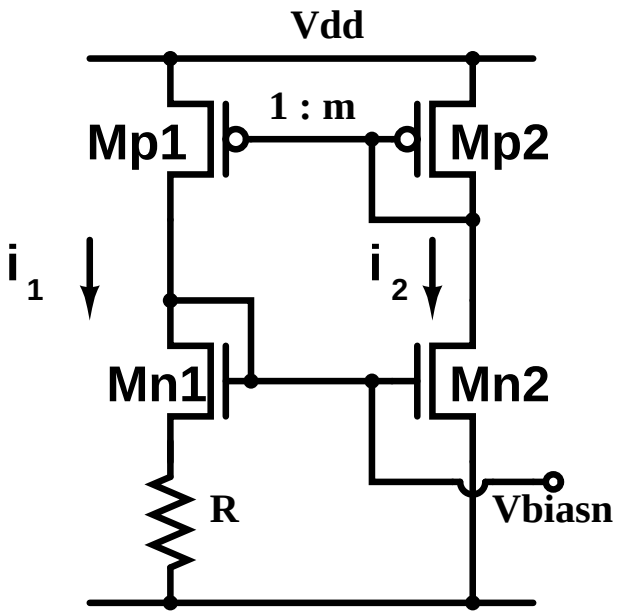
Digital Designers need not panic!

Only the interface works in current mode. Rest of the circuit is traditional.
Two voltage encoded bits from the circuit are converted to four current levels by a fast current mode DAC.

To put this plan into action, we need a receiver with zero input impedance.

(If inductive effects are to be taken into account, we would like to terminate the line into its characteristic impedance.)

The Beta Multiplier



We have $I_2 = mI_1$ with $m = \frac{(W/L)_{p2}}{(W/L)_{p1}}$

Equating voltages at the gates of n transistors:

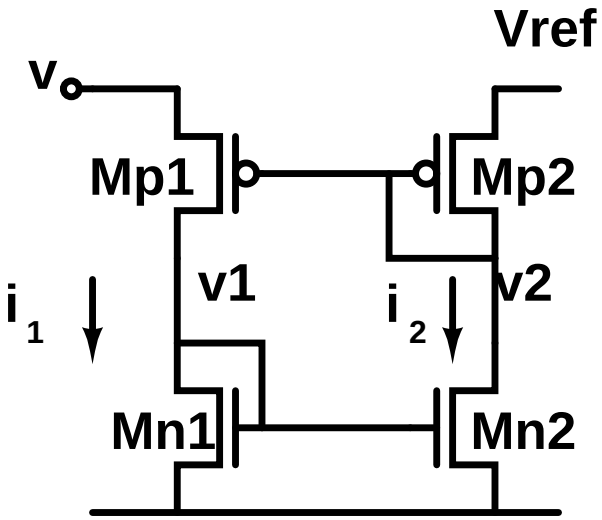
$$V_{Tn} + \sqrt{\frac{2I_1}{K_{n1}}} + RI_1 = V_{Tn} + \sqrt{\frac{2I_2}{K_{n2}}}$$

$$\text{so } \sqrt{\frac{2I_1}{K_{n1}}} + RI_1 = \sqrt{\frac{2mI_1}{K_{n2}}}$$

$$\text{or } \sqrt{\frac{2I_1}{K_{n1}}} + RI_1 = \sqrt{\frac{2I_1}{K_{n1}}}$$

Zero input impedance circuit

Low r_{in} amps are used for photo-detectors. (C.-K. Kim et al, "High Injection Efficiency Readout Circuit for Low Resistance Infrared Detector", IEE Electronic Letters, 35, 1507, 1999).



$$\begin{aligned} i_1 &= g_{mn1}v_1 = g_{mp1}(v - v_2) \\ i_2 &= g_{mn2}v_1 = -g_{mp2}v_2 \\ v_2 &= -\frac{g_{mn2}}{g_{mp2}}v_1 = -\frac{g_{mn2}}{g_{mp2}}\frac{i_1}{g_{mn1}} \end{aligned}$$

$$i_1 = g_{mp1}v + \frac{g_{mn2}/g_{mn1}}{g_{mp2}/g_{mp1}}i_1$$

$$\text{define } \Gamma \equiv \frac{g_{mn2}/g_{mn1}}{g_{mp2}/g_{mp1}} \qquad \text{then, } i_1(1-\Gamma) = g_{mp1}v$$

$$\text{This gives } r_{in} = (1-\Gamma)/g_{mp1}$$

Robustness of design

In saturation,

$$I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_g - V_T)^2$$

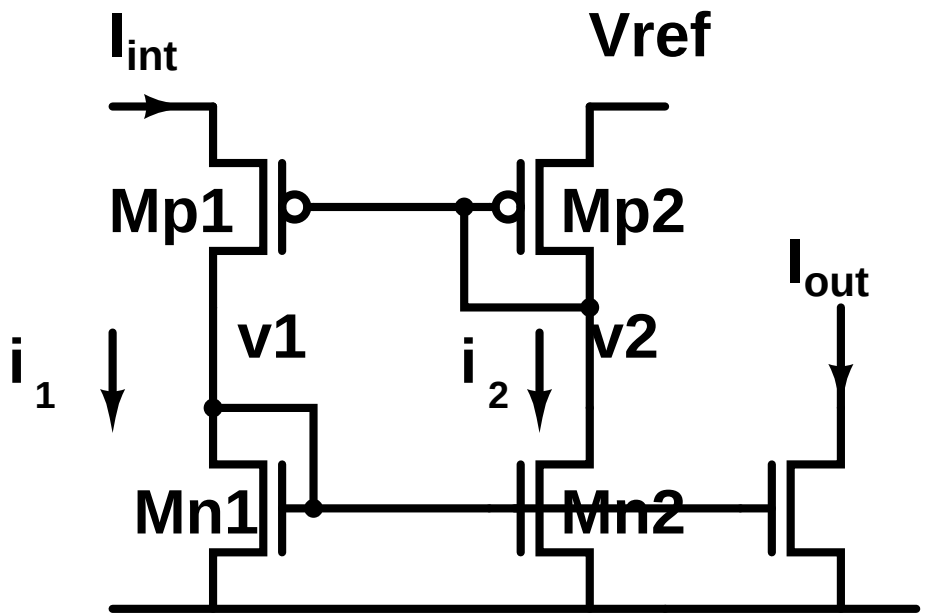
$$\text{So, } g_m = \mu C_{ox}\frac{W}{L}(V_g - V_T) = \sqrt{2\mu C_{ox}\frac{W}{L}I_d}$$

$$g_{mn2}/g_{mn1} = \sqrt{\frac{(W/L)_{n2}}{(W/L)_{n1}}\frac{I_2}{I_1}}$$

$$g_{mp2}/g_{mp1} = \sqrt{\frac{(W/L)_{p2}}{(W/L)_{p1}}\frac{I_2}{I_1}}$$

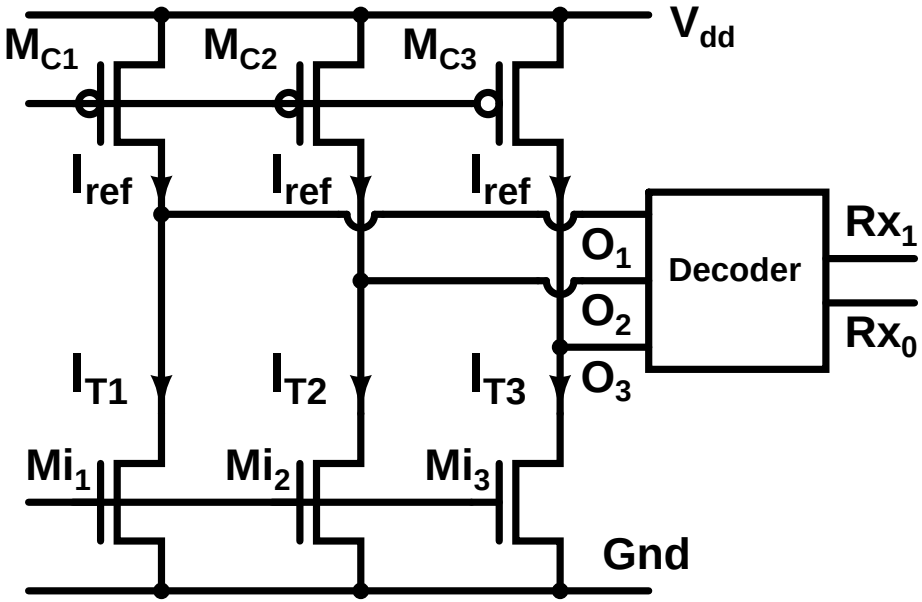
$$\text{Therefore } \Gamma \equiv \frac{g_{mn2}/g_{mn1}}{g_{mp2}/g_{mp1}} = \sqrt{\frac{(W/L)_{n2}/(W/L)_{n1}}{(W/L)_{p2}/(W/L)_{p1}}}$$

Receiver Design - Input stage



- Input resistance controlled by geometry of transistors
- Interconnect voltage held fixed
- Input resistance insensitive to process variations

receiver using Current comparators

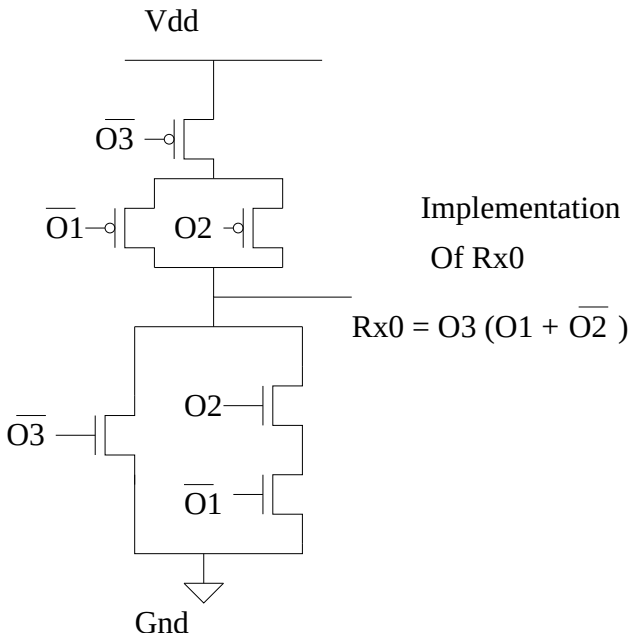


- $I_{T1} = k_1 \cdot I_{int}$; $I_{T2} = k_2 \cdot I_{int}$; $I_{T3} = k_3 \cdot I_{int}$

Current	O1	O2	O3
0	1	1	1
I	0	1	1
2I	0	0	1
3I	0	0	0

- $0 < I_{ref} < k_1 I$; $k_2 I < I_{ref} < 2k_2 I$; $2k_3 I < I_{ref} < 3k_3 I$

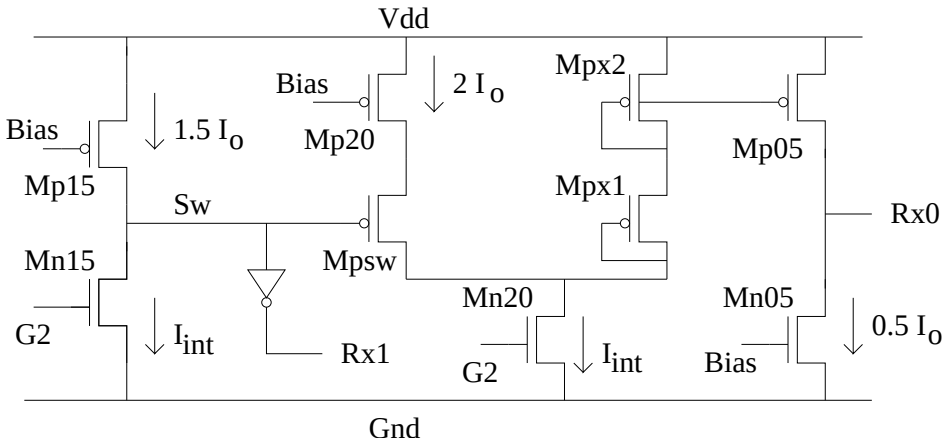
Decoder Circuit



$$Rx1 = O2$$
$$Rx0 = O3 \cdot (O1 + O2)$$

This circuit may produce glitches if comparators don't settle simultaneously.

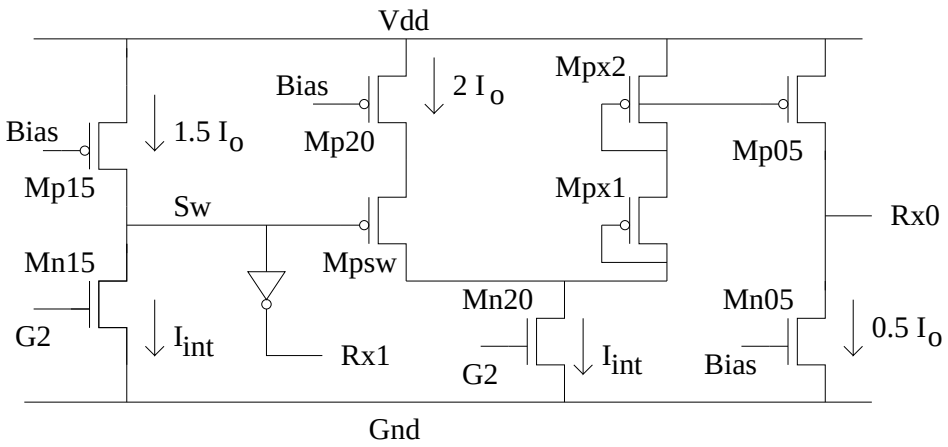
A to D based receiver



Mp15 and Mn15 form the comparator which determines the MSB. When MSB = '1', $2I_0$ flows through Mp20 and Mpsw.

The interconnect current is mirrored in Mn20.
Hence, the residual current $I_{int} - 2I_0$ flows through the transistors Mpx1 and Mpx2.
This residual current is mirrored in Mp05.

A to D based receiver

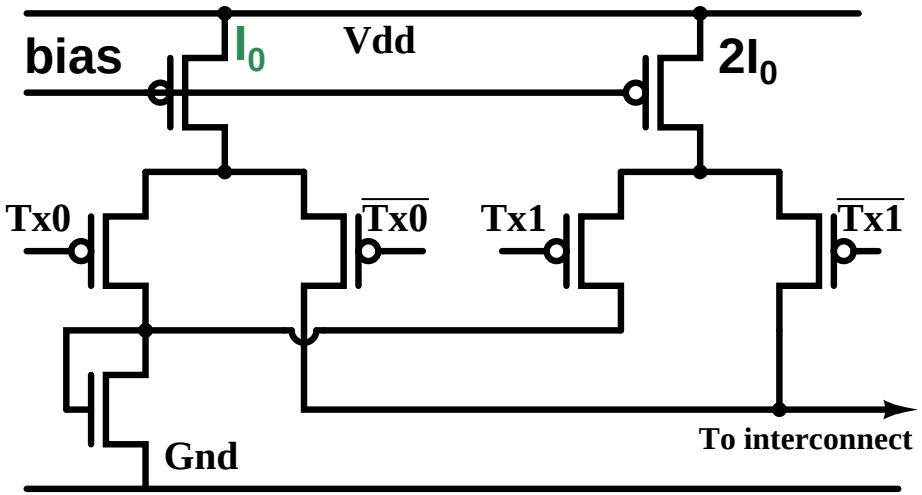


The residual current is mirrored in Mp05 for comparison with $0.5I_0$ (carried by Mn05).
This determines Rx0 (LSB).

When MSB is ‘0’, no current flows through Mp20-Mpsw branch and the entire interconnect current is replicated in Mp05 for comparison.

This A-to-D style receiver can be designed to be glitch free.

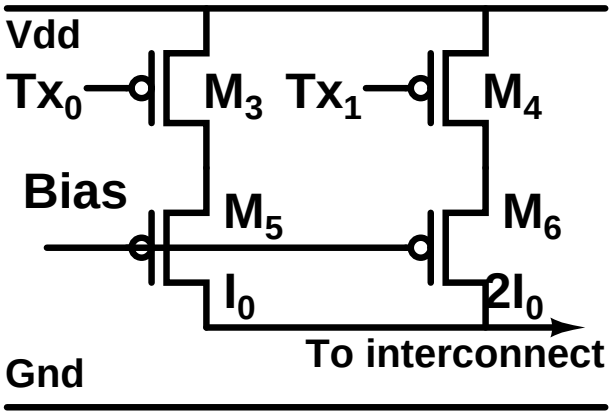
Current Steering Transmitter



- Essentially a 2bit current mode D to A.
- b0 controls the steering of current I_0 into the wire or into the ground.
- Similarly b1 steers $2I_0$ into the wire or into the ground.
- Consumes a constant current of $3I_0$.

Current steering is fast. (Like an ECL circuit).

Current Switching Transmitter



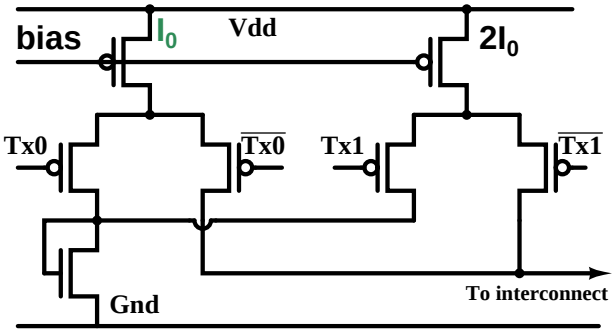
This design is marginally slower - but consumes less power.

Average current = $\frac{0+1+2+3}{4} I_0 = \frac{3}{2} I_0$

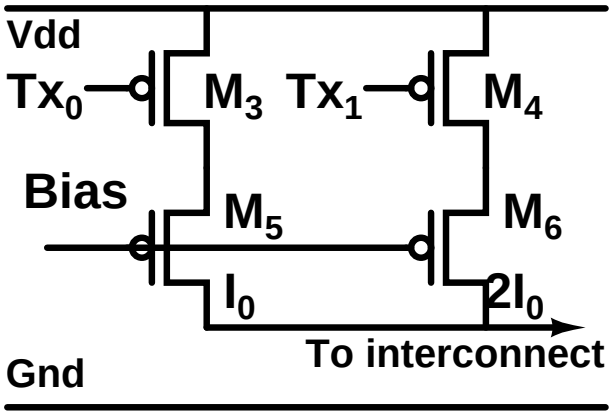
power modeling

$$
\begin{aligned}
R_0 &\equiv \text{Resistance of the wire per unit length} \\
C_0 &\equiv \text{Capacitance per unit length.} \\
L &\equiv \text{length of the wire.} \\
R_{int} &\equiv \text{Total wire Resistance} = R_0 L \\
C_{int} &\equiv \text{Total wire Capacitance} = C_0 L
\end{aligned}
$$

Power dissipation in the transmitter

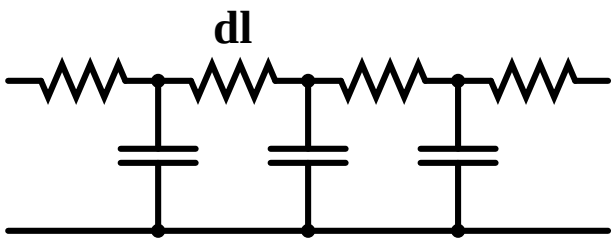


Current steering transmitter consumes $3V_{dd}.I_0$. This is inclusive of the static and dynamic power in the wire as well as in the left half of input receiver.



Current switching transmitter consumes $\frac{3}{2}V_{dd}.I_0$ inclusive of the static and dynamic power in the wire as well as in the left half of input receiver.

Static power dissipation in the wire

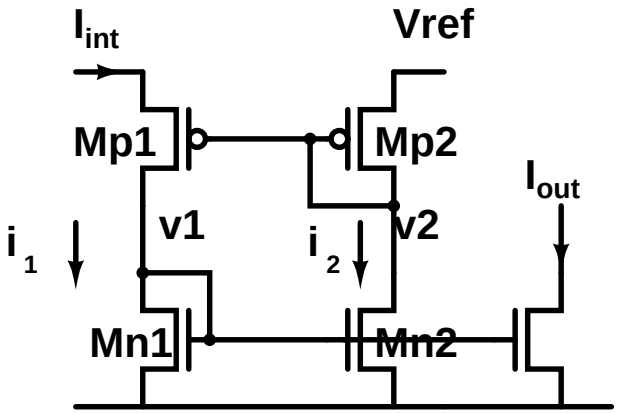


- The static power is given by $R_{int} I^2$.
- If all logic states are equally likely, Average $I^2 = \frac{0^2+1^2+2^2+3^2}{4} I_0^2 = \frac{7}{2} I_0^2$ where I_0 is the unit current step.

Therefore the static power dissipation is

$$P_{static} = \frac{7}{2} R_{int} I_0^2 = \frac{7}{2} L R_0 I_0^2$$

Beta multiplier Power Dissipation



The left arm of the beta-multiplier (Mp1-Mn1) has already been accounted for in the transmitter power loss.

The right arm carries a current I_{int} (the wire current), whose average value is $1.5I_0$.

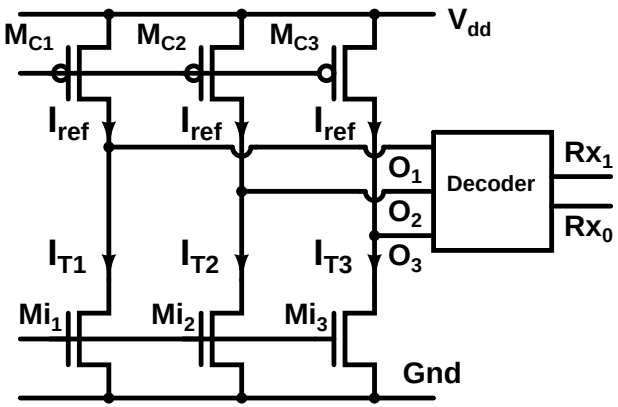
Also the generation of the reference voltage at source of Mp2 requires an additional current of I_{ref}

Hence, the power loss in the beta multiplier is :

$$V_{dd} \cdot (1.5I_0 + I_{ref})$$

Current comparator decoder

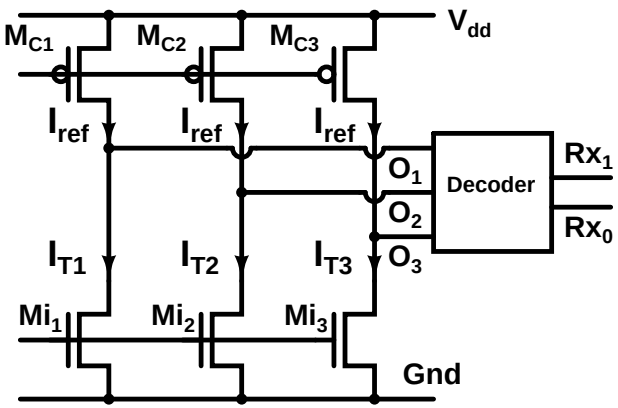
Comparators carry the smaller of the currents being compared.



- Wire current = $3I_0$:
  Comparators currents are:
  $0.5I_0$, $1.5I_0$ and $2.5I_0$.
  Power loss = $V_{dd} \cdot 4.5I_0$.
- Wire current = $2I_0$:
  Comparator currents are:
  $0.5I_0$, $1.5I_0$ and $2I_0$.
  Power loss = $V_{dd} \cdot 4I_0$.

Current comparator decoder

Comparators carry the smaller of the currents being compared.



- Wire current = I_0:
  Comparators currents are:
  $0.5I_0$, I_0 and I_0.
  Power loss = $V_{dd} \cdot 2.5I_0$.
- Wire current = 0:
  No current flows in any comparator.
  Hence, there is no static power loss.

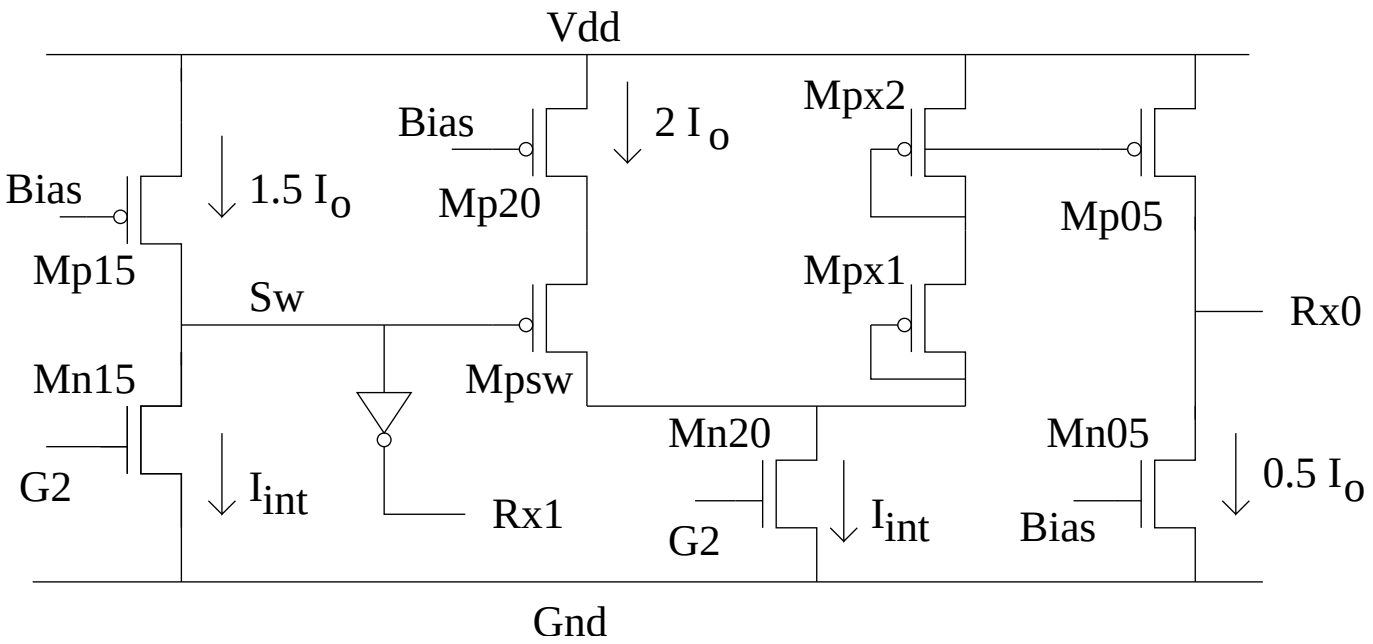
Current comparator decoder

The average power consumption (assuming equal likelihood of all states) is given by

$$\frac{4.5 + 4 + 2.5 + 0}{4} I_0 \cdot V_{dd} = 2.75 I_0 \cdot V_{dd}$$

The decoder following this current comparator does not consume any static power loss, being a digital CMOS circuit.

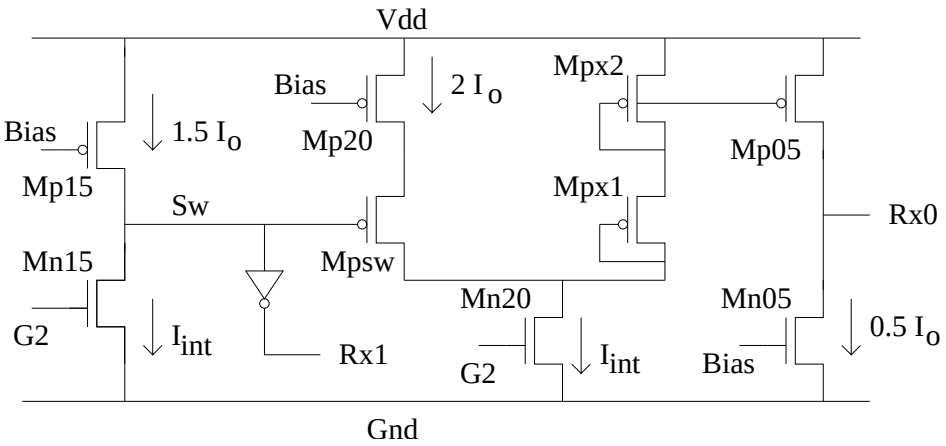
A to D type decoder



Mn20 always carries I_{int}

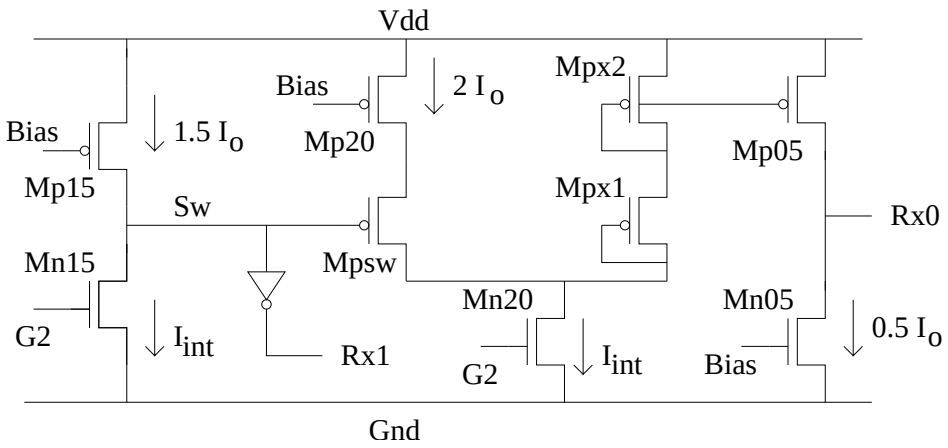
The power loss in residue generating section (Mp20, Mpsw, Mpx1, Mpx2 and Mn20) is always $I_{int} \cdot V_{dd}$.

A to D type decoder



- Wire current = $3I_0$
  Comparators:$1.5I_0$ and $0.5I_0$.
  Residue generator: $3I_0$
  Total power = $5I_0 \cdot V_{dd}$.
- Wire current = $2I_0$:
  Comparators: $1.5I_0$ and 0.
  Residue generator: $2I_0 \cdot V_{dd}$.
  Total power = $3.5I_0 \cdot V_{dd}$.

A to D type decoder



- Wire current = I_0 :
  Comparators: I_0 and $0.5I_0$.
  Residue generator: $I_0 \cdot V_{dd}$
  Total power = $2.5I_0 \cdot V_{dd}$.
- Wire current = 0 :
  no current flows anywhere and hence there is no static power loss.

Assuming equal likelihood of all states, the average power consumption is $2.75I_0 \cdot V_{dd}$.

Comparison of the two receivers

- The average power consumption of both circuits is identical,
- In the worst case, the A to D type receiver consumes more power than the standard receiver.
- However, the A to D type receiver offers advantages in speed and eliminates the possibility of glitches in the output.

Summary of Power Analysis

- The static power in the circuits dominates over the power dissipation in the wire.
- The power consumption of the system is independent of the wire length.
- This is because the power consumed in the wire is always supplied by the transmitter - which depends only on Io.
- Therefore, the power consumed by the transmitter circuit + wire + left arm of the beta multiplier is independent of the wire length.

Summary of Power Analysis

The wire length limit of operation of this system arises from the current drawn by the wire capacitance and the transmitter-end voltage.

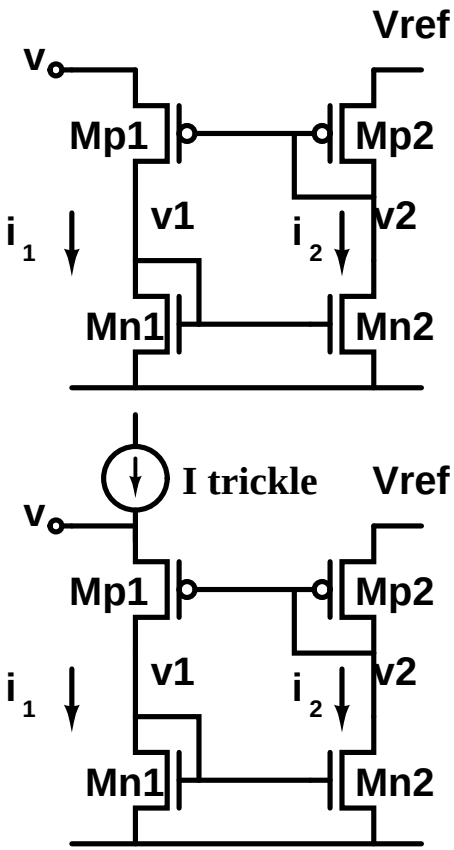
- If the wire length is high enough such that the wire capacitance sinks current more than $0.5I_0$, then the current reaching the beta-multiplier will reduce by half the unit current level, which can lead to (transient) incorrect decoding.
- If the wire is so long that the transmitter-end voltage, $V_{dd} + I_{int} \cdot R_{int}$, rises sufficiently for the transmitter transistors to go out of saturation, then the transmitter will be unable to drive the required current into the wire.

Speed Analysis

Latency:

- Current switching at transmitter is faster.
- Wire delay is lower due to negligible voltage swings on the interconnect.
- However, the receiver may be slower due to
  - Beta multiplier turning off at zero current.
  - Slow current comparison

Beta-Multiplier with Trickle Current

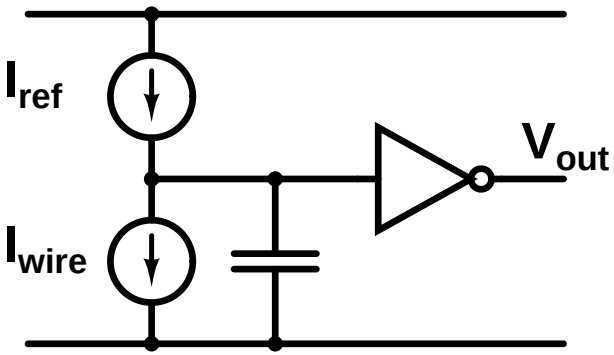


For input current of 0, the beta multiplier will turn off completely. For subsequent input transitions, the beta multiplier needs to be turned on.

Turn on delay can be avoided by adding a trickle current. The trickle current is added to the interface current.

Trickle current of $40\mu A$ to $80\mu A$ has been used in the design.

Current Comparators



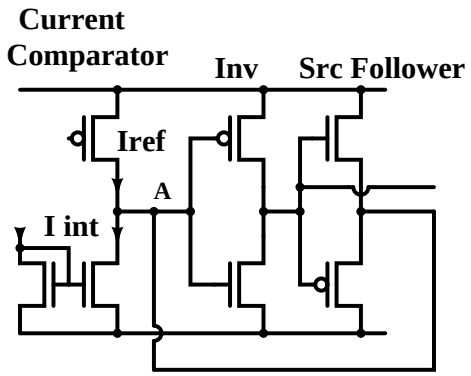
Current mode receivers use current comparators to produce a voltage mode digital output.

The load capacitance is charged by the difference current.

- These comparators have a ‘dead spot’ when the two currents are exactly equal.
- If the currents are *nearly* equal, the comparators are extremely slow.
- This has a bearing on deciding the current separation between differnt levels, as the nominal current difference between I_{ref} and I_{int} is $\frac{\Delta I}{2}$.

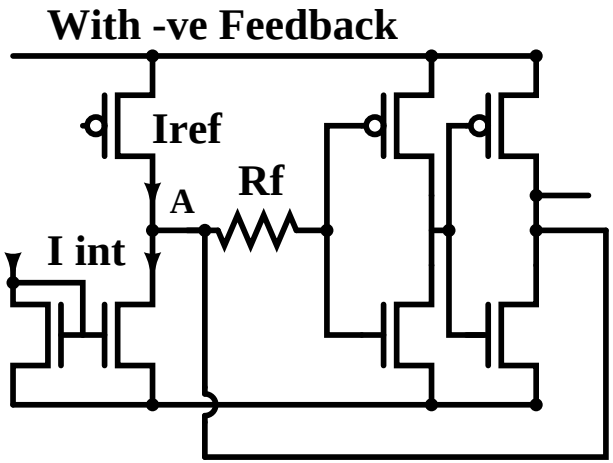
Current Comparators

Current comparators can be speeded up by limiting the voltage swing required at their output.



- The source follower stage restricts the output beyond a swing of V_{Tn} above and V_{Tp} below the resting voltage.
- It does have a dead band near zero difference current.
- Also, the inverter amplifier consumes static power.

Current Comparators



The circuit here uses an inverter with resistive feedback to amplify the small swing at A.

- the Value of Rf is critical for fast operation of the circuit.
- Large Rf reduces voltage swing at node A but the reduced output voltage swing causes static power dissipation in the subsequent inverter.
- Rf is implemented using a transmission gate circuit.

Speed Analysis: Throughput

- Throughput is inversely proportional to variation in delay
- There is Lower delay variation in current mode.
- Also, in multi bit current mode systems, 2 bits can be sent per wire $\Rightarrow$ Higher Throughput

Simulation Results: Current Comparators

$I_{ref} - I_{in}$	Neg.Feedback Amplifer		Low Op. Impedance	
(μA)	Rise	Fall	Rise	Fall
40	251	239	439	387
50	252	240	395	349
60	255	243	364	320
80	267	252	320	284
100	279	261	291	259
120	288	268	270	241

Simulation Results: Current Comparators

I_{in}	Neg.Feedback Amplifer(μW)	Circuit A (μW)
0	266.4	312.8
I_0	339.8	349.74
$2I_0$	372.6	395.64
$3I_0$	371.9	458.58

- $R_f = 35K$ and around $I_{ref} = 160\mu A$
- Power consumption in circuit A is large. Hence, we chose current comparators with negative feeck amplifier.

Simulation Results: Multi-level Current Mode Signaling

- CVCS scheme for two bits per line (N=2) was designed for $I_0 = 80\mu A$ and $I_{trickle} = 60\mu A$
- CVCS scheme for N=1 was designed with $I_0 = 40\mu A$ and $I_{trickle} = 40\mu A$

Parameters	CVCS with		Voltage Mode
	N=1	N=2	
Avg Delay (ns)	0.786	0.9	0.862
Throughput	1Gbps	1Gbps	1Gbps
Power (mW)	8.896	20.704	118.152
Area μm^2	870.4	758.16	18560
Wires (16bit bus)	16	8	16

Simulation Results: Multi-level Current Mode Signaling