DRIFT CANCELLATION CIRCUIT

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INTRODUCTION

In biomedical signal processing, we have waveforms in which signals of interest are small in magnitude, often superimposed on a large offset or base. This base may be changing with time due to motion artifacts or may be the result of a large amplification factor [1]. Usually, a high pass filter with very low cutoff frequency is used to cancel the base and drifts in it. But the frequencies thus attenuated might be of interest. So instead of conventional frequency domain method an amplitude domain method, similar to successive approximation is used here. Here, we assume that the signal excursions are restricted to a particular range. Whenever this range is crossed, it must be due to baseline drift and therefore should be compensated for. A baseline drift that does not result in crossing of this range will not be compensated.

The block diagram of the circuit is shown in Fig.1. An adder gives the difference of the input signal and the integrated feedback. If this sum is beyond the limits V_{r1} and V_{r2}, (preset reference range), then the feedback is activated. The integrator gives an integrated negative feedback. The three level comparator output is zero if Vo is in the acceptable range. This circuit has been developed as part of an impedance cardiograph [4,5]. In impedance cardiography, the change in the thoracic impedance due to varying amounts of blood is of interest. The changes in the impedance are of the order of 1 to 2% and have to be amplified. However, the base impedance varies due to motion artifacts. Qu et al. [2] used a successive approximation register (SAR) along with a D/A converter (DAC) for DC cancellation. The digital output of SAR was converted to an analog signal by DAC, and was subtracted from the impedance signal giving only the change in impedance. The SAR and DAC ICs being costly and power consuming, the circuit reported here is based on the same concept as [2] but uses analog ICs.

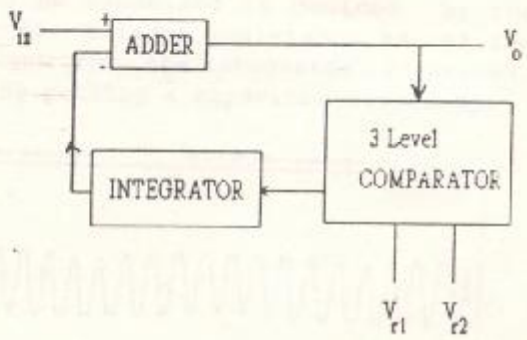

Figure 1: Block diagram of the circuit

The circuit

The circuit is an adaptation of circuits reported earlier in [3] and [4], and is shown in Fig. 2. Op-amp A1 acts as an inverting adder, op-amp A2 is an inverter. Op-amps A3 and A4 are used as comparators, and op-amp A5 is an inverting integrator. Op-amp A5 should be a low input bias current op-amp. In implementation, quad op-amp LF347 is used for op-amps A1, A3, A4, and A5. Op-amp A2 is a μA741 op-amp.

The output of op-amp A1, V_a, can be written as -

$$V_a = -(V_i + V_c).(R_3/R_1) = -a.(V_i + V_c)$$

The output of op-amp A2, V_b, is $-V_a$. V_a and V_b are given to the comparators A3 and A4 respectively. Initially, let the output of the ~~comparator~~ integrator, V_c, be

V_{c0}. The output of A3, V_a is $-a(V_i+V_{c0})$. If V_a is less than V_r, both A3 and A4 are driven to positive saturation since V_b is greater than V_r. Therefore diode D2 is on, and D3 is off. The integrator output, V_c, starts decreasing, V_a starts increasing, and V_b starts decreasing. Finally, when V_b goes below V_r, the output of A3 goes to negative saturation, and diode D2 turns off. Since both the diodes are off, the integrator output stabilizes so that -

$$V_b = a.(V_i + V_c) < V_r$$

If the output drops below $-V_r$, the output of A4 goes to negative saturation, and D3 turns on. The integrator output now starts increasing till $V_a > -V_r$, and $V_b < V_r$. Thus the output V_b is always maintained within the range $\pm V_r$.

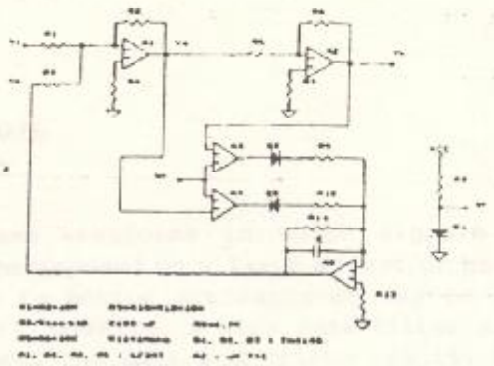

Figure 2: Drift Cancellation Circuit (for up to 0.5Hz). (Note:Vr1=-Vr2=0.65V)

The highest frequency DC drift that can be cancelled is decided by the charging RC time constant of integrator A5. A large resistance across the capacitor provides the input bias current for the integrator. If needed, a low pass filter can be realized by putting a capacitor across R3.

RESULTS

The circuit was used for cancelling the base impedance in an impedance cardiograph [5]. An amplification of 10 was used with the inverting adder. The circuit could cancel drifts up to 8.5 Hz. And the bandwidth was up to 160 KHz.The response of this circuit for an input signal is shown in Fig. 3.

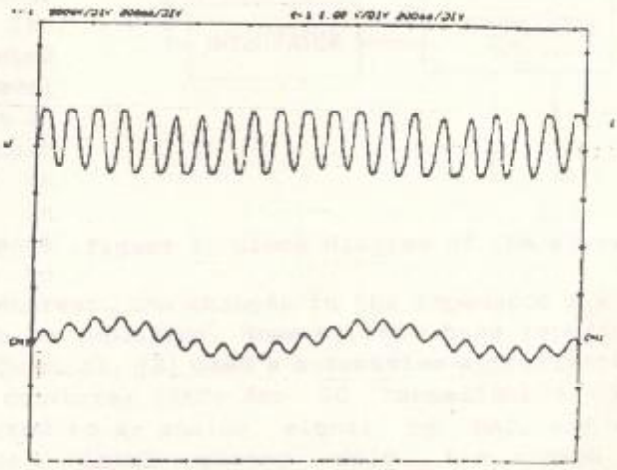

Figure 3: Input and output response of Drift Cancellation Circuit (Ch.1 Input, Ch.2 Output)

REFERENCES

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