A Tracking Based Drift Cancellation Circuit for Biosignal Acquisition

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Abstract: *In most biosignals, acquired for diagnosis purpose, the signal excursion is limited to a small range, often superimposed on a baseline which may drift over a large range. While amplifying the signal for signal acquisition and processing, the baseline drift needs to be reduced in order to make effective use of the ADC input dynamic range. The microcontroller based circuit reported here uses tracking technique for estimation and removal of the base line drift before signal acquisition. This circuit is versatile in application as it is independent of the processor to which the ADC is interfaced.*

Keywords: Biosignal acquisition, Drift cancellation, Tracking conversion, Microcontroller application.

I. INTRODUCTION

Various biosignals which are acquired for diagnosis purpose have their frequency spectrum in the range of 0.2 Hz to 5 kHz [1]. In most biosignals, the signal excursion is limited to a small range, superimposed on a large baseline which may slowly drift over a large range. While amplifying the signal, the baseline drift needs to be removed. Several methods have been reported for suppressing base line drift, including bridge circuit [2], reset circuit [3], successive approximation register (SAR) based drift cancellation circuit [4], and integrator based drift cancellation circuit [5]. Bridge based circuit does not permit removal of base line drift related to artifacts. Reset circuit [3] makes use of sample-and-hold circuit and hold error may introduce its own drift. SAR based drift cancellation circuit [4] is free from these problems. Our circuit makes use of tracking in place of successive approximation, resulting in a hardware simplification.

We have developed a microcontroller based drift cancellation circuit using tracking technique. During amplification of the input, a correction voltage is subtracted, so that the output voltage is within a range defined by two thresholds. As long as output remains within this range, the correction voltage is not changed. If the output voltage crosses the range in either direction, the correction voltage is changed to track the base line drift and bring back the output signal in the middle of the range. The main application of this scheme is to fully use the dynamic range of the signal acquisition unit. Further removal of the baseline drift may be carried out by digital processing. This circuit was developed as part of instrument development for impedance cardiography. Impedance cardiography technique is based on sensing the variation in thoracic impedance due to changes in the blood volume in the thorax [4], [6], [7], [8], [9], [10], [11], [12]. The change in impedance of thorax is generally within 2% of base impedance [8], [10], [11]. Breathing and thoracic dimension changes introduce respiratory and motion artifact components. These artifacts have large amplitude and partly overlapping frequency band as compared to varying impedance signal. It may be possible to employ digital signal processing for suppressing the baseline drift due to these artifacts, but the drift needs to be at least partly removed before analog-to-digital conversion in order to make proper use of ADC input range.

A drift cancellation circuit using successive approximation technique (SAR) has been earlier reported as part of an impedance cardiograph [4], [13]. This circuit uses an adder, threshold detector, successive approximation register (SAR), and digital-to-analog converter (DAC) as shown in Fig. 1. In this circuit, the successive approximation register (SAR) and digital-to-analog converter (DAC) approximate the base line drift, which is subtracted from the input signal and the difference is amplified to give the output V_o. Whenever voltage V_o crosses the threshold range [V_{t1}, V_{t2}] in either direction, a start pulse is given to SAR and successive approximation is initiated. Polarity of V_o with respect to the center of threshold range is used as data input for successive approximation to obtain a new estimate of the base line and output is brought to near the center of the range. The signal V_o is not usable for processing during the base line balancing process, which lasts for a short duration (8 clock pulses for 8-bit SAR).

A simpler version based on ramp approximation was later reported [5], [6], using an integrator in place of the SAR and DAC. However, capacitor discharges and op amp DC errors in the integrator introduce a drift, whose correction may lead to oscillatory drift. This can be removed in the subsequent signal processing, but it reduces the ADC input dynamic range.

In the circuit presented here, we have used tracking, in place of successive approximation, for estimation and removal of the base line drift. Since tracking can be done

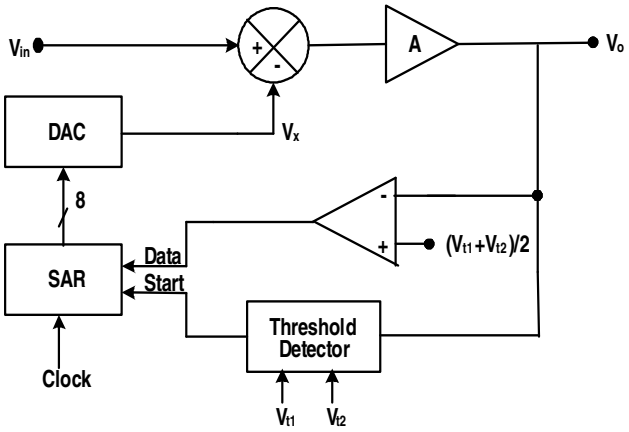


Fig. 1 A block diagram of successive approximation based drift cancellation circuit reported in [4] , [13].

as soon as signal crosses the range, we can use PWM for digital-to-analog conversion, resulting in overall hardware simplification. The technique has been implemented using a microcontroller. Using this circuit, signal acquisition can be done by using any standard signal acquisition set-up. An alternative to our approach will involve implementing a similar scheme for estimating the correction voltage on the processor controlling the signal acquisition system, and outputting the correction voltage using its digital-to-analog port. Thus the microcontroller based design is versatile in application, as it is independent of signal acquisition set-up.

II. BASIC PRINCIPLE

A block diagram of the drift cancellation circuit based on tracking approximation is given in Fig.2. The up/down counter and DAC are used to track the base line drift in the input signal, and the estimated drift is subtracted from the input to give the drift balanced output V_o. Whenever the output crosses threshold range [V_{t1}, V_{t2}], a new estimation of the drift is carried out in the up/down counter, depending on the direction of the drift. If $V_o > V_{t1}$, the counter is incremented. If $V_o < V_{t2}$, the counter is decremented. One quantization step of the DAC corresponds to half of the threshold range. Thus after crossing of the threshold in either direction, the signal is brought back to center of the range. For the correction interval, the signal is not usable for processing. The base line drift correction is done in one clock pulse, and hence we can use a relatively slower DAC. The up/down counter and clock generator can be realized through software under a microcontroller. Further, the digital-to-analog conversion can be realized using PWM output from one of the port pins of the microcontroller, and the hardware can be made simpler.

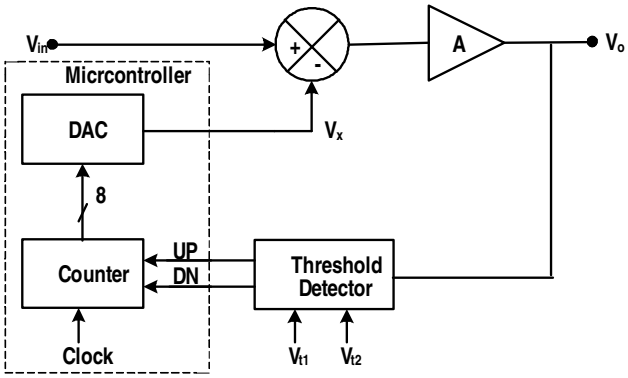


Fig. 2 Block diagram of tracking based drift cancellation circuit.

III. CIRCUIT DISCRIPTION

The circuit diagram of the microcontroller based implementation is shown in Fig. 3. The circuit uses quad op amp TL084 as U1 and 20-pins microcontroller AT89C2051 [14] as U2. This circuit has been developed for base line drift removal in an impedance cardiograph [15]. The impedance cardiograph circuit works with ±12 V supply. In addition to these two supply voltages, microcontroller requires +5 V supply.

Expected actual impedance cardiograph signal range is [-25, 30] mV and because of base line drift the signal excursion can be [1.75, 5] V. For proper signal acquisition, the signal after drift reduction and amplification, should fit well within the ±5 V input range of the ADC.

Op amp U1A is an inverting adder for input V_{in} and base line approximation V_x

$$V_0 = A_1 V_{in} + A_2 V_x \qquad (1)$$

where $A_1 = - R_2 / R_1$ and $A_2 = 1 + R_2 / (R_1 \| R_3)$.

The output V_o is compared with the threshold voltages V_{t1} and V_{t2}, with op amps U1B and U1C used as comparators. Threshold detector outputs are given to microcontroller U2 port pins P1.0 and P1.1. The tracking up/down counter of Fig. 2 is realized through software inside the microcontroller. The count value is output as PWM as an approximation to the base line drift. The PWM pulses are low pass filtered by second order Butterworth low pass filter formed by U1D. In our implementation, microcontroller operates with 24 MHz crystal. The 8-bit up/down counter and PWM output on pin P3.5 are implemented through software, with PWM clock of 10 kHz. The duty cycle can be varied from 5% to 90% in 256 steps, in accordance with the counter output. The cutoff frequency of the low pass filter is selected as ≈ 60 Hz (<< 10 kHz), so that the output V_x, is ripple free. It is to be noted that because of the low pass filter, the

tracking process has to wait for approximately 10 ms after each step change, before tracking the next tracking step.

Let input be given as actual signal V_s superimposed on base line drift V_d.

$$V_{in} = V_s + V_d \tag{2}$$

Actual input signal range is mapped to the output voltage, and hence the gain for the input signal is

$$A_1 = -(V_{t2} - V_{t1}) / (V_{s\max} - V_{s\min}) \tag{3}$$

If the output of adder crosses lower threshold V_{t1}, the comparator U1B is driven to positive saturation, producing high input to pin P1.0 of microcontroller U2. The duty cycle of PWM is increased by a fixed percentage, corresponding to one step change in counter. Similarly, if V_o crosses the upper threshold $V_{t2,}$ input P1.1 of microcontroller becomes high and the PWM duty cycle is decremented by one step. The low pass filter output V_x changes correspondingly to

$$\begin{aligned} V_x(t_{n+1}) &= V_x(t_n) + \Delta V_x,\ V_0(t_n) < V_{t1} \\ &= V_x(t_n) - \Delta V_x,\ V_0(t_n) > V_{t2} \\ &= V_x(t_n), \text{ otherwise} \end{aligned} \tag{4}$$

The step ΔV_x is given by

$$\Delta V_x = 0.5\,(V_{t2} - V_{t1}) / A_2 \tag{5}$$

and also as

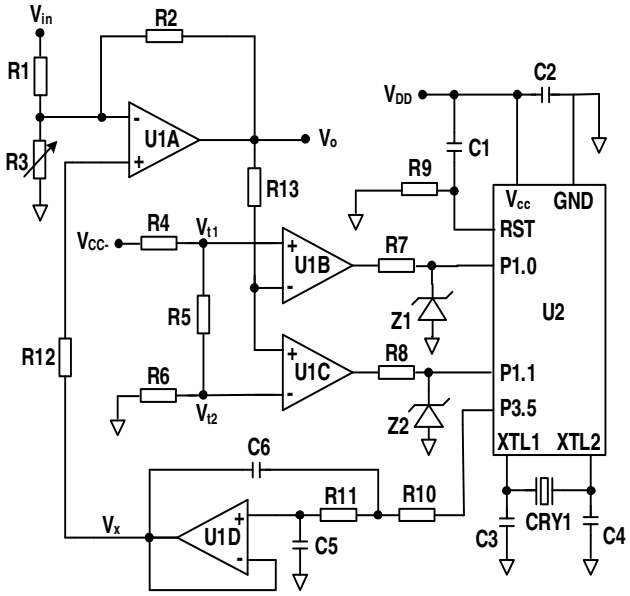
$$\Delta V_x = (V_{x\max} - V_{x\min}) / N \tag{6}$$

where N = total number of PWM steps. This feedback voltage is used for base line drift correction as per Eqn. 1 to bring V_o within the threshold range. If V_o is still below V_{t1}, the process is repeated. If the V_0 is in the range [V_{t1}, V_{t2}], both the comparator outputs are low, the count in the counter is not changed, the duty cycle of PWM pulses remains unchanged, and the value remains constant.

The relationship between input voltage V_{in} and the output voltage V_o along with the correction voltage V_x is shown in Fig. 4, for (a) increasing input and (b) decreasing input. It is to be noted that drift cancellation has a hysterisis, and the actual output depends on the direction of input change.

IV. RESULTS

Component values shown in Fig. 3 were selected for threshold voltages V_{t1} = - 2.5 V and V_{t2} = - 1 V, signal gain A_1 = - 10 and correction voltage gain A_2 = 39. An example of drift cancellation by the implemented circuit is shown in Fig. 5. Input consisted of 50 mV (p-p) sine wave of 20 Hz superimposed on a triangular drift changing from 1.3 V to 1.5 V. Output signal shows the drift compensation when the signal crosses the threshold range. It is to be noted that the signal is not usable during the drift correction interval. The small amount of residual drift may require further signal processing.



R1=10k, R2=100k, R3=10k, R4=33k, R5=5.6k, R6=3.3k, R7=10k, R8=10k, R9=8.2k, R10=33k, R11=22k, R12=3.9k, R13=10k, C1=10µ, C2=10µ, C3=22p, C4=22p, C5=0.1µ, C6=0.1µ, V_{cc-}=-12V, V_{DD}=+5V

Fig. 3 Circuit diagram of the microcontroller based implementation (U1 : TL 084, U2 : AT89C2051).

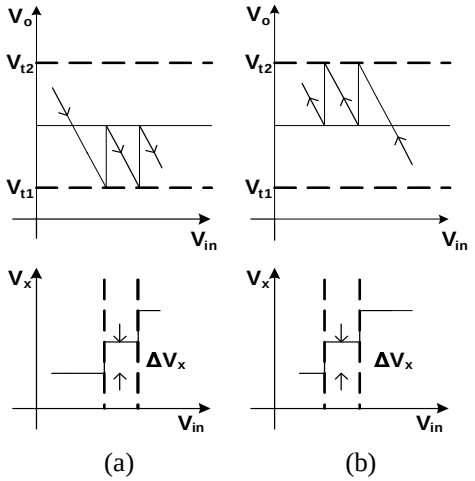


Fig. 4 Input-output relationship for (a) increasing input and (b) decreasing input.

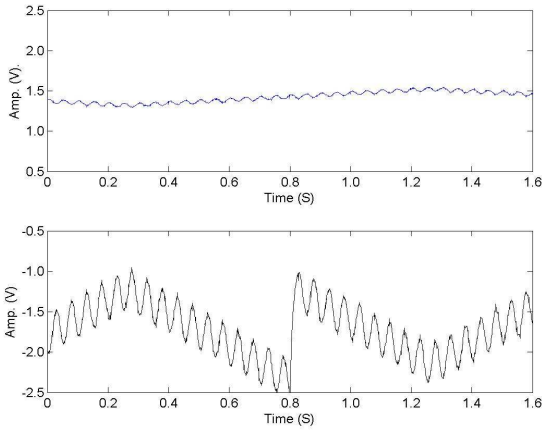


Fig. 5 Example of drift cancellation.

V. CONCLUSION

For suppressing the low frequency drift present in biosignals, a tracking based drift cancellation circuit is developed. Implementation has been carried out using a 20-pin microcontroller with tracking up-down counter and PWM based DAC, thereby simplifying the hardware. The implemented circuit uses 10 kHz carrier for clock and hence each correction step involves about 10 ms for ripple free correction, and hence the circuit can be used effectively for drifts of up to 10 Hz. This is a versatile circuit for suppression of large drift in biosignals, as it is independent of the processor to which the signal acquisition unit is interfaced and can be used in set-ups with real time as well as offline processing. In the present implementation, tracking of base line drift is initiated by the output going out of the defined range. Alternatively, the microcontroller can be programmed to carry out the tracking for drift cancellation at periodic intervals, and this may be more appropriate for certain applications.

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