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Tracking Based Baseline Restoration for Acquisition of Impedance Cardiogram and Other Biosignals

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***Abstract*—Most of the biosignals have a baseline which may drift over a large range compared to the excursion of the signal of interest. To make effective use of the input dynamic range of the signal acquisition setup, this offset drift needs to be cancelled. The circuit reported here uses amplitude tracking technique for estimation and removal of the baseline drift. This circuit is independent of the processor to which the signal acquisition unit is interfaced.**

***Keywords*—Baseline restoration, Offset drift cancellation, Impedance cardiogram, Biosignal acquisition.**

I. Introduction

BIOIMPEDANCE signals usually consist of a time-varying component, related to the physiological phenomenon of interest, superimposed on a baseline with an offset. This offset may drift over a range much larger than the excursion of the signal component. To make effective use of the input dynamic range of the signal acquisition setup, the offset drift needs to be at least partly removed.

In bioimpedance measurement, the baseline varies from subject to subject and with electrode placement and it may also drift for the same subject with movement. A high pass filter cannot be used because the spectrum of the signal often overlaps with that of the drift. Hence automatic cancellation of offset drift is required for restoration of baseline. The solution presented here has been developed as a part of instrumentation for impedance cardiography, but may be applied for other bioimpedance measurements.

Impedance cardiography involves measurement of variation in electrical impedance of the thorax, caused by change in the blood volume during the cardiac cycle, for monitoring stroke volume and obtaining diagnostic information on cardiovascular functioning [1]-[5]. The variation in the impedance is only around 1 to 2 % of basal impedance [1], [3], [5]. The basal impedance gives rise to dc offset voltage and exhibits a drift related to respiration and movements.

Several automatic balancing methods have been reported including bridge circuit [6], automatic reset circuit [7], self-balancing system [8], successive approximation register (SAR) based method [9], [10], and integrator based drift cancellation circuit [4]. Bridge circuit [6] is specifically designed for temperature drift cancellation, and not easily adaptable for other applications. Automatic reset circuit [7] uses sample-and-hold, and the hold error introduces its own drift.

The self-balancing system [8] is based on balancing the baseline drift by ramp approximation by digital counting. It works for unipolar input and baseline is restored to below a set threshold value. It consists of a differential amplifier, threshold detector, counter, digital-to-analog converter (DAC), and comparator. The counter output is given to the DAC and the difference between the DAC output and the input is amplified, to provide the baseline corrected output. Whenever the output voltage crosses a set threshold, a narrow pulse is generated to reset the counter, and the counter starts incrementing until the DAC output equals the analog input. For n-bit counter and DAC, the balancing may take up to 2^n clock pulses.

In the successive approximation based method [9], [10], the counter has been replaced by a SAR. The SAR and DAC approximate the baseline drift, which is subtracted from the input signal and the difference is amplified to give the output V_o. Whenever voltage V_o crosses the threshold range [V_{t1}, V_{t2}] in either direction, a start pulse is given to SAR and successive approximation is initiated. Polarity of V_o with respect to the center of the threshold range is used as input for successive approximation to obtain a new estimate of the baseline and output is brought to near the center of the range. The baseline balancing process requires n clock cycles for an n-bit SAR. A simpler version based on ramp approximation was later reported [4], using an integrator in place of the SAR and DAC. However, capacitor discharges and op amp DC errors in the integrator introduce a drift, whose correction may lead to oscillatory drift. This can be removed in the subsequent signal processing, but it reduces the ADC input dynamic range.

In the circuit presented here, we have used tracking, in place of successive approximation, for estimation and removal of the baseline drift. The baseline restoration requires only one clock cycle. This technique has been implemented using a microcontroller which controls the DAC by giving the digital output corresponding to the baseline value.

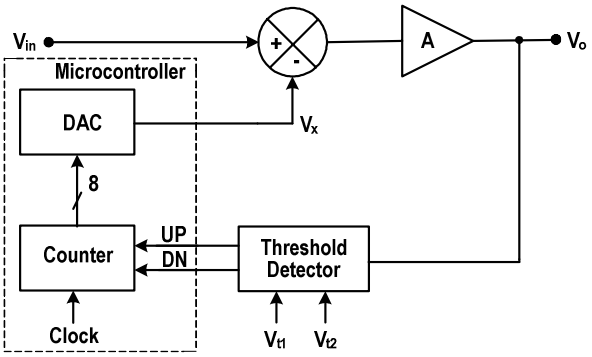

Fig. 1. Block diagram of tracking based drift cancellation circuit.

II. Tracking Based Baseline Restoration

The basic idea is to subtract an estimate of the baseline voltage from the signal such that the signal after amplification would be well within the input dynamic range of the signal acquisition system. The block diagram for the tracking based approach is given in Fig. 1. It is to be noted that the circuit does not continuously remove the drift, but only if the signal crosses the threshold range, set in accordance with the excursion of the output signal and the input range of the signal acquisition unit.

The up/down counter and DAC are used to track the baseline drift in the input signal, and the estimated drift is subtracted from the input to give the drift balanced output V_o. Two thresholds [V_{t1}, V_{t2}] are selected corresponding to the desired range of the signal or the input range of the ADC used in the succeeding stage. Whenever the output crosses threshold range [V_{t1}, V_{t2}], a new estimation of the drift is carried out in the up/down counter, depending on the direction of the drift. If $V_o > V_{t2}$, the counter is incremented and if $V_o < V_{t1}$, the counter is decremented. One quantization step of the DAC corresponds to half of the threshold range. Thus after crossing of the threshold in either direction, the signal is brought back to center of the range. During the correction interval, the signal is not usable for processing.

The baseline drift correction is done in one clock pulse, and hence a relatively slower DAC can be used. The up/down counter and the clock can be realized through software using a microcontroller. Further, the digital-to-analog conversion can be realized using PWM output from one of the port pins of the microcontroller, and the hardware can be made simpler. To cancel both positive as well as negative baselines, the duty cycle of 50% can be kept corresponding to a baseline value of 0 V. Another way to implement it would be to use a microcontroller with on-chip DAC, or a digital potentiometer or DAC serially interfaced to the microcontroller.

The relationship between input voltage V_{in} and the output voltage V_o along with the correction voltage V_x is shown in Fig. 2, for (a) decreasing input and (b) increasing input. It is to be noted that drift cancellation has a hysteresis, and the actual output depends on the direction of input change.

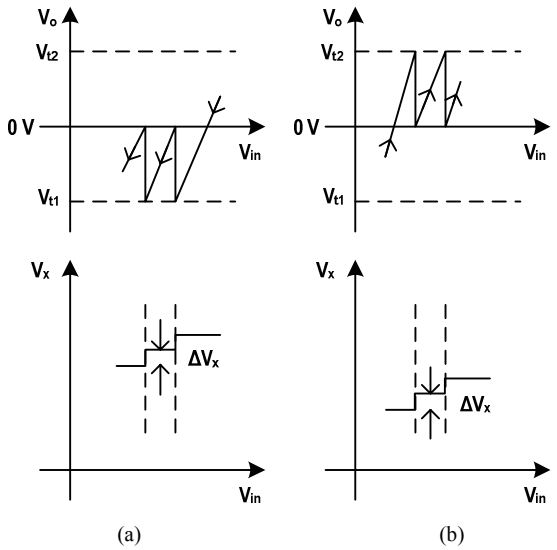

Fig. 2. Input-output relationship for (a) decreasing input and (b) increasing input.

III. Circuit Description

The circuit diagram of the microcontroller based implementation is shown in Fig. 3. The circuit uses quad op amp TL084 as U1 and 20-pin microcontroller AT89C2051 [11] as U2. This circuit has been developed for baseline drift removal in an impedance cardiograph [12]. The impedance cardiograph circuit works with ± 12 V supply. In addition to these two supply voltages, microcontroller requires 5 V supply.

Expected actual impedance cardiograph signal range is [-25, 30] mV and because of baseline drift the signal excursion can be [1.75, 5] V. For proper signal acquisition, the signal after drift reduction and amplification, should fit well within the ± 5 V input range of the ADC.

Op amp U1C is configured as a summer for the input voltage, V_{in}, with gain A_s, the reference voltage, V_{REF} with gain A_r, and the correction voltage, V_x, with gain $-A_x$.

$$V_o = V_{in}A_s + V_{REF}A_r - V_xA_x \quad (1)$$

where, $A_s = (R_2||R_3/(R_1+R_2||R_3))(1+R_5/R_4)$

$A_r = (R_1||R_2/(R_3+R_1||R_2))(1+R_5/R_4)$

$A_x = R_5/R_4$

The output V_o is compared with the threshold voltages V_{t1} and V_{t2}, with op amps U1A and U1B used as comparators. Threshold detector outputs are given to the port pins P1.0 and P1.1 of microcontroller U2. The tracking up/down counter of Fig. 2 is realized using software inside the microcontroller. The count value is output as PWM as an approximation to the baseline drift. The PWM pulses are low pass filtered by second order low pass filter formed by U1D.

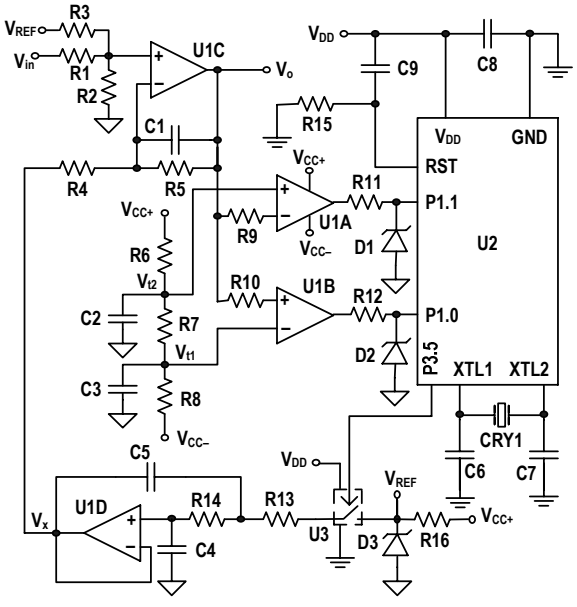

Fig. 3. Circuit diagram of the microcontroller based implementation.

In our implementation, the microcontroller operates with 24 MHz crystal. The 8-bit up/down counter and PWM output on port pin P3.5 are implemented through software, with PWM clock of 7.8 kHz. The duty cycle can be varied from 5% to 90% in 256 steps, in accordance with the counter output. The cutoff frequency of the low pass filter is selected as ≈ 60 Hz (<< 10 kHz), so that the output V_x, is ripple free. It is to be noted that because of the low pass filter, the tracking process has to wait for approximately 10 ms after each step change, before taking the next tracking step. A voltage reference D3 has been used to stabilize the amplitude of the PWM.

Let input consist of actual signal V_s superimposed on baseline drift V_d.

$$V_{in} = V_s + V_d \tag{2}$$

Input range is mapped to the output voltage, and hence the gain for the input signal is

$$A_s = (V_{t2}–V_{t1})/(V_{smax}–V_{smin}) \tag{3}$$

If the summer output crosses lower threshold V_{t1}, the comparator U1B is driven to positive saturation, producing high input to pin P1.0 of microcontroller U2. The duty cycle of PWM is decreased by a fixed percentage, corresponding to one step change in counter. Similarly, if V_o crosses the upper threshold V_{t2}, input P1.1 of microcontroller becomes high and the duty cycle of PWM is incremented by one step.

The correction voltage V_x is

$$\begin{aligned} V_x(t_{n+1}) &= V_x(t_n) + \Delta V_x,\ V_o(t_n) > V_{t2} \\ &\quad V_x(t_n) - \Delta V_x,\ V_o(t_n) < V_{t1} \\ &\quad V_x(t_n), \text{ otherwise.} \end{aligned} \tag{4}$$

For N steps in PWM output, the step voltage $\Delta V_x = (V_{smax}–V_{smin})/ N$ and is given by

$$\Delta V_x = 0.5(V_{t2}–V_{t1})/ A_x \tag{5}$$

This feedback voltage is used for baseline drift correction as per (1) to bring V_o within the threshold range. If V_o is still outside the range $[V_{t1}, V_{t2}]$, the process is repeated. If the output V_o is within the range $[V_{t1}, V_{t2}]$, both the comparator outputs are low, the count in the counter is not changed, the duty cycle of the PWM remains unchanged and the value of the correction voltage remains constant.

IV. Results

Component values shown in Fig. 3 were selected for threshold voltages of ± 4 V, signal gain of 55, correction voltage gain of 220 and reference voltage gain of 110.5. An example of drift cancellation by the implemented circuit is shown in Fig. 4. Input consisted of 15 mV (p-p) sine wave of 20 Hz superimposed on a dc offset of + 2 V with a triangular drift of 60 mV (p-p) and 0.5 Hz frequency. Output signal shows that the baseline has been restored and the drift is compensated when the signal crosses the threshold range. It is to be noted that the signal is not usable during the drift correction interval. The small amount of residual drift may require further signal processing.

Fig. 5 shows the output obtained when this circuit has been used in the impedance cardiograph instrument. The desired signal is the variation in impedance $z(t)$, superimposed on the basal impedance Z_o. It can be seen that the baseline of $z(t)$ signal has been restored and the drift in it is tracked whenever it crosses the threshold range. Derivative of $z(t)$ is known as impedance cardiogram (ICG) and is used for stroke volume calculation and obtaining diagnostic information on the functioning of cardiovascular system.

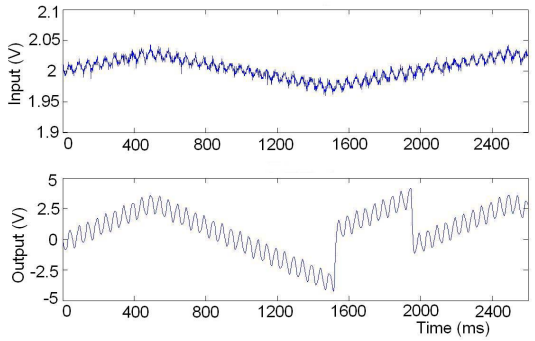

Fig. 4. Example of drift cancellation.

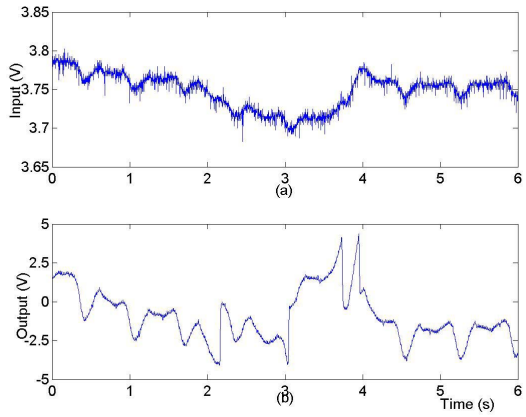

Fig. 5 Output of baseline restoration circuit for the varying impedance signal, $Z(t)$ ($Z_o + z(t)$) from an impedance cardiograph (a) Input (b) Output.

V. Conclusion

For restoration of baseline and suppressing its low frequency drift in bioimpedance signals, a tracking based baseline restoration circuit is developed. Since the logic and PWM is implemented in software with an 8-bit microcontroller with in-built timers, the hardware requirement is simplified. Although the circuit has been used for impedance cardiography, it can be used in other applications also where the signal has a large baseline which can drift. This circuit is independent of the processor to which the signal acquisition unit is interfaced and can be used in set-ups with real time as well as offline processing. In the present implementation, tracking of baseline is initiated by the output going out of the defined range. Alternatively, the microcontroller can be programmed to carry out the tracking for drift cancellation at periodic intervals, and this may be appropriate for certain applications.

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