FPGA-Based Design of a Hearing Aid with Frequency Response Selection through Audio Input

Shankarayya G. Kambalimath [1], Prem C. Pandey [2], Pandurangarao N. Kulkarni [1,]
Shivaling S. Mahant-Shetti [3], and Sangamesh G. Hiremath [4]

[1] Dept. of Electronics & Comm. Engg., Basaveshwar Engg. College, Bagalkot, Karnataka, India
[2] Dept. of Electrical Engg., Indian Institute of Technology Bombay, Mumbai, India
[3] Karnataka Microelectronics Design Center, Manipal, Karnataka, India
[4] G.M. Institute of Technology, Davangere, Karnataka, India
<kambalimathsg@rediffmail.com>, <pcpandey@ee.iitb.ac.in>, <pnk_bewoor@yahoo.com>, <mahant@karmic.co.in>, <dr_sgh@yahoo.co.in>

***Abstract*—Hearing aids provide frequency-selective amplification to compensate for the elevated hearing thresholds and automatic volume control to partly compensate for the significantly reduced dynamic range of hearing. The response selection controls of these devices are not easy to access during their normal use. To address this problem, an FPGA-based design of a hearing aid is presented, with frequency response selection by DTMF coded sound from a hand-held device without using switches, ports, or additional hardware. The audio input is given to two parallel processing blocks. The first block is a DTMF detector employing Goertzel algorithm and outputs control bits for selecting one of the pre-stored responses. The second block processes the signal for frequency-selective amplification and produces the audio output. The filter is designed as an FIR filter with its magnitude response approximating the product of the responses required for hearing-loss compensation and noise attenuation. It is efficiently realized using a processing architecture employing sequential multiply-accumulate operations. The design is implemented using FPGA "Altera Cyclone IV EP4CE115F29C7" and an audio codec and verified for satisfactory operation.**

Keywords—DTMF detector; FPGA based signal processing; hearing aid.

I. INTRODUCTION

Persons with sensorineural hearing loss experience degraded speech perception and find it to difficult to adapt to different listening conditions. The currently available digital hearing aids provide frequency-selective amplification to compensate for the elevated hearing thresholds and automatic volume control to partly compensate for the significantly reduced dynamic range of hearing [1]. They generally have a set of filter responses to partly compensate for the different adverse listening conditions and for suppressing significant spectral components of the noise. However, the selection controls are not easy to access during their normal use. As optical and RF links require additional hardware in the device and are not useable when it resides in the ear canal, an audio controlled selection can be of great help to the hearing aid user.

For reducing the size and power, hearing aids are designed using ASICs and an FPGA-based prototyping and testing is helpful in significantly reducing the development time and nonrecurring cost [2]. Hence, an FPGA-based design of a hearing aid is presented, with the response selection by dual-tone multi-frequency (DTMF) coded sounds from a hand-held device. The control signal is input through the same microphone, pre-amplifier, and ADC as used for speech. Goertzel algorithm-based DTMF detection [3]−[5] is used as it is not affected much by speech and environmental noise.

II. DESIGN AND IMPLEMENTATION

Realization of hearing loss compensation filter as a parallel bank of IIR band-pass filters, with adjustable gains to obtain the desired magnitude response, results in nonlinear phase response. FIR filter design, although requiring a relatively higher order, permits coupling an almost arbitrary magnitude response with a linear phase response. We use a linear-phase FIR filter, with the magnitude response approximating the product of the responses required for hearing-loss compensation and noise attenuation. A single filter helps in reducing the signal delay. The loss compensation response is obtained from the audiogram, by linear interpolation of the gains desired at the audiometric test frequencies. Four noise attenuation responses are devised: neutral or all pass (AP), low pass (LP) with 6 dB/octave tilt above 2 kHz to suppress high-frequency noise, high-pass (HP) with 6 dB/octave tilt below 500 Hz to suppress low-frequency noise, and band-pass (BP) as a cascade of LP and HP. The sets of filter coefficients are calculated by iterative application of frequency sampling technique and are stored. The set of coefficients for the appropriate response is selected through DTMF coded sounds from a handheld device.

The design is implemented using an FPGA board with audio codec "WM8731" and FPGA "Altera Cyclone IV FPGA EP4CE11529C7". The audio input with sampling frequency of 10 kHz is applied, as shown in Fig. 1, to two parallel processing blocks: (i) DTMF detector with output control bits for selecting one of the pre-stored set of filter coefficients and (ii) FIR filter for frequency-selective amplification.

A DTMF signal is a sum of two harmonically unrelated tones, one from four "row" frequencies and the other from four "column" frequencies. The DTMF detector, shown in Fig. 2, has a set of four Goertzel filter blocks for row frequencies and another such set for column frequencies, each with a second order IIR filter and 250-sample energy calculation. The detector generates 2-bit row and 2-bit column output. Only 4 out of 16 codes are used at present. The bits are applied as input to the ROM containing four sets of filter coefficients each consisting of 513 coefficients.

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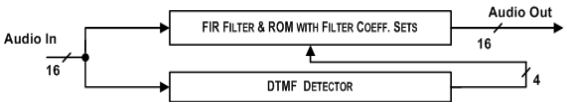

Fig. 1. Hearing aid response selection through DTMF audio input.

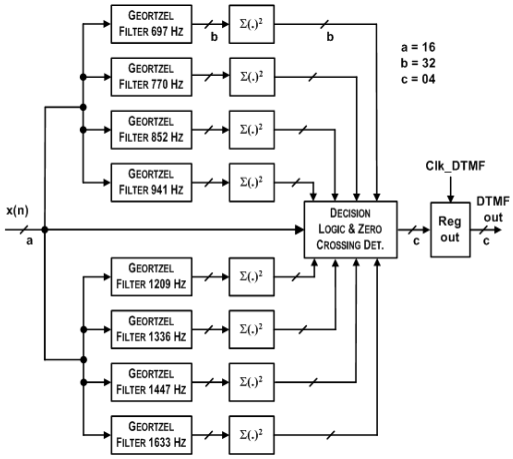

Fig. 2. Goertzel filter based DTMF detector.

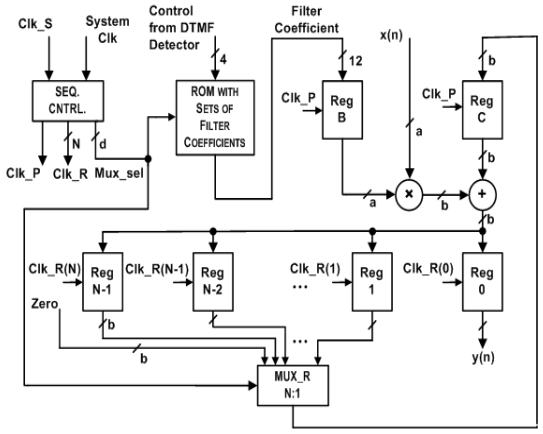

Fig.3. FIR filter architecture with sequential multiply-accumulate operations. Clk S: Samp. Clock; Clk P: Proccess. Clock; a=16; b=32.

For FPGA-based FIR filter design, three architectures were investigated in [6]: direct-form, transposed-form, and using sequential multiply-accumulate operations. The last one makes optimal use of the hardware and requires lesser resources. It is used in the current design, as shown in Fig. 3. It consists of two buffer registers (Reg-B, Reg-C), a multiplier, an adder, N registers (Reg-I, I = 0, 1, 2,....N-1) for intermediate results, and multiplexer MUX-R. The operation is sequenced by the controller SEQ.CNTRL, with the sampling clock CLK_S and the System Clock as the inputs. It outputs the cycle clock CLK_P, register load clocks CLK_R(I) ($0 < I < N-1$), and multiplexer control MUX_sel. There are N processing clocks during each sampling interval. Each of the register load clocks are generated in successive processing cycles. Active edges of CLK_R and CLK_P are out of phase. The MUX_sel is changed sequentially in phase with the processing clock. In each processing cycle, the input sample $x(n)$ is multiplied with the coefficient from the ROM and added to the corresponding register content.

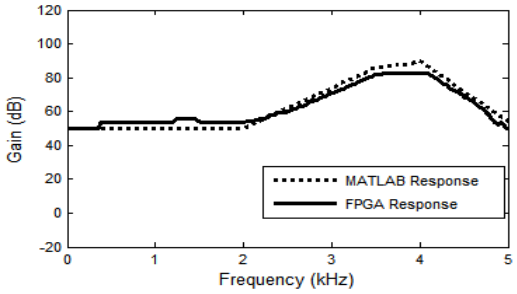

Fig. 4. Magnitude responses of hearing loss compensation filters.

III. Test Results

The FPGA-based implementation has been tested for realizing the loss compensation filter for a number of audiograms and coupled with four noise attenuation filters. Magnitude responses of these filters, measured using swept sinusoidal tone as input, showed close match with the corresponding desired magnitude responses. An example of the filter responses is shown in Fig. 4. DTMF detector was found to work satisfactory even in the presence of 0 dB broad-band noise. Resources of the Altera FPGA EP4CE115F29C7 utilized in the implementation are: 65% logic elements, 58% combinational functions, 15% dedicated logic registers, 1% memory bits, and 21% embedded multipliers. Use of sequential multiply-accumulate operations for FIR filters has significantly reduced the resource requirement, with a scope for implementing other processing blocks of the hearing aid.

IV. Conclusions

An FPGA-based design of a hearing aid has been presented in which the appropriate response can be selected through DTMF coded sound without having to physically access the device. Future work involves providing volume control, converting the FPGA-based implementation to an ASIC suitable for hearing aids, and clinical evaluation.

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