Automatic Test Pattern Generation - IV

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EE 709: Testing & Verification of VLSI Circuits

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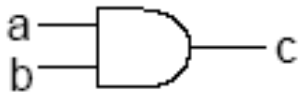
ATPG - Algorithmic

- Path Sensitization Method
  - Fault Sensitization
  - Fault Propagation
  - Line Justification

- Path Sensitization Algorithms
  - D- Algorithm (Roth)
  - PODEM (P. Goel)
  - FAN (Fujiwara)
  - SOCRATES (Schultz)
  - SPIRIT (Emil & Fujiwara)

Common Concept

- Fault Activation problem → a LJ Problem
- The Fault Propagation problem →
  1. Select a FP path to PO → Decision
  2. Once the path is selected → a set of LJ problems
- The LJ Problems → Decisions or Implications



To justify c = 1 → a = 1, b = 1 (Implication)

To justify c = 0 → a = 0 or b = 0 (Decision)

- Incorrect decision → Backtrack → Another decision

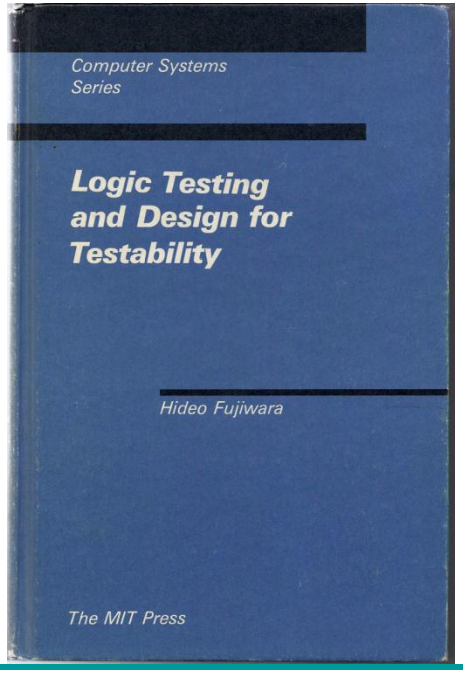
FANout oriented test generation

FAN

(Fujiwara & Shimono, 1983)

Prof. Hideo Fujiwara

- Prof. Fujiwara is Eminent Researcher and Academician in VLSI Testing
- Many contributions to VLSI Testing
- Co-founder of ATS and WRTLT
- Special Workshop was organized in his honour with 20th IEEE ATS 2011



TG Algorithms

Objective

- TG time reduction
  - Reduce number of backtracks
  - Find out the non-existence of solution as soon as possible
  - Branch and bound

FAN Algorithm

- **New concepts:**
  - **Immediate assignment of *uniquely-determined signals***
  - ***Unique sensitization***
  - **Stop Backtrace at *head lines***
  - ***Multiple Backtrace***

FAN Algorithm

Strategies:

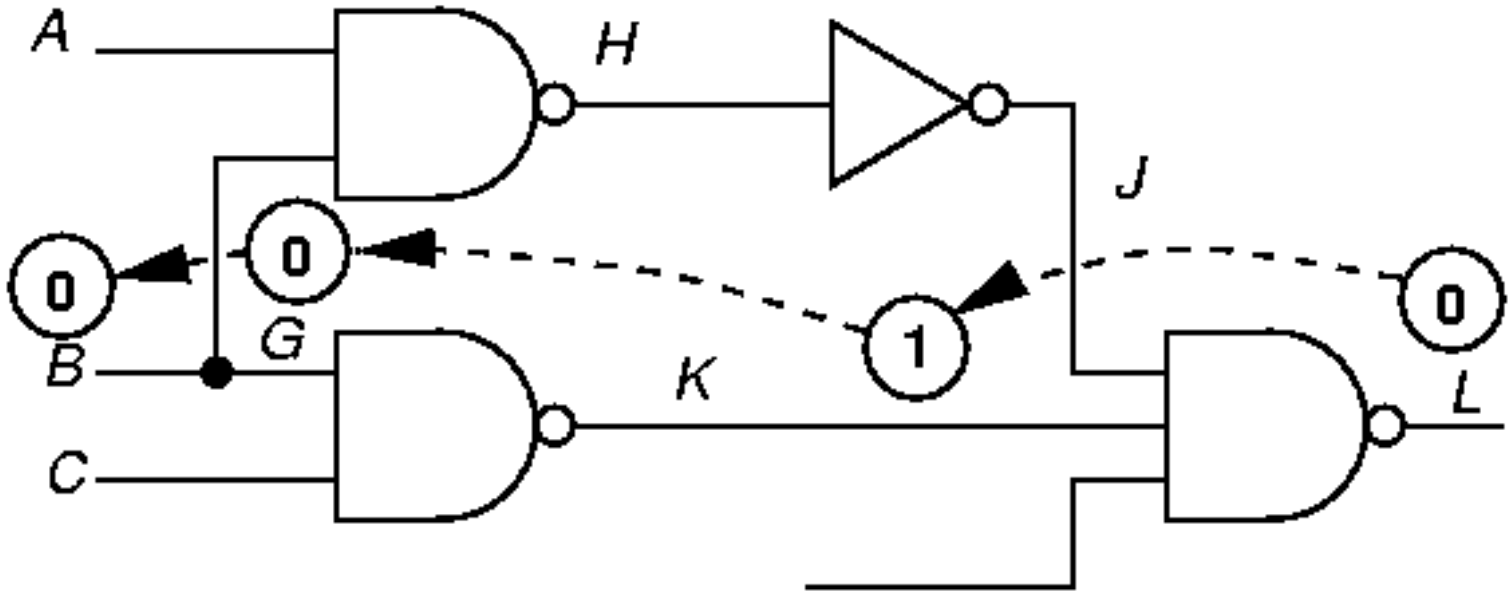
Strategy1:

- In step of the algorithm determine as many signal values as possible
  - Implication

Strategy 2:

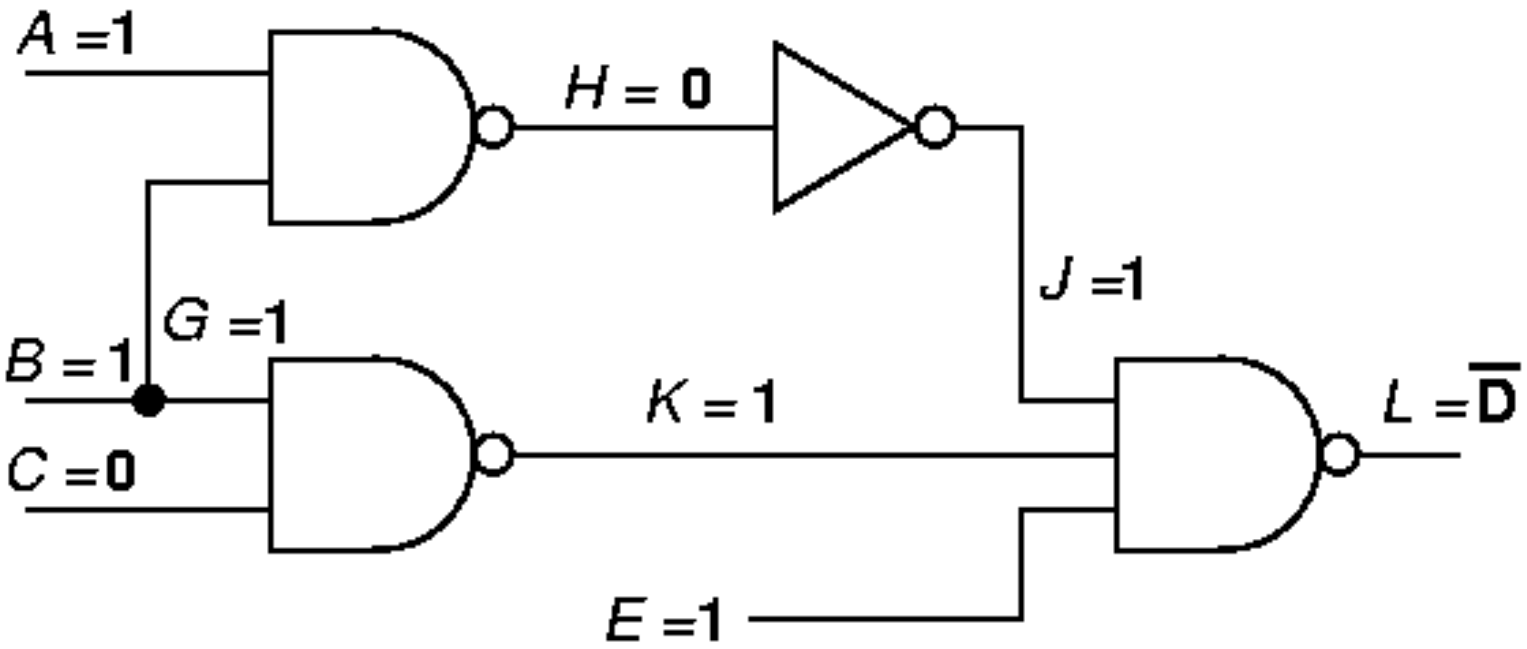
- Assign faulty signal D or D’ that is uniquely determined or implied by the fault in question

PODEM Fails to Determine Unique Signals



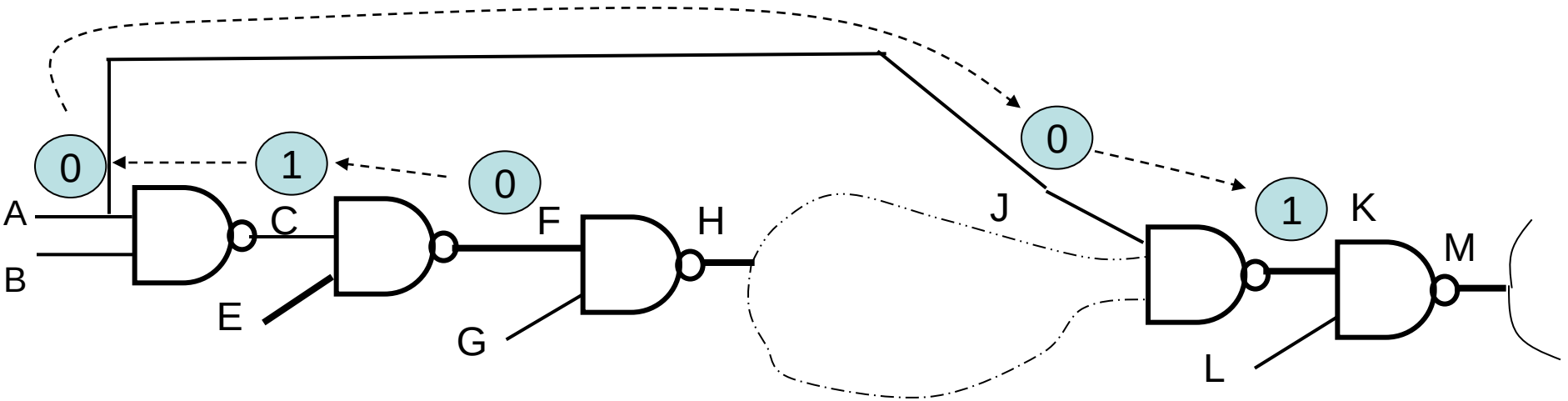
- **Backtracing operation fails to set all 3 inputs of gate *L* to 1**
  - **Causes unnecessary search**

FAN -- Early Determination of Unique Signals



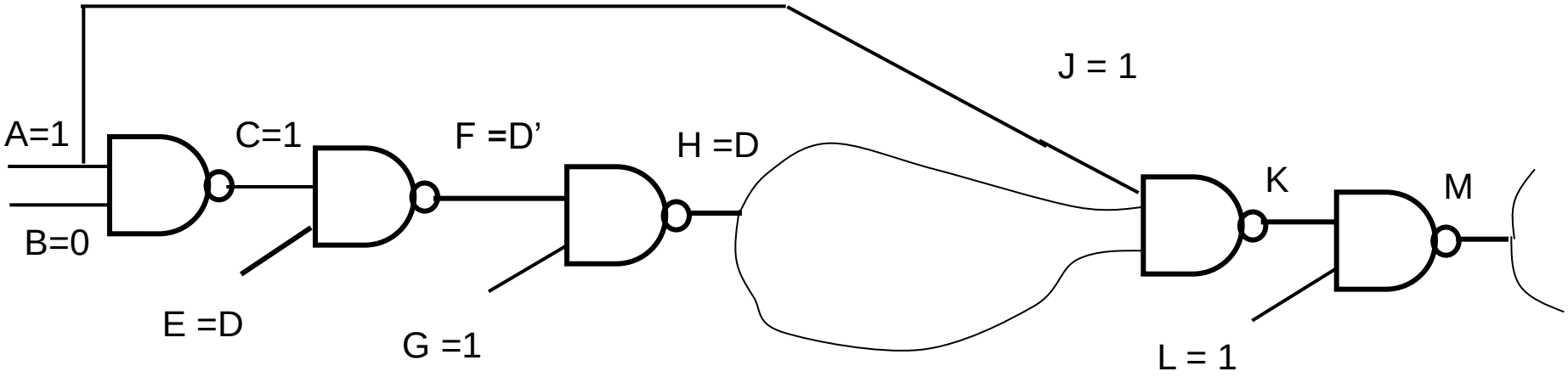
- **Determine all unique signals implied by current decisions immediately**
  - **Avoids unnecessary search**

PODEM Makes Unwise Signal Assignments



- Blocks fault propagation due to assignment $J = 0$

FAN – Unique sensitization



- FAN immediately sets necessary signals to propagate fault

Unique sensitization and implication

Partial sensitization, which uniquely determined, is called unique sensitization

FAN Algorithm

Strategies:

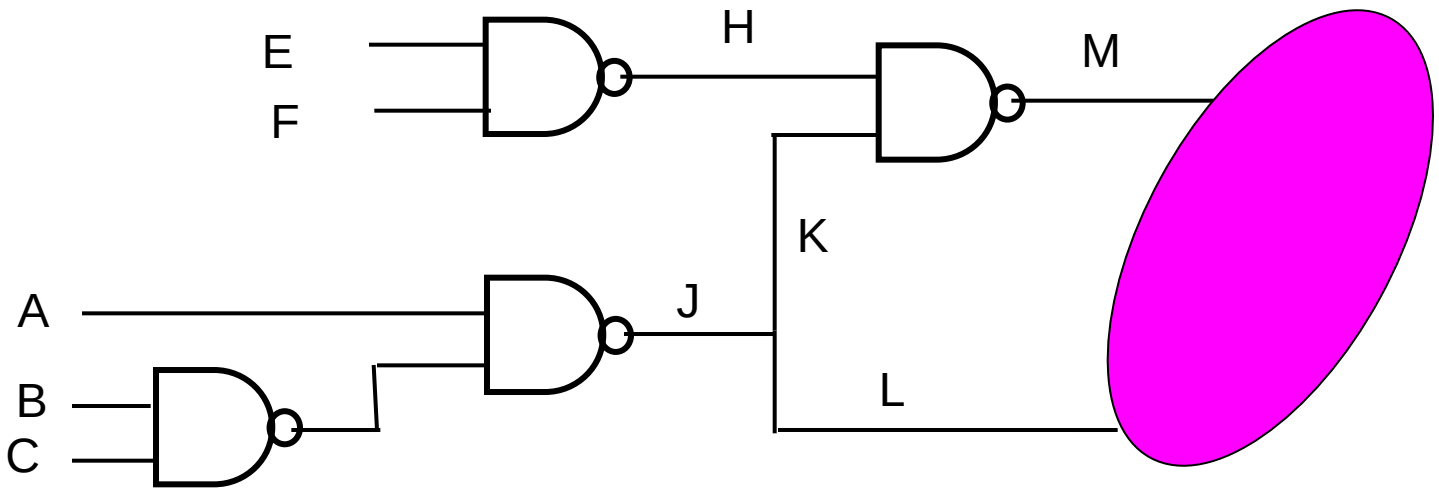
Strategy 3:

- When the D-frontier consists of a single gate, apply a unique sensitization

Strategy 4:

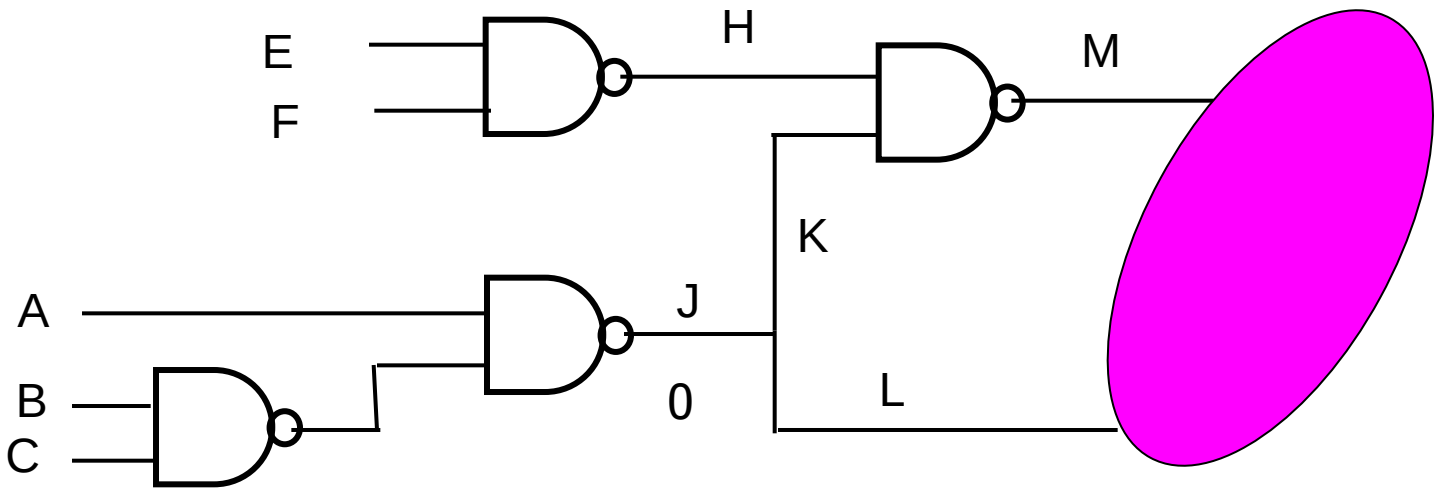
- Stop the backtrace at a *headline*, and postpone the line justification for the *headline* to later

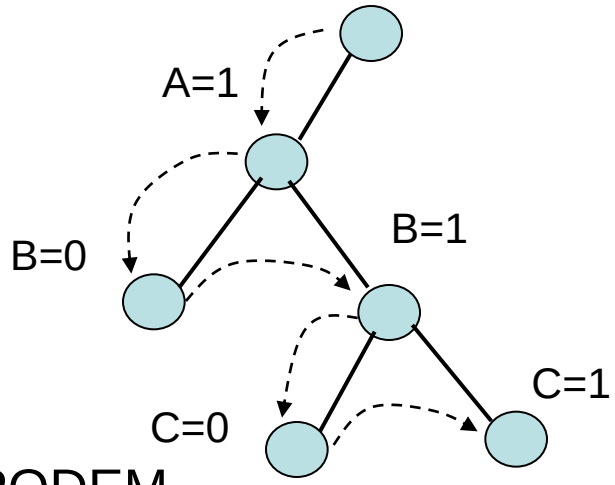
Headlines



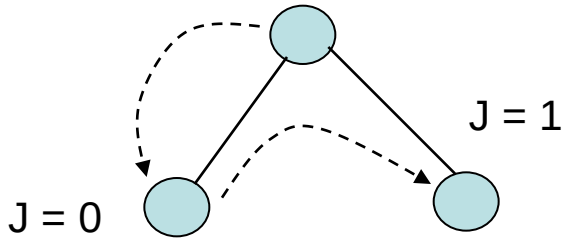
- When a line L is reachable from a fanout point, L is said to be bound
- A signal line that is not bound is said to be free
- When a line is adjacent to some bound line, it is said to be head line

Decision Trees





PODEM



Backtracking at Head-lines

FAN Algorithm

Strategies:

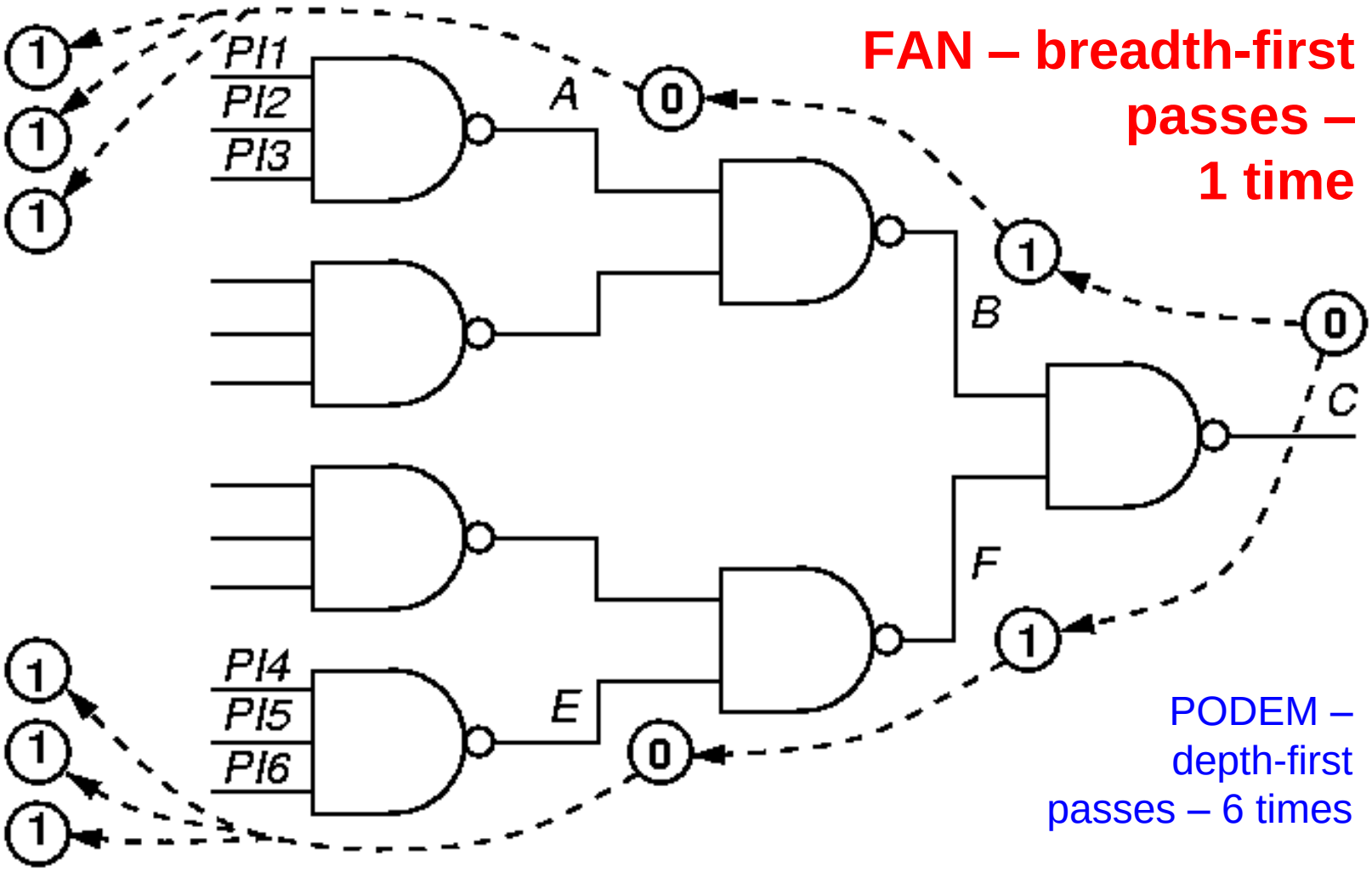
Strategy 5:

- Multiple backtracing (concurrent backtracing of more than one path) is more efficient than backtracing along a single path

Objective for multiple backtrace

- Triplet
- (s, $n_0(s)$, $n_1(s)$)

Multiple Backtrace



FAN Algorithm

Objective for multiple backtrace

- Triplet
- (s, $n_0(s)$, $n_1(s)$)

AND gate

- Let X be the easiest to set to 0 input

$n_0(X) = n_0(Y)$, $n_1(X) = n_1(Y)$

For other inputs X_i

$n_0(X_i) = 0$, $n_1(X_i) = n_1(Y)$

OR gate

Let X be the easiest to set to 1 input

$n_0(X) = n_0(Y)$, $n_1(X) = n_1(Y)$

For other inputs X_i

$n_0(X_i) = n_0(Y)$, $n_1(X_i) = 0$

FAN Algorithm

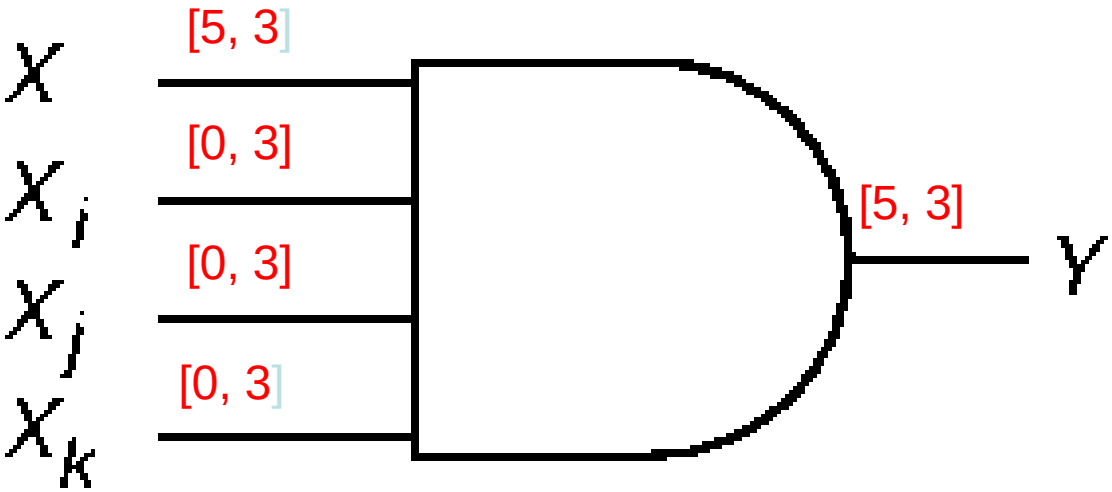
NOT gate

$n_0(X) = n_1(Y),\ \ n_1(X) = n_0(Y)$

Fanout points

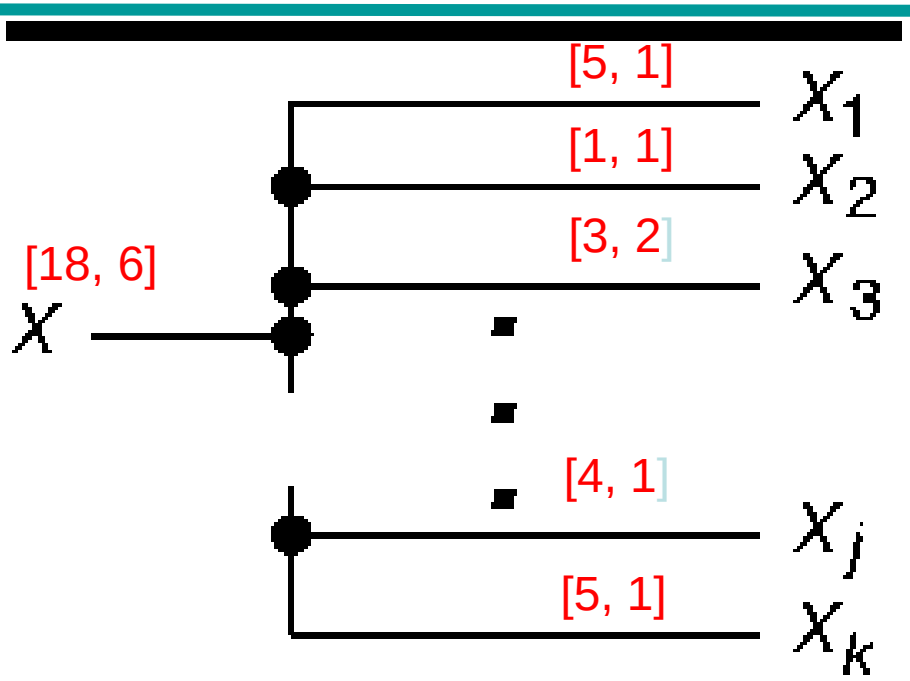
$n_0(X) = \Sigma\ n_0(X_i),\ \ n_1(X) = \sum n_1(X_i)$

AND Gate Vote Propagation



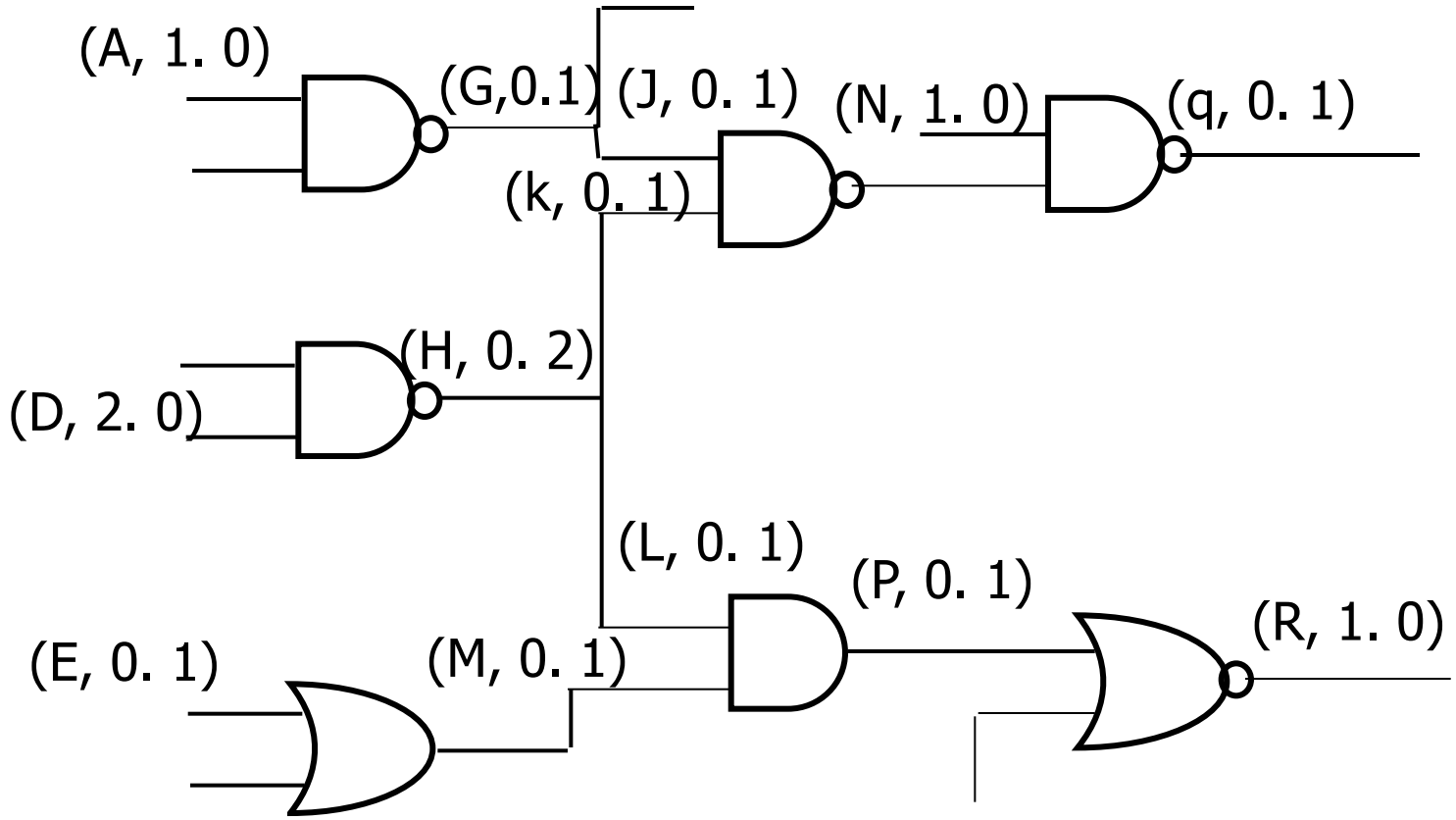
- **AND Gate**
  - **Easiest-to-control Input –**
    - **# 0's = OUTPUT # 0's**
    - **# 1's = OUTPUT # 1's**
  - **All other inputs --**
    - **# 0's = 0**
    - **# 1's = OUTPUT # 1's**

Multiple Backtrace Fanout Stem Voting



- **Fanout Stem --**
  - **# 0's = Σ Branch # 0's,**
  - **# 1's = Σ Branch # 1's**

FAN



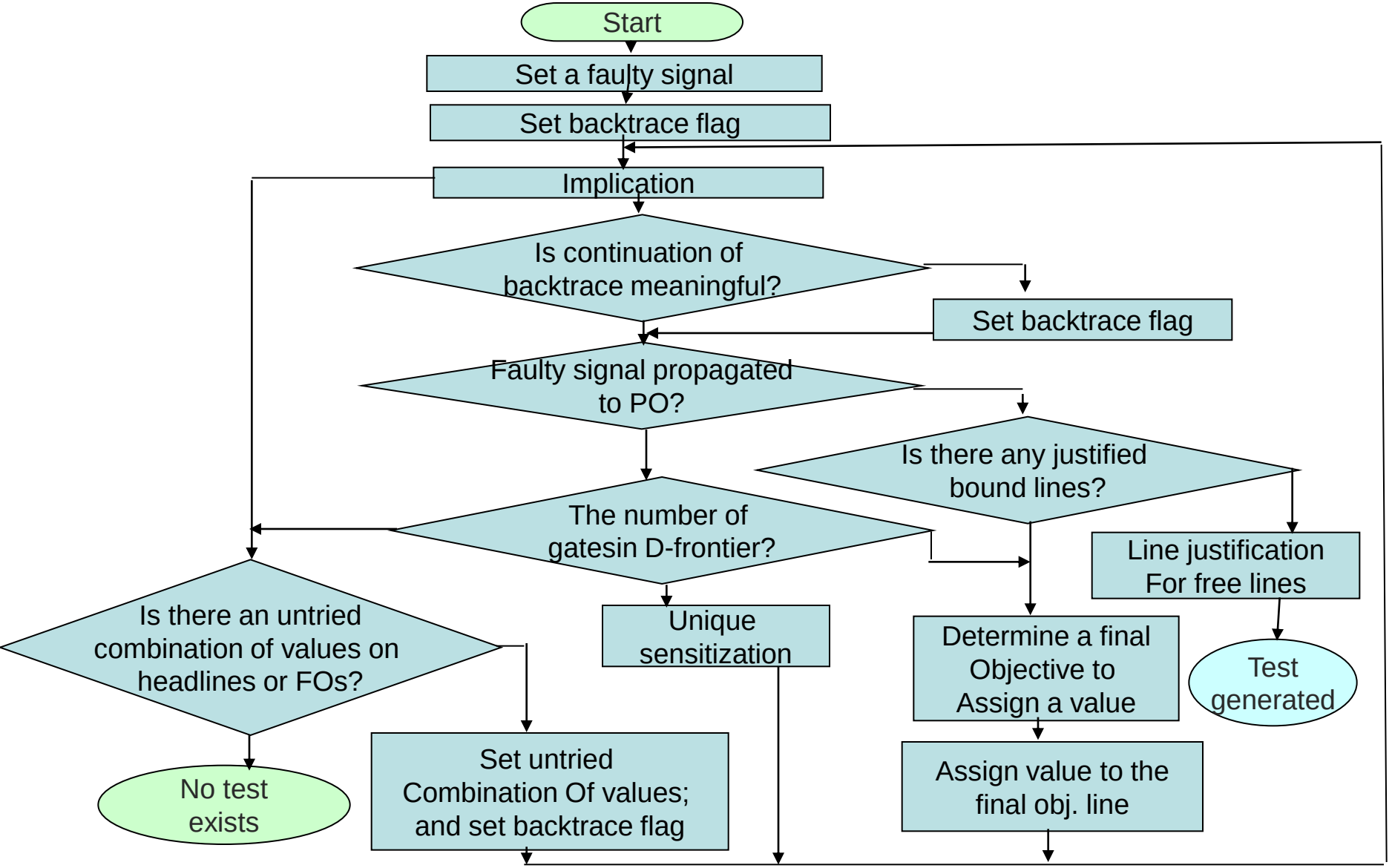
FAN Algorithm

Strategies:

Strategy 6:

- In the multiple backtrace, if an objective at a fanout point *p* has a contraditory requirement, that is, if both $n_0(p)$ and $n_1(p)$ are non-zero, stop backtrace so as to assign a binary value to the fanout point.

FAN - Algorithm



Static and Dynamic Compaction of Sequences

- **Static compaction**
  - **ATPG should leave unassigned inputs as X**
  - **Two patterns *compatible* – if no conflicting values for any PI**
  - **Combine two tests t_a and t_b into one test $t_{ab} = t_a \cap t_b$ using D-intersection**
  - **Detects union of faults detected by t_a & t_b**
- **Dynamic compaction**
  - **Process every partially-done ATPG vector immediately**
  - **Assign 0 or 1 to PIs to test additional faults**

Compaction Example

- t_1 = 0 1 X t_2 = 0 X 1
  t_3 = 0 X 0 t_4 = X 0 1

- **Combine t_1 and t_3, then t_2 and t_4**
- **Obtain:**
  - t_{13} = 0 1 0 t_{24} = 0 0 1

- ***Test Length* shortened from 4 to 2**

Thank You