Scan Design

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EE 709: Testing & Verification of VLSI Circuits

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Sequential Circuits

- A sequential circuit has memory in addition to combinational logic
- Test for a fault in a sequential circuit is a sequence of vectors, which
  - Initializes the circuit to a known state
  - Activates the fault, and
  - Propagates the fault effect to a PO
- Methods of sequential circuit ATPG
  - Time-frame expansion methods
  - Simulation-based methods

Difficulties in Seq. ATPG

- Poor initializability.
- Poor controllability/observability of state variables.
- Gate count, number of flip-flops, and sequential depth do not explain the problem.
- Cycles are mainly responsible for complexity.
- An ATPG experiment:

Circuit	Number of gates	Number of flip-flops	Sequential depth	ATPG CPU s	Fault coverage
TLC	355	21	14*	1,247	89.01%
Chip A	1,112	39	14	269	98.80%

** Maximum number of flip-flops on a PI to PO path*

Benchmark Circuits

Circuit	s1196	s1238	s1488	s1494
PI	14	14	8	8
PO	14	14	19	19
FF	18	18	6	6
Gates	529	508	653	647
Structure	Cycle-free	Cycle-free	Cyclic	Cyclic
Sequential depth	4	4	--	--
Total faults	1242	1355	1486	1506
Detected faults	1239	1283	1384	1379
Potentially detected faults	0	0	2	2
Untestable faults	3	72	26	30
Abandoned faults	0	0	76	97
Fault coverage (%)	99.8	94.7	93.1	91.6
Fault efficiency (%)	**100.0**	**100.0**	**94.8**	**93.4**
Max. sequence length	3	3	24	28
Total test vectors	313	308	525	559
Gentest CPU s (Sparc 2)	10	15	19941	19183

Finite State Machines

- A fault in a machine M_0 transforms into another machine M_i with n or fewer states
- A test sequence is a sequence of inputs that distinguishes M_0 from each of M_i defined by a fault
- A synchronizing sequence for a sequential machine M is an input sequence whose application is guaranteed to leave M in a certain final state irrespective of initial state of M
- A homing sequence for M is an input sequence whose application makes it possible to determine the final state of M by observing the corresponding output sequence that M produces

Finite State Machines

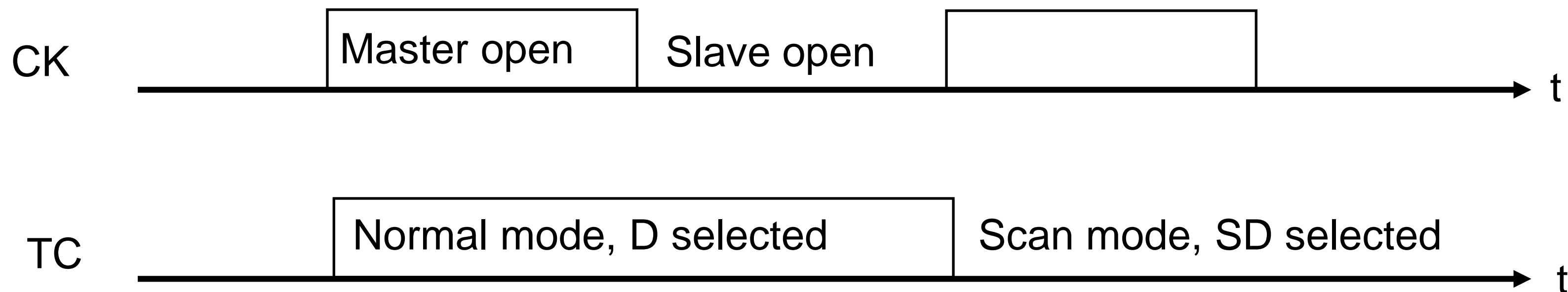
- A distinguishing sequence is an input sequence whose application makes it possible to determine the initial state of M by observing the corresponding output sequence M produces
- A test sequence is a sequence of inputs that distinguishes M_0 from each of M_i defined by a fault
- Test sequence can be generated from the counter example of equivalence of M_0 and M_i

Scan Design

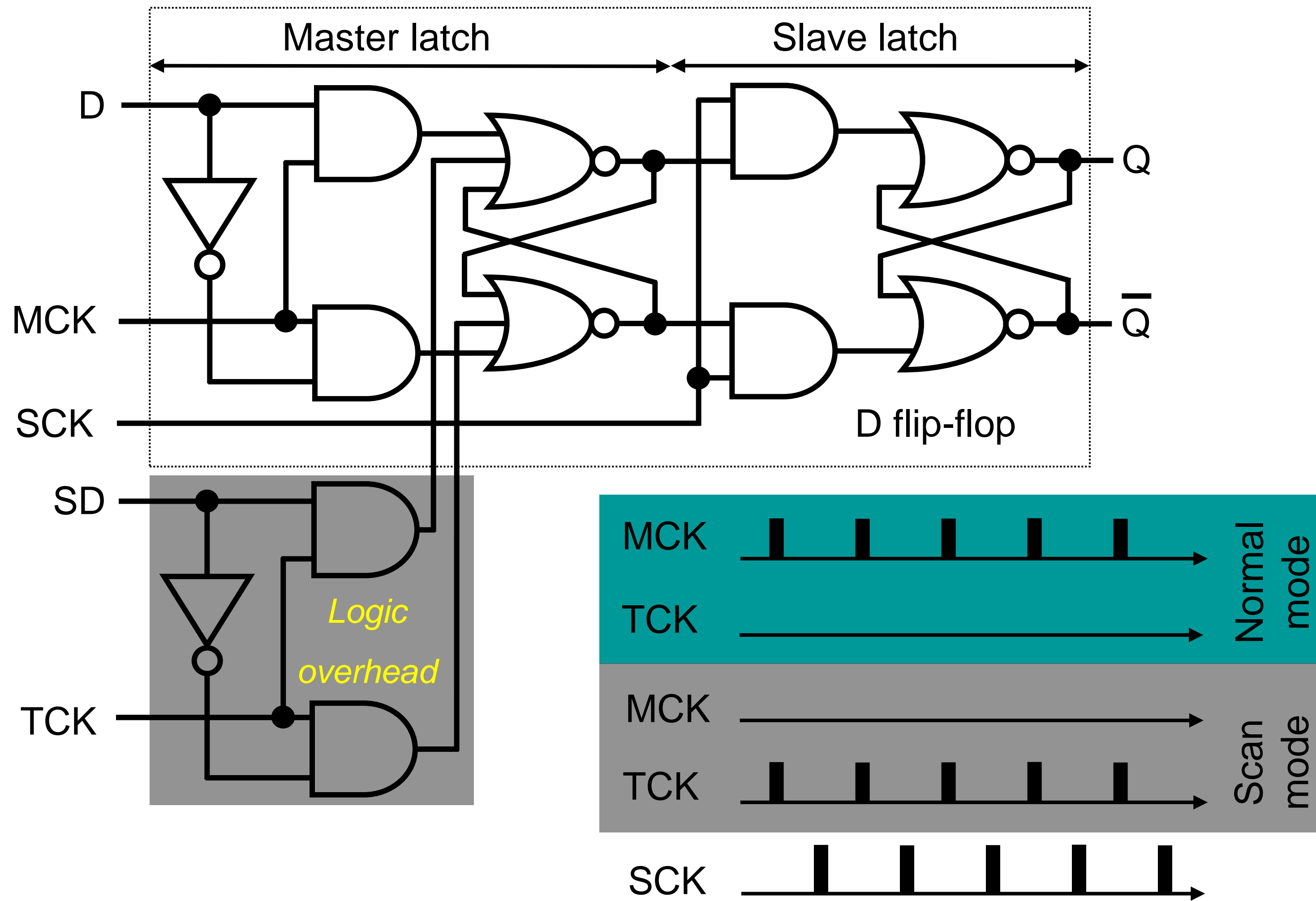
- Circuit is designed using pre-specified design rules.
- Test structure (hardware) is added to the verified design:
  - Add a *test control* (TC) primary input.
  - Replace flip-flops by *scan flip-flops* (SFF) and connect to form one or more shift registers in the test mode.
  - Make input/output of each scan shift register controllable/observable from PI/PO.
- Use combinational ATPG to obtain tests for all testable faults in the combinational logic.
- Add shift register tests and convert ATPG tests into scan sequences for use in manufacturing test.

Scan Flip-Flop (SFF)

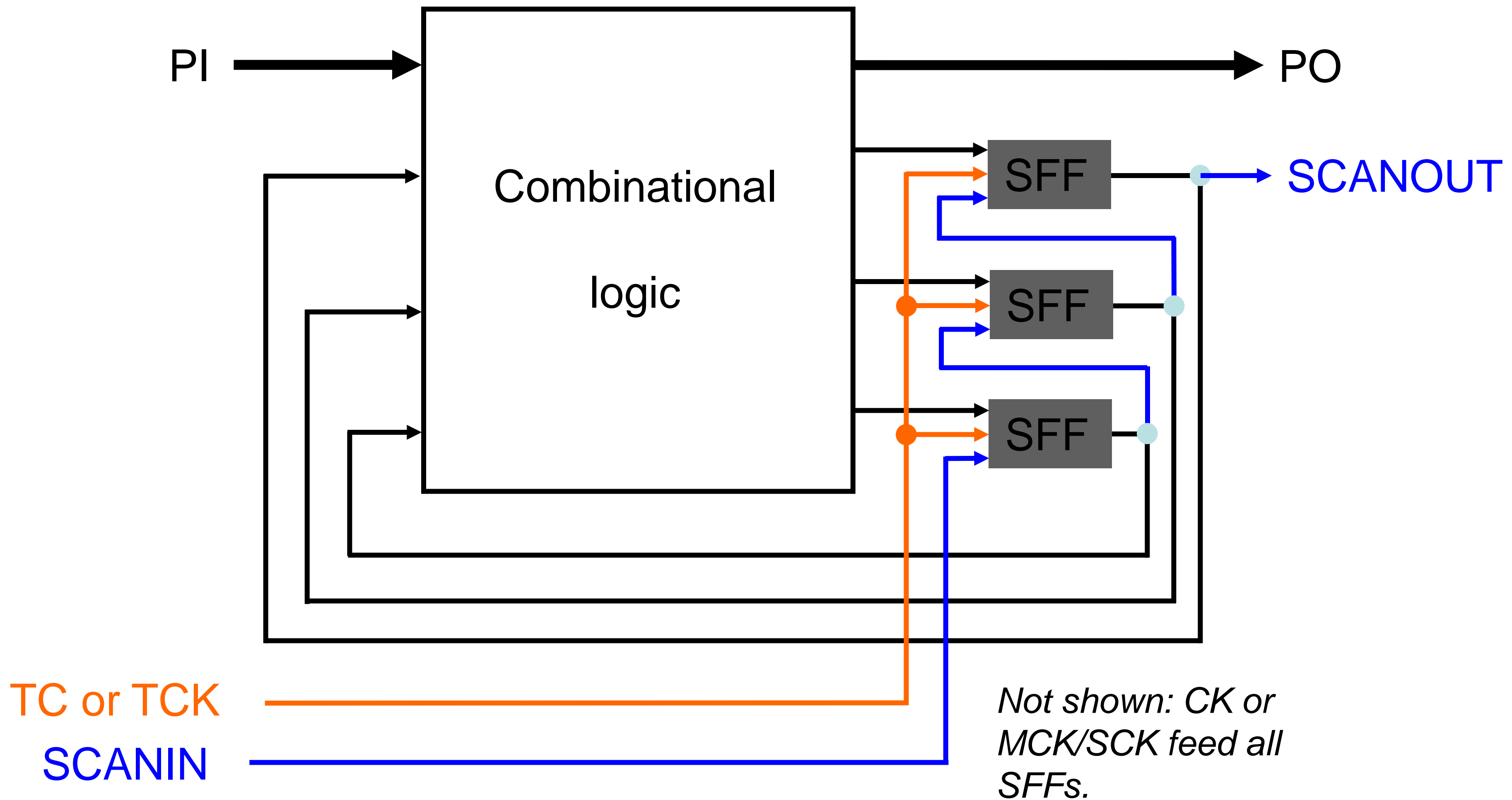
D
TC
Logic overhead
MUX
SD
CK
Master latch
Slave latch
Q
$\overline{Q}$
D flip-flop



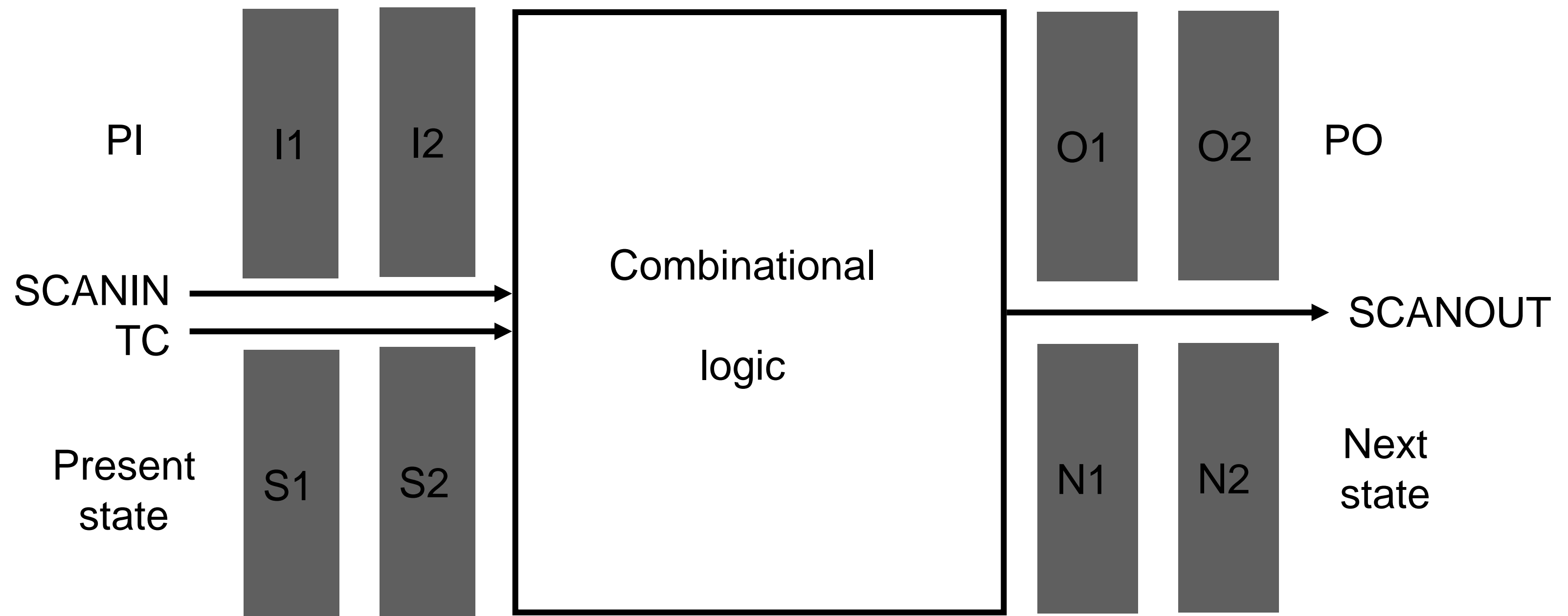
Level-Sensitive Scan-Design Flip-Flop (LSSD-SFF)



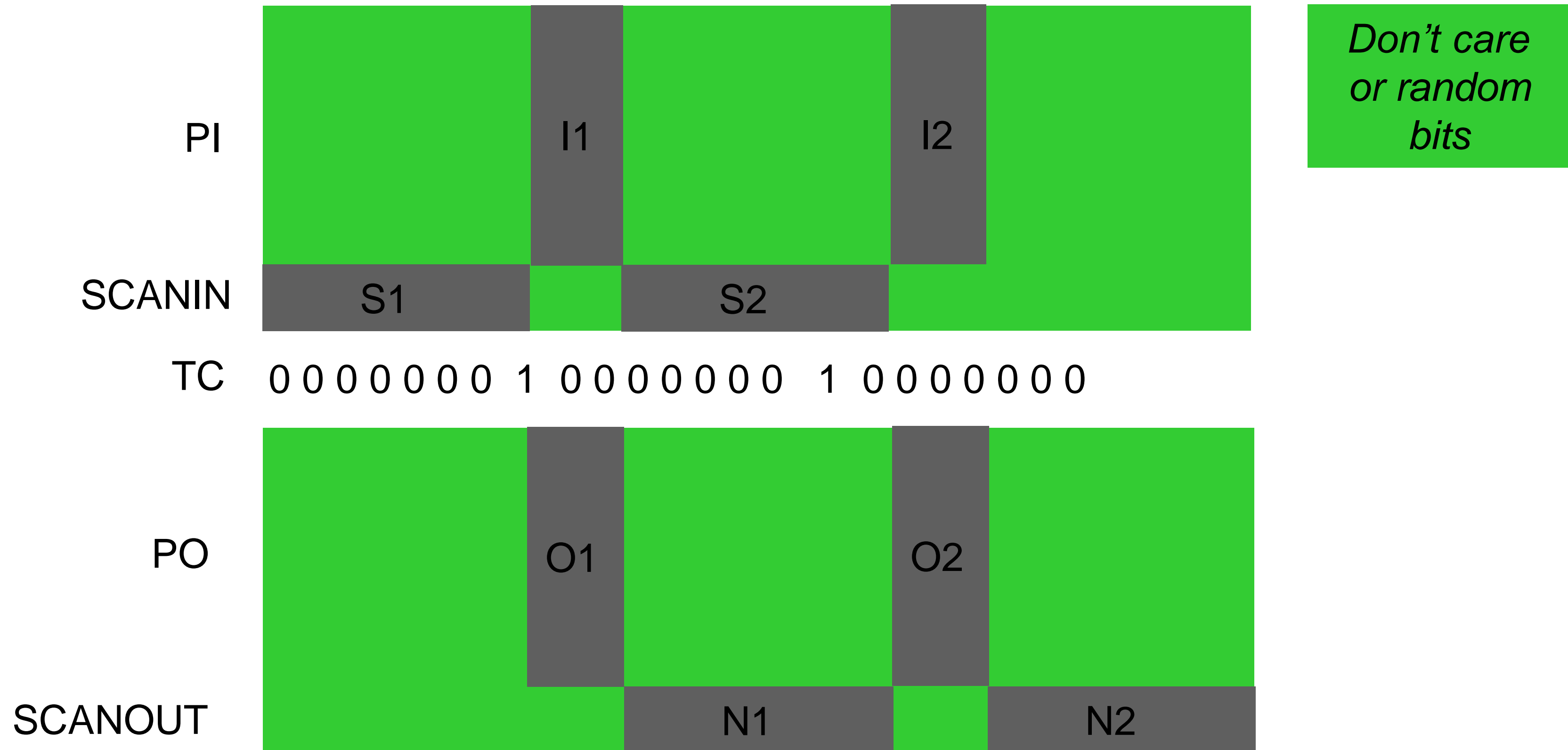
Adding Scan Structure



Comb. Test Vectors



Comb. Test Vectors



Sequence length = $(n_{comb} + 1)\, n_{sff} + n_{comb}$ *clock periods*

n_{comb} = number of combinational vectors

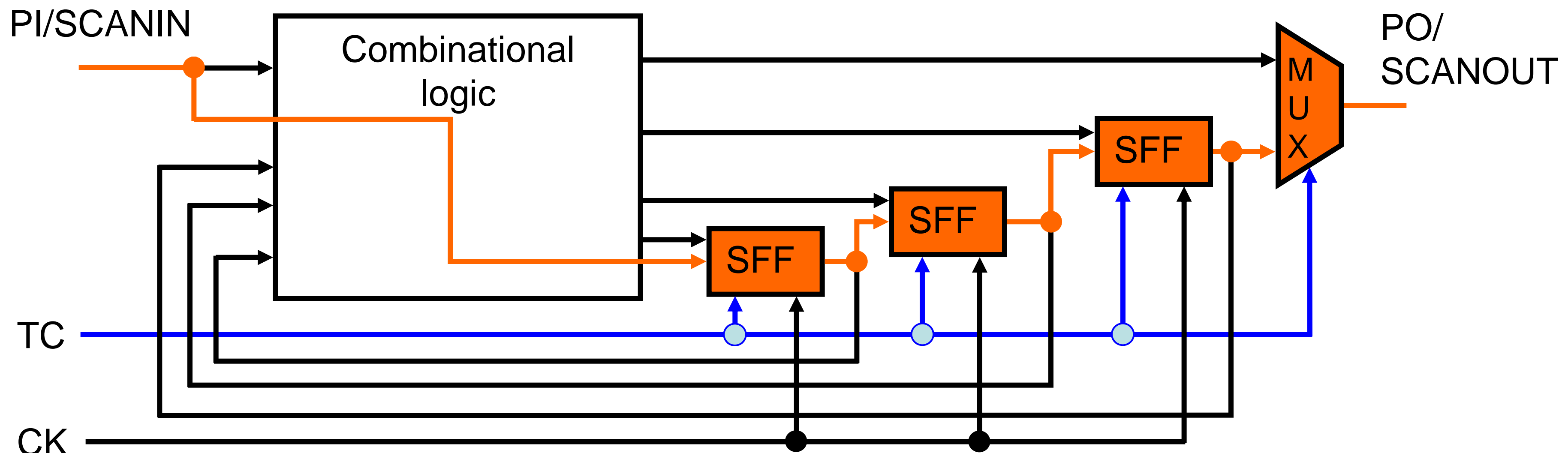
n_{sff} = number of scan flip-flops

Testing Scan Register

- Scan register must be tested prior to application of scan test sequences.
- A shift sequence 00110011 . . . of length n_{sff}+4 in scan mode (TC=0) produces 00, 01, 11 and 10 transitions in all flip-flops and observes the result at SCANOUT output.
- Total scan test length: $(n_{comb} + 2)\, n_{sff} + n_{comb} + 4$ *clock periods*.
- Example: 2,000 scan flip-flops, 500 comb. vectors, total scan test length ~ 10^6 clocks.
- Multiple scan registers reduce test length.

Multiple Scan Registers

- Scan flip-flops can be distributed among any number of shift registers, each having a separate *scanin* and *scanout* pin.
- Test sequence length is determined by the longest scan shift register.
- Just one *test control* (TC) pin is essential.

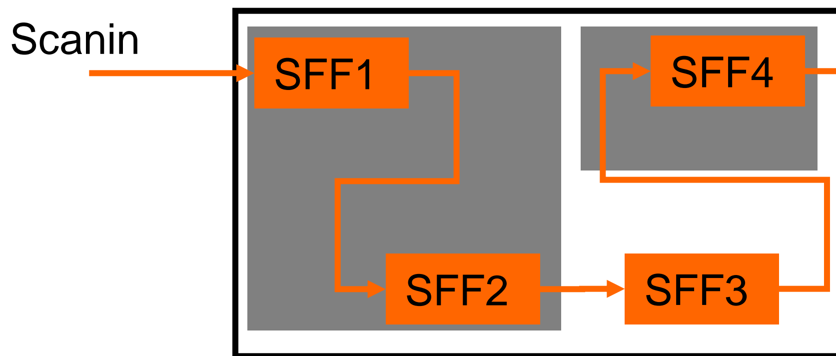


Scan Overheads

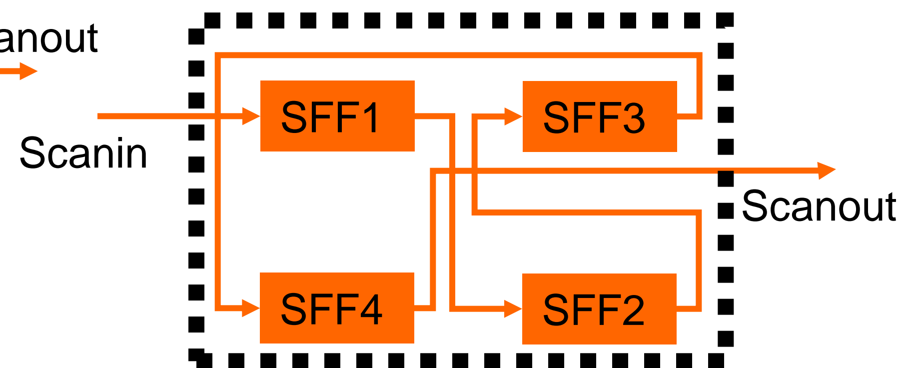
- IO pins: One pin necessary.
- Area overhead:
  - *Gate overhead* = $[4\, n_{sff}/(n_g+10n_{ff})] \times 100\%$, where n_g = *comb. gates*; n_{ff} = *flip-flops*; Example – n_g = 100k gates, n_{ff} = 2k *flip-flops*, overhead = 6.7%.
  - More accurate estimate must consider scan wiring and layout area.
- Performance overhead:
  - Multiplexer delay added in combinational path; approx. two gate-delays.
  - Flip-flop output loading due to one additional fanout; approx. 5-6%.

Hierarchical Scan

- Scan flip-flops are chained within subnetworks before chaining subnetworks.
- Advantages:
  - Automatic scan insertion in netlist
  - Circuit hierarchy preserved – helps in debugging and design changes
- Disadvantage: Non-optimum chip layout.

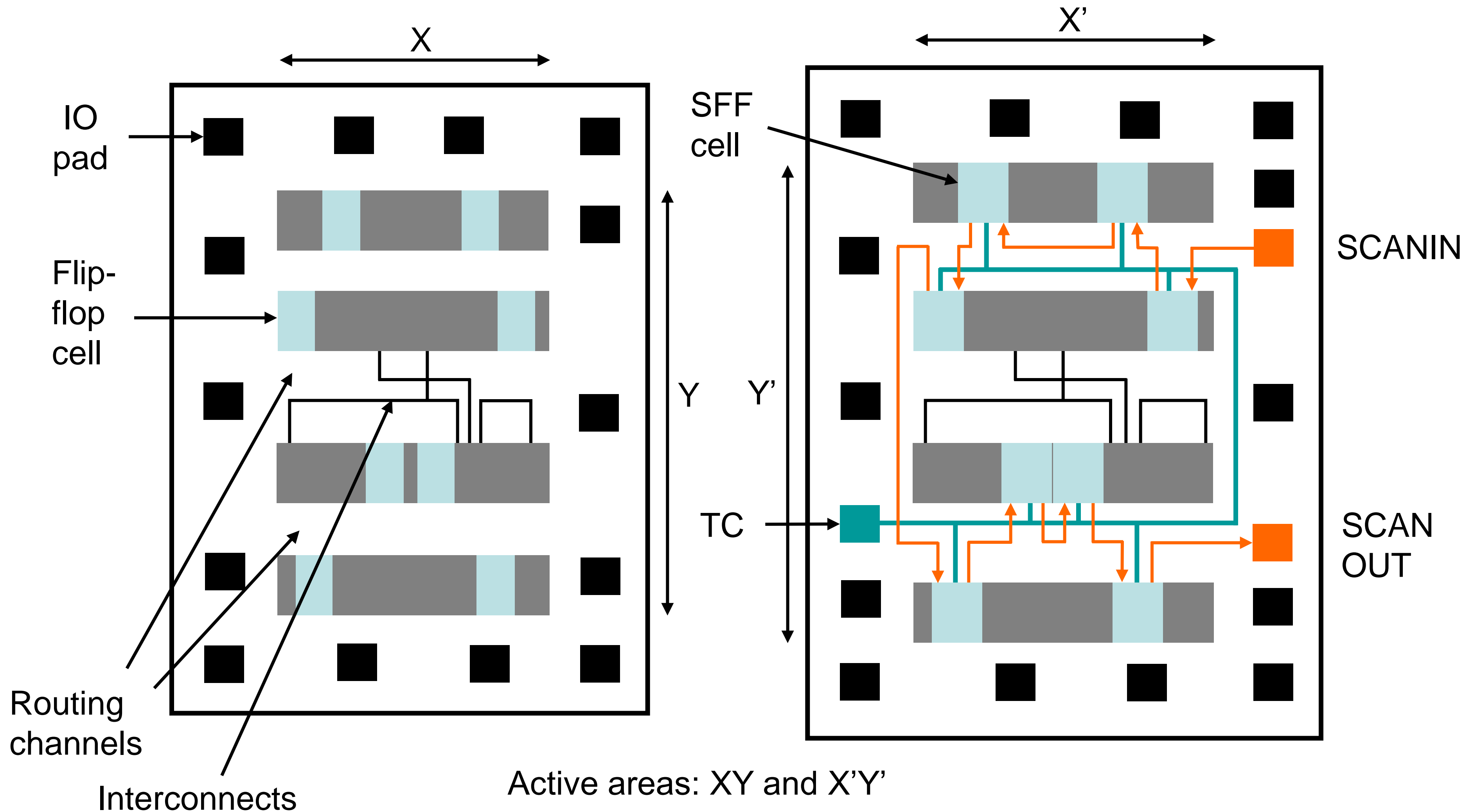


Hierarchical netlist



Flat layout

Optimum Scan Layout



Active areas: XY and X'Y'

ATPG Example: S5378

	Original	Full-scan
Number of combinational gates	2,781	2,781
Number of non-scan flip-flops (10 gates each)	179	0
Number of scan flip-flops (14 gates each)	0	179
Gate overhead	0.0%	15.66%
Number of faults	4,603	4,603
PI/PO for ATPG	35/49	214/228
Fault coverage	70.0%	99.1%
Fault efficiency	**70.9%**	**100.0%**
CPU time on SUN Ultra II, 200MHz processor	5,533 s	5 s
Number of ATPG vectors	414	585
Scan sequence length	414	105,662

Thank You