VLSI testing

Introduction

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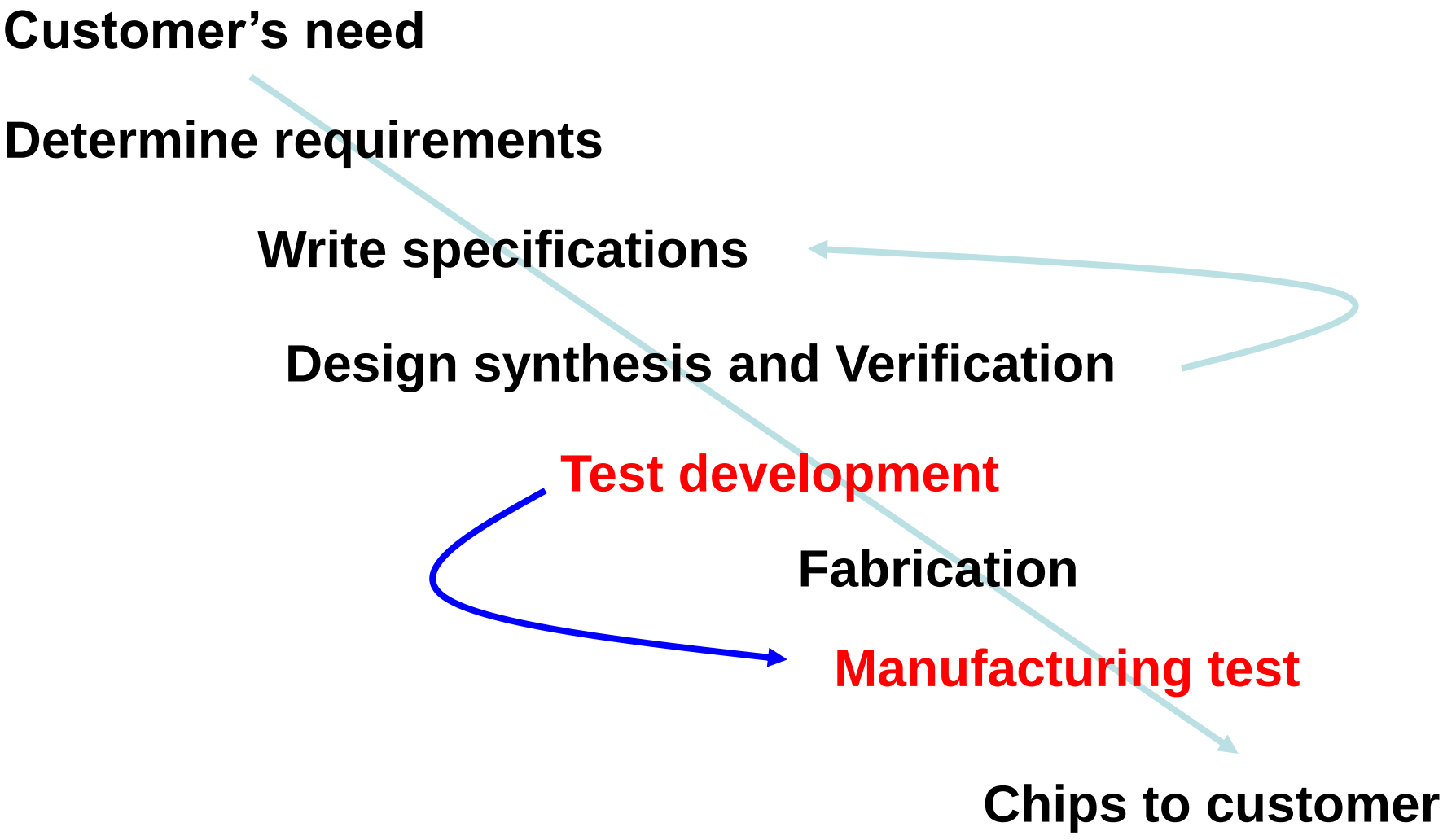
EE 709: Testing & Verification of VLSI Circuits

Lecture – 3 (Jan 05, 2011)

VLSI Realization Process



Verification vs. Test

Verification

- Verifies correctness of design.
- Performed by simulation, hardware emulation, or formal methods.
- Performed once prior to manufacturing.
- Responsible for quality of design.

Test

- Verifies correctness of manufactured hardware.
- Two-part process:
  1. Test generation: software process executed once during design
  2. Test application: electrical tests applied to hardware
- Test application performed on every manufactured device.
- Responsible for quality of devices.

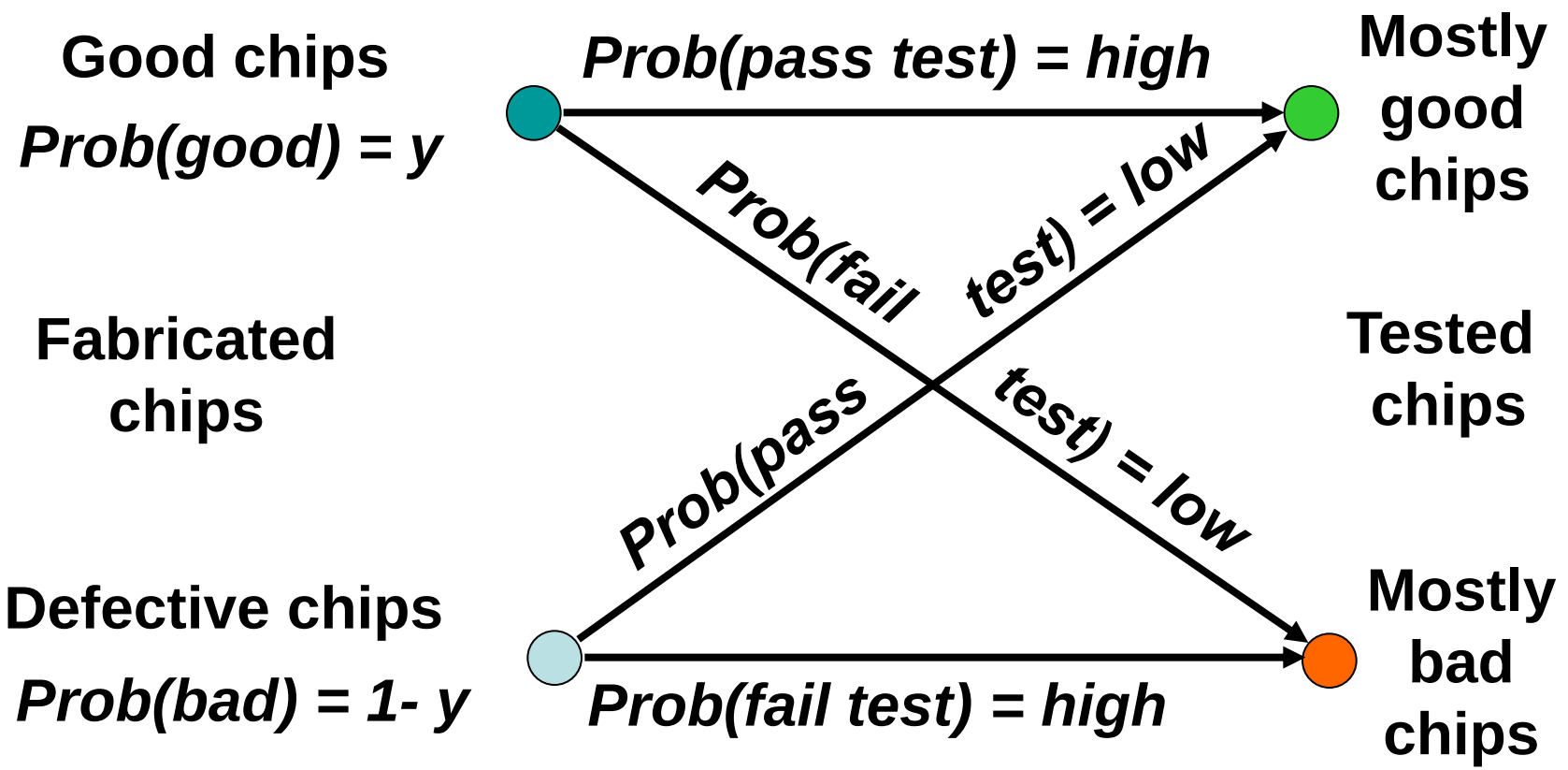
Problems of Ideal Tests

- Ideal tests detect all defects produced in the manufacturing process.
- Ideal tests pass all functionally good devices.
- Very large numbers and varieties of possible defects need to be tested.
- Difficult to generate tests for some real defects. *Defect-oriented testing is an open problem.*

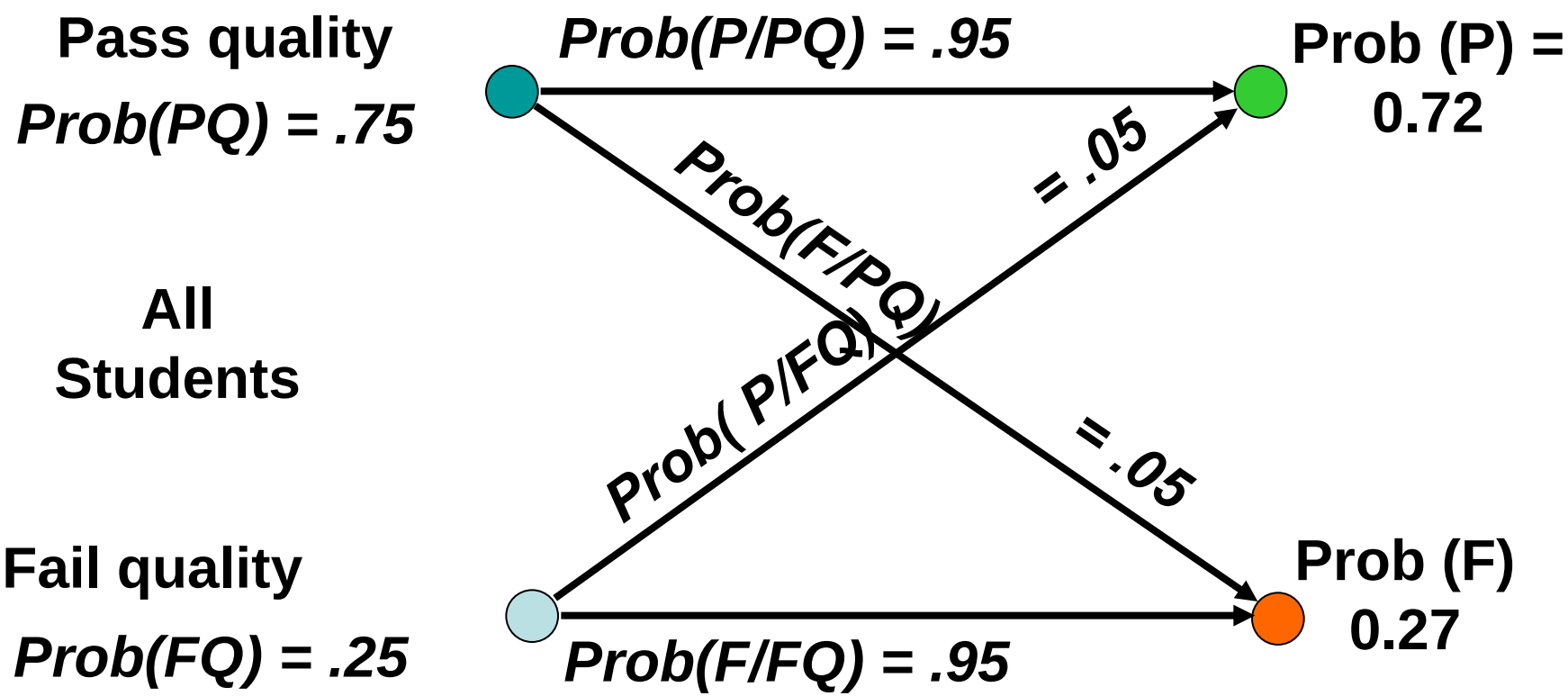
Real Tests

- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected. The fraction (or percentage) of such chips is called the *yield loss.*
- Some bad chips pass tests. The fraction (or percentage) of bad chips among all passing chips is called the *defect level.*

Testing as Filter Process



Students Examination



Roles of Testing

- Detection: Determination whether or not the *device under test* (DUT) has some fault.
- Diagnosis: Identification of a specific fault that is present on DUT.
- Device characterization: Determination and correction of errors in design and/or test procedure.
- *Failure mode analysis* (FMA): Determination of manufacturing process errors that may have caused defects on the DUT.

Costs of Testing

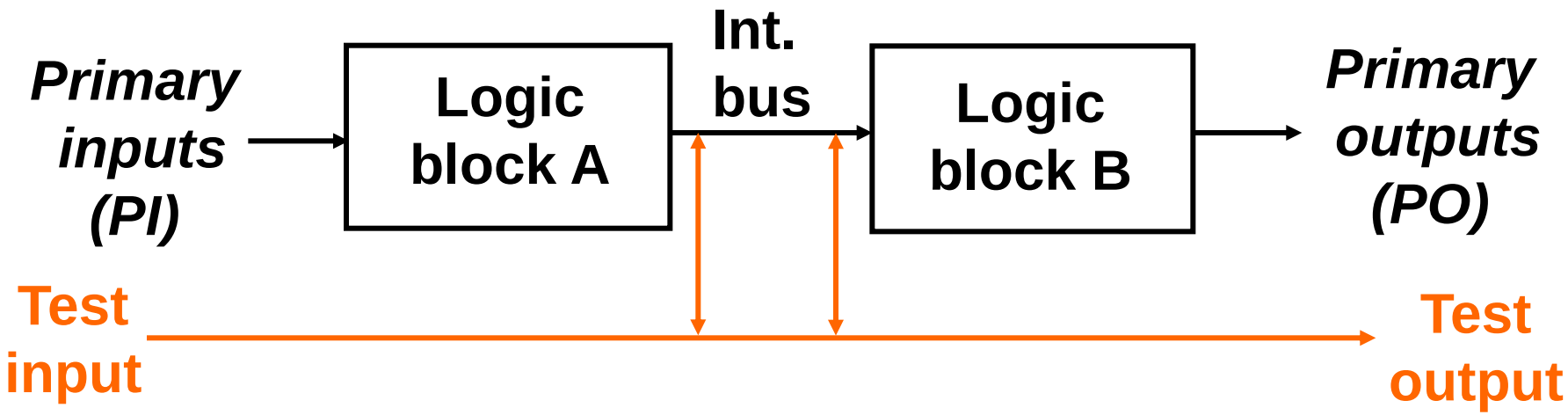
- *Design for testability* (DFT)
  - Chip area overhead and yield reduction
  - Performance overhead
- Software processes of test
  - Test generation and fault simulation
  - Test programming and debugging
- Manufacturing test
  - *Automatic test equipment* (ATE) capital cost
  - Test center operational cost

Design for Testability (DFT)

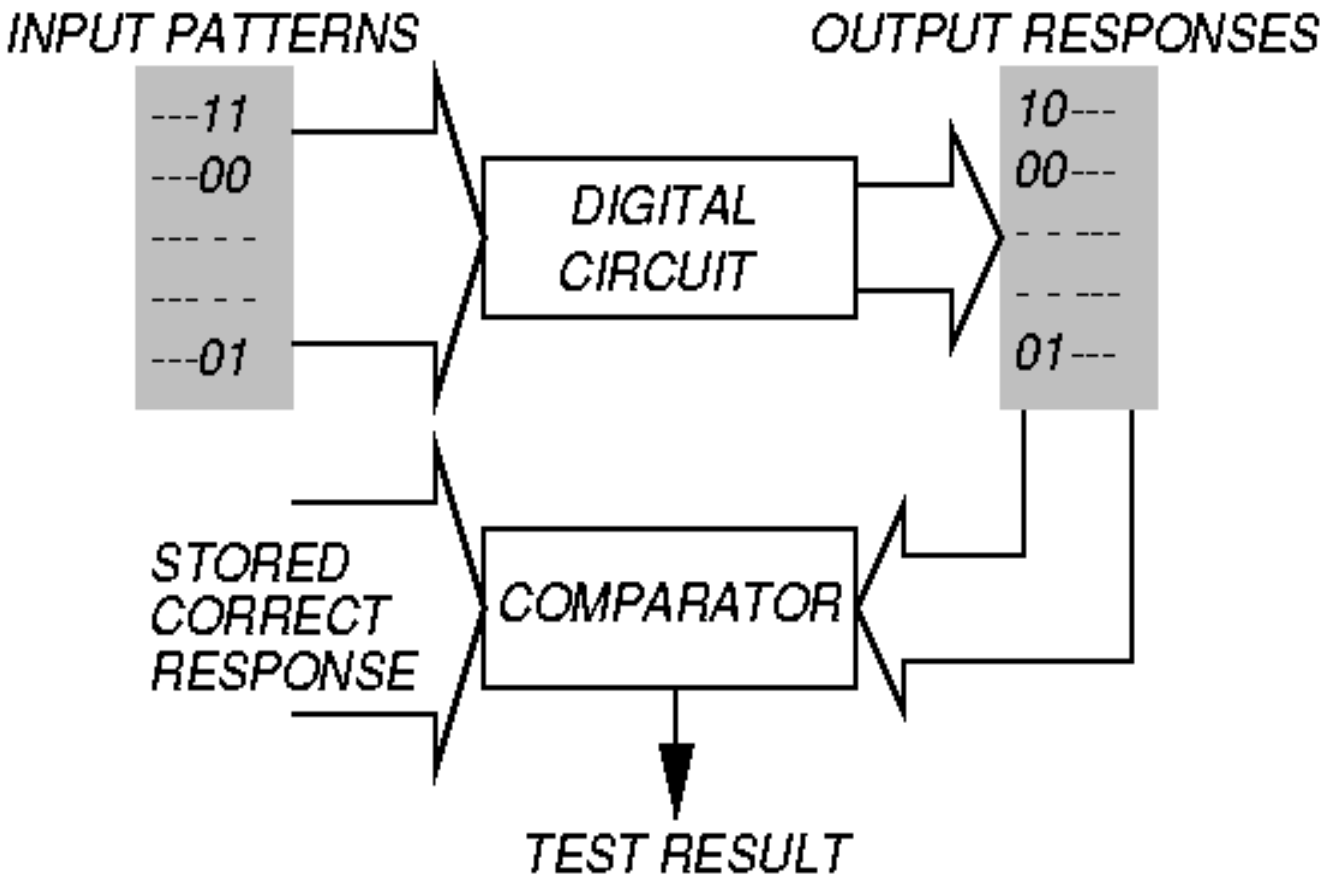
DFT refers to hardware design styles or added hardware that reduces test generation complexity.

Motivation: Test generation complexity increases exponentially with the size of the circuit.

Example: Test hardware applies tests to blocks A and B and to internal bus; avoids test generation for combined A and B blocks.



Testing Principle

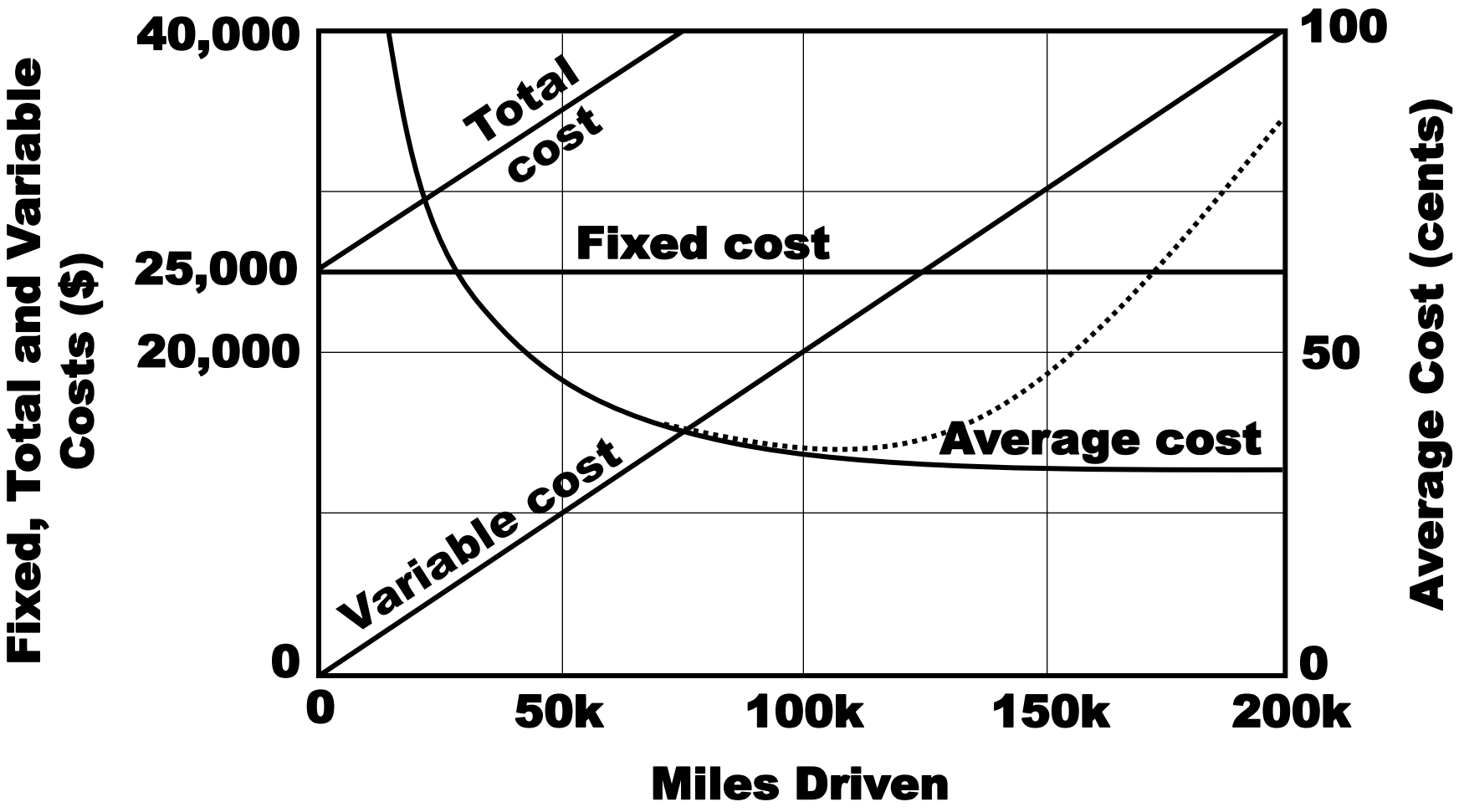


ADVANTEST Model T6682 ATE

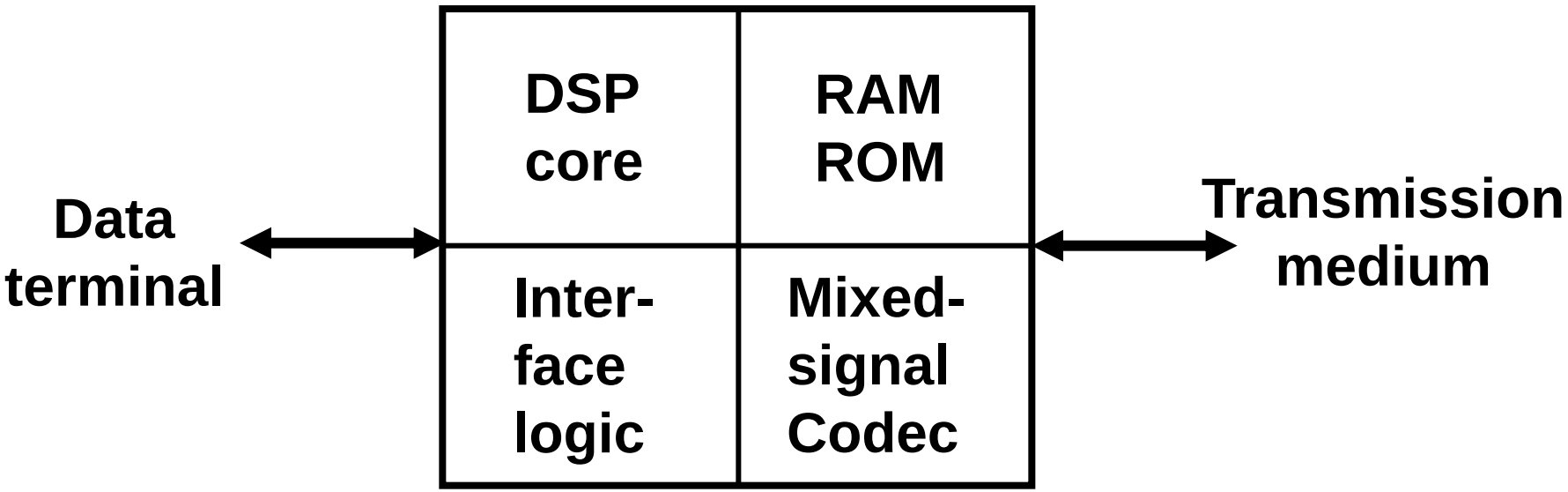
Cost of Manufacturing Testing

- 0.5-1.0GHz; analog instruments; 1,024 digital pins: ATE purchase price
  - = $1.2M + 1,024 x $3,000 = $4.272M
- Running cost (five-year linear depreciation)
  - = Depreciation + Maintenance + Operation
  - = $0.854M + $0.085M + $0.5M
  - = $1.439M/year
- Test cost (24 hour ATE operation)
  - = $1.439M/(365 x 24 x 3,600)
  - = 4.5 cents/second

Cost Analysis Graph



A Modern VLSI Device System-on-a-chip (SOC)



VLSI Chip Yield

- A manufacturing defect is a finite chip area with electrically malfunctioning circuitry caused by errors in the fabrication process.
- A chip with no manufacturing defect is called a good chip.
- Fraction (or percentage) of good chips produced in a manufacturing process is called the *yield*. Yield is denoted by symbol *Y*.
- Cost of a chip:

$$\frac{\text{Cost of fabricating and testing a wafer}}{\text{Yield x Number of chip sites on the wafer}}$$

Thank You