Random Access Scan

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EE 709: Testing & Verification of VLSI Circuits

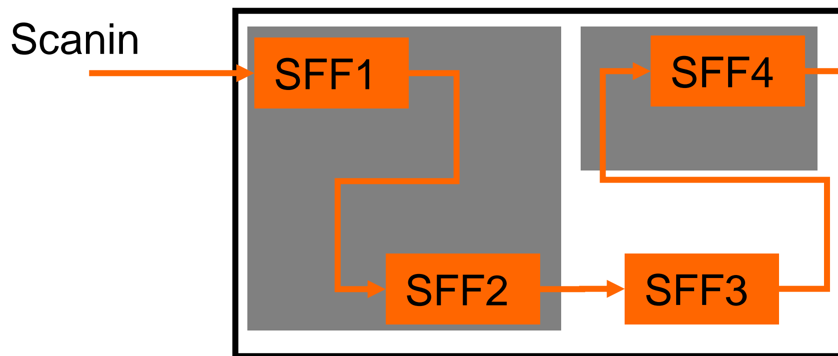
Lecture – 22 (Feb 16, 2012)

Scan Overheads

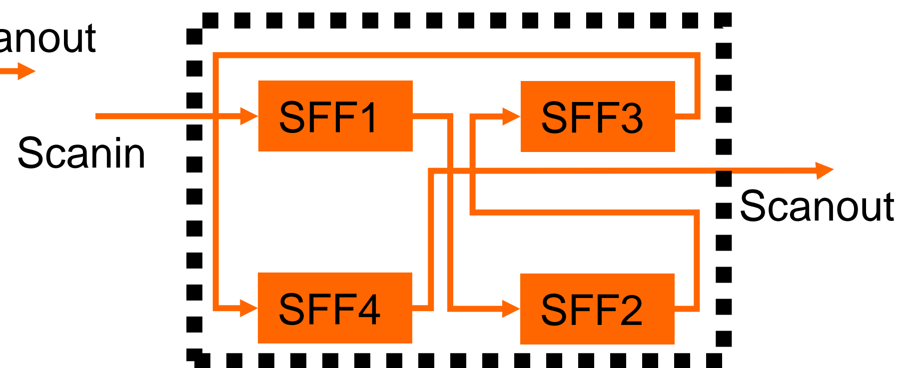
- IO pins: One pin necessary.
- Area overhead:
  - *Gate overhead* = $[4\, n_{sff}/(n_g+10n_{ff})] \times 100\%$, where n_g = *comb. gates*; n_{ff} = *flip-flops*; Example – n_g = 100k gates, n_{ff} = 2k *flip-flops*, overhead = 6.7%.
  - More accurate estimate must consider scan wiring and layout area.
- Performance overhead:
  - Multiplexer delay added in combinational path; approx. two gate-delays.
  - Flip-flop output loading due to one additional fanout; approx. 5-6%.

Hierarchical Scan

- Scan flip-flops are chained within subnetworks before chaining subnetworks.
- Advantages:
  - Automatic scan insertion in netlist
  - Circuit hierarchy preserved – helps in debugging and design changes
- Disadvantage: Non-optimum chip layout.

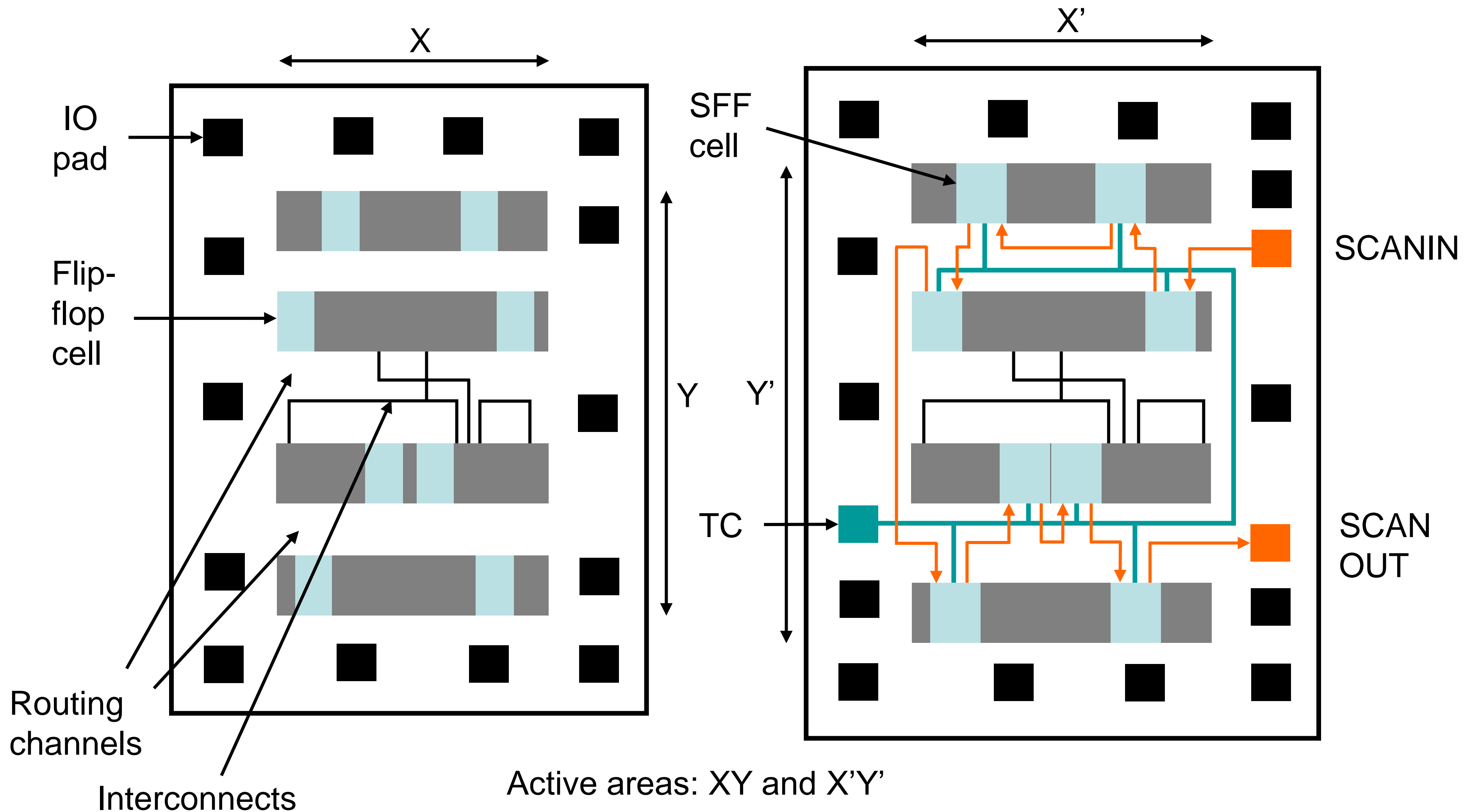


Hierarchical netlist



Flat layout

Optimum Scan Layout



ATPG Example: S5378

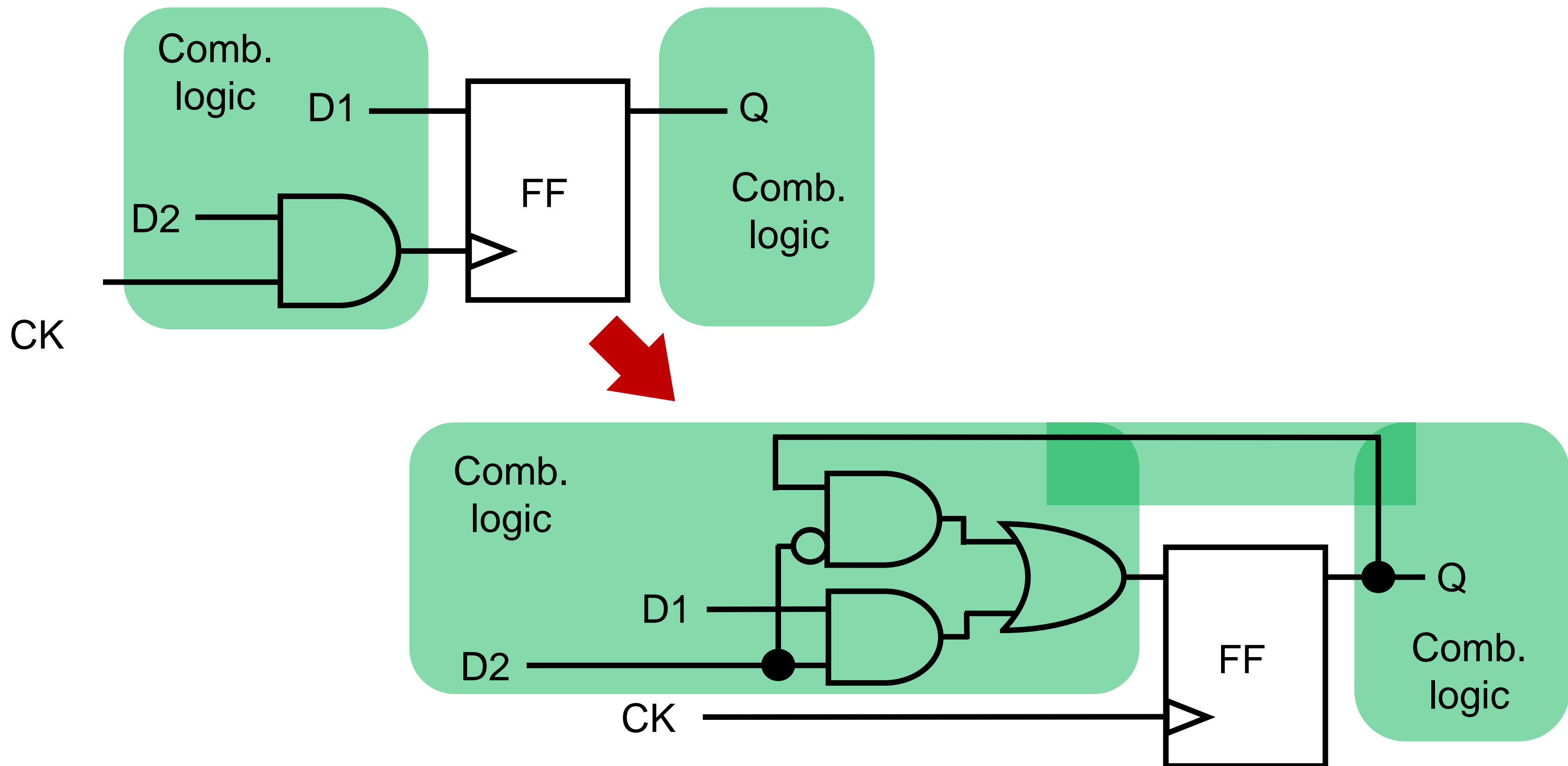
	Original	Full-scan
Number of combinational gates	2,781	2,781
Number of non-scan flip-flops (10 gates each)	179	0
Number of scan flip-flops (14 gates each)	0	179
Gate overhead	0.0%	15.66%
Number of faults	4,603	4,603
PI/PO for ATPG	35/49	214/228
Fault coverage	70.0%	99.1%
Fault efficiency	**70.9%**	**100.0%**
CPU time on SUN Ultra II, 200MHz processor	5,533 s	5 s
Number of ATPG vectors	414	585
Scan sequence length	414	105,662

Scan Design Rules

- Use only clocked D-type of flip-flops for all state variables.
- At least one PI pin must be available for test; more pins, if available, can be used.
- All clocks must be controlled from PIs.
- Clocks must not feed data inputs of flip-flops.

Correcting a Rule Violation

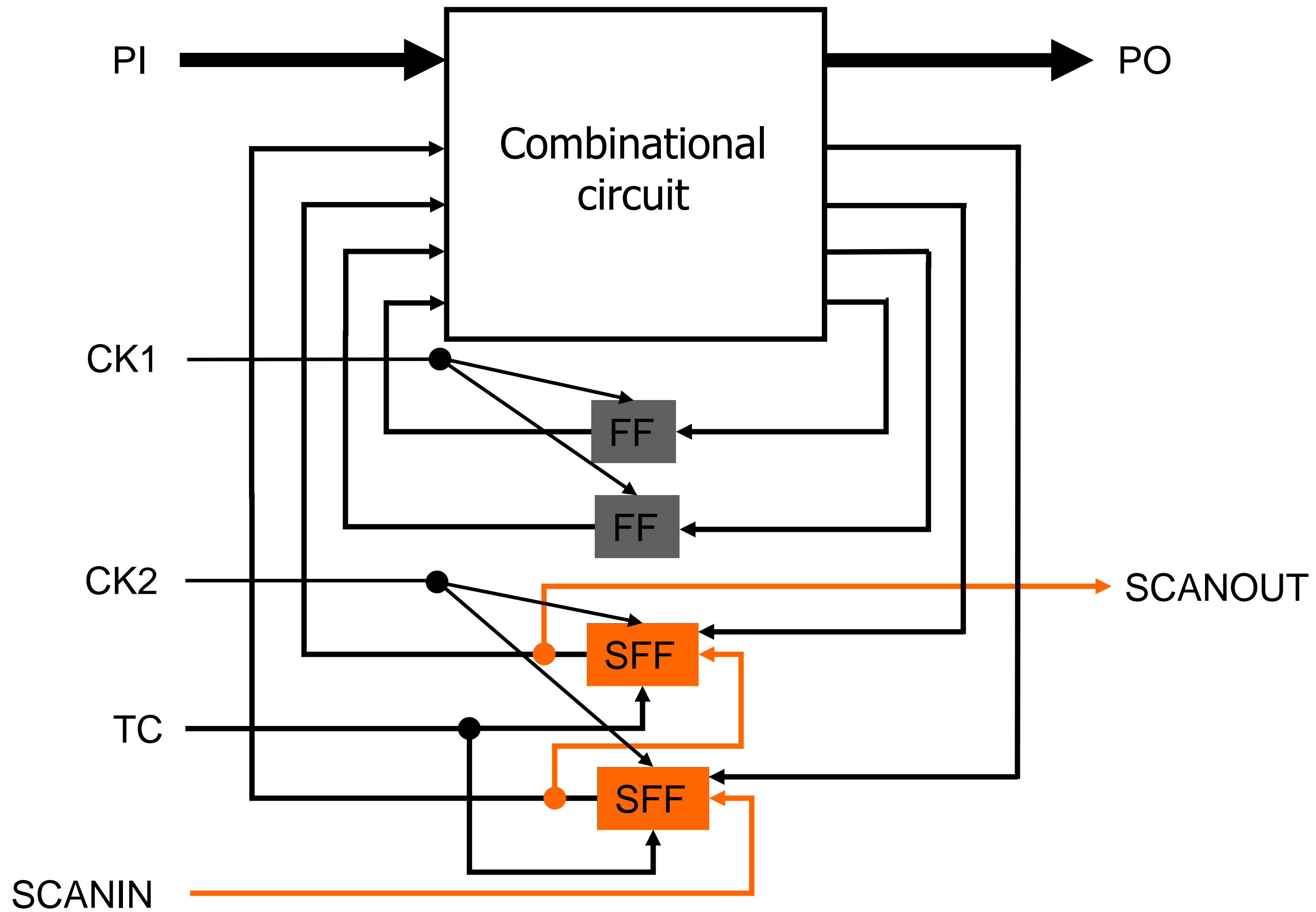
- All clocks must be controlled from PIs.



Partial-Scan Definition

- A subset of flip-flops is scanned.
- Objectives:
  - Minimize area overhead and scan sequence length, yet achieve required fault coverage
  - Exclude selected flip-flops from scan:
    - Improve performance
    - Allow limited scan design rule violations
  - Allow automation:
    - In scan flip-flop selection
    - In test generation
  - Shorter scan sequences

Partial-Scan Architecture



Relevant Results

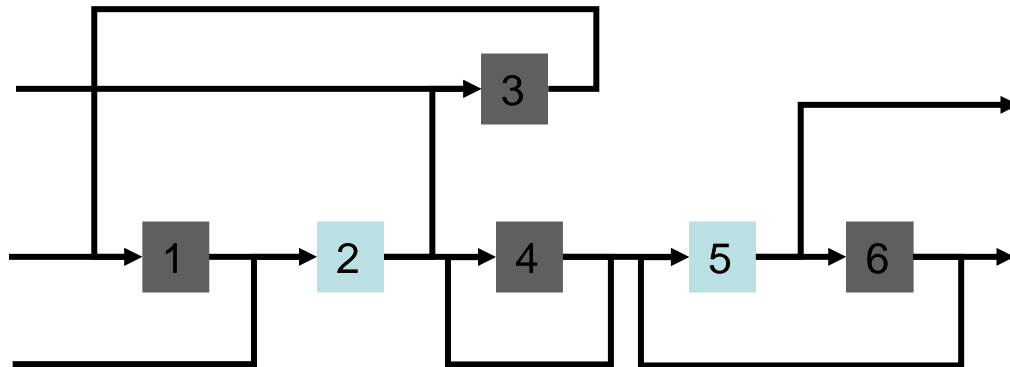
- Theorem1: A cycle-free circuit is always initializable. It is also initializable in the presence of any non-flip-flop fault.
- Theorem 2: Any non-flip-flop fault in a cycle-free circuit can be detected by at most $d_{seq} + 1$ vectors.
- ATPG complexity: To determine that a fault is untestable in a cyclic circuit, an ATPG program using nine-valued logic may have to analyze $9^{N_{ff}}$ time-frames, where N_{ff} is the number of flip-flops in the circuit.

A Partial-Scan Method

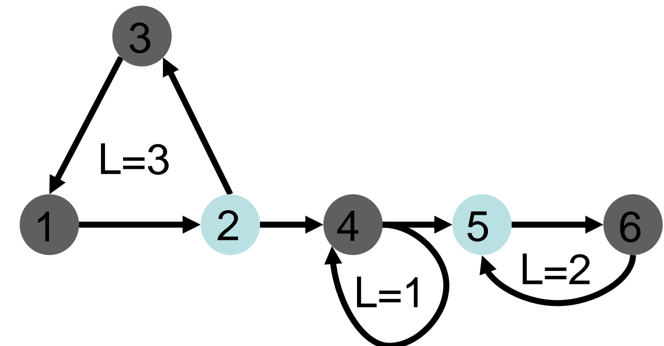
- Select a minimal set of flip-flops for scan to eliminate all cycles.
- Alternatively, to keep the overhead low only long cycles may be eliminated.
- In some circuits with a large number of self-loops, all cycles other than self-loops may be eliminated.

The MFVS Problem

- For a directed graph find a set of vertices with smallest cardinality such that the deletion of this vertex-set makes the graph acyclic.
- The *minimum feedback vertex set* (MFVS) problem is NP-complete; practical solutions use heuristics.
- A secondary objective of minimizing the depth of acyclic graph is useful.



A 6-flip-flop circuit



s-graph

Should Serial Scan Continue

A solution to test power, test time and test data volume

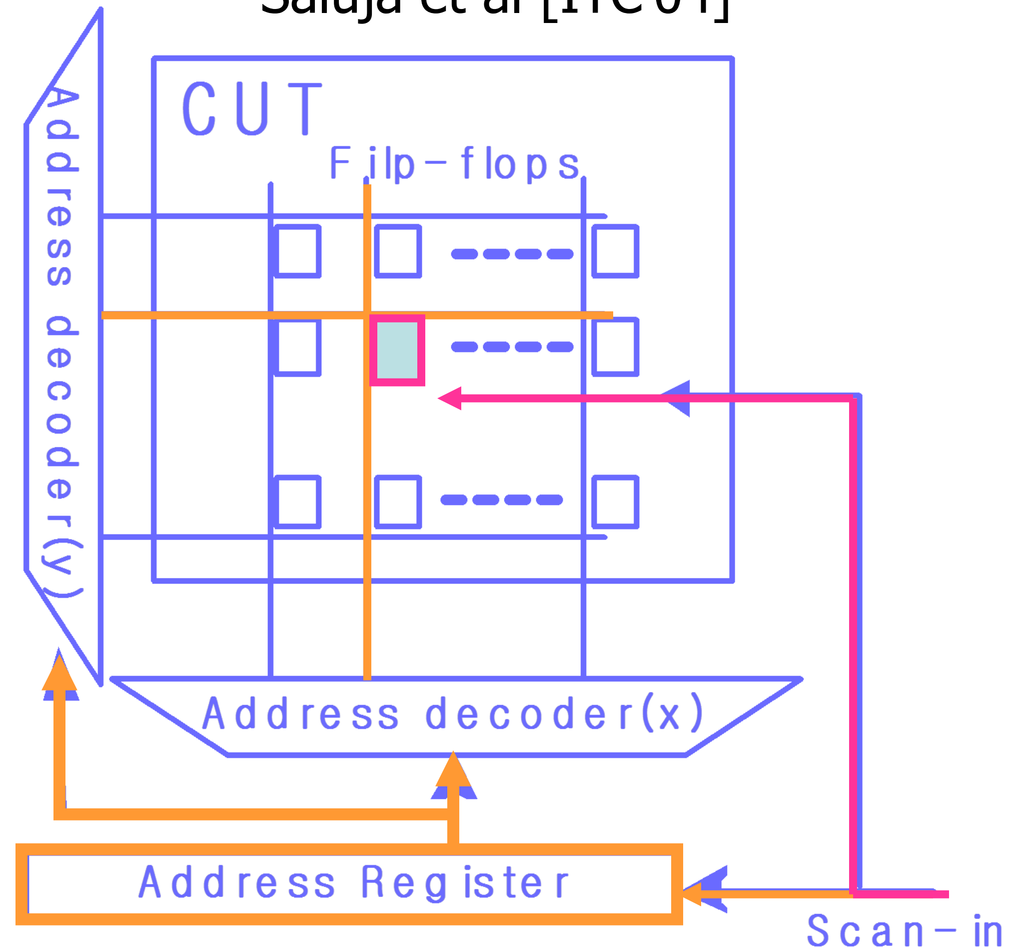
- Three Problems with serial-scan
  - Test power
  - Test application time
  - Test data volume
- Efforts and limitations
  - ATPG for low test power consumption
    - → Test power ↓ Test length ↑
  - Reducing scan clock frequency
    - → Test power ↓ Test application time ↑
  - Scan-chain re-ordering (with additional logic insertion)
    - → Test power/time ↓ Design time ↑
  - Test Compression
    - →Test time/data size ↓ Has limited capability for Compacted test
- Orthogonal attack
  - Random access scan instead of Serial-scan
  - Hardware overhead? Silicon cost << Testing cost

Random Access Scan

A solution to test power, test time and test data volume

Saluja et al [ITC'04]

- Architecture
- Each FF has unique address
- Address shift register
- X-Y Decoder
- Select FF to write/read

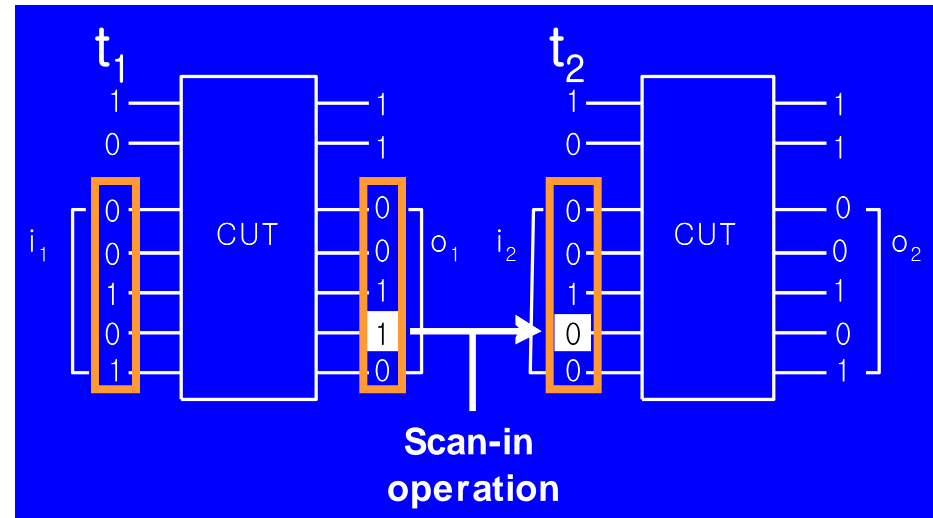


Scan Operation Example

- Test vector

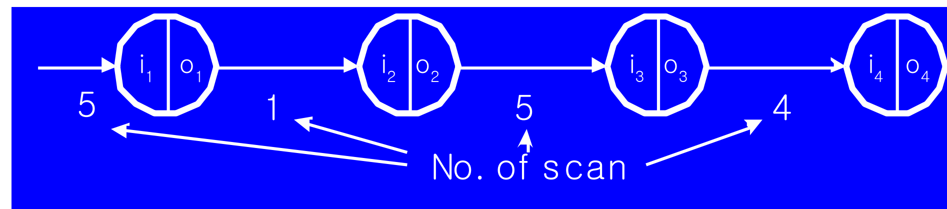
Test	PPI(i_i)	PPO(o_i)
t1	00101	00110
t2	00100	00101
t3	11010	11010
t4	00111	01011

- Scan operation for *t2*



- Complete test application

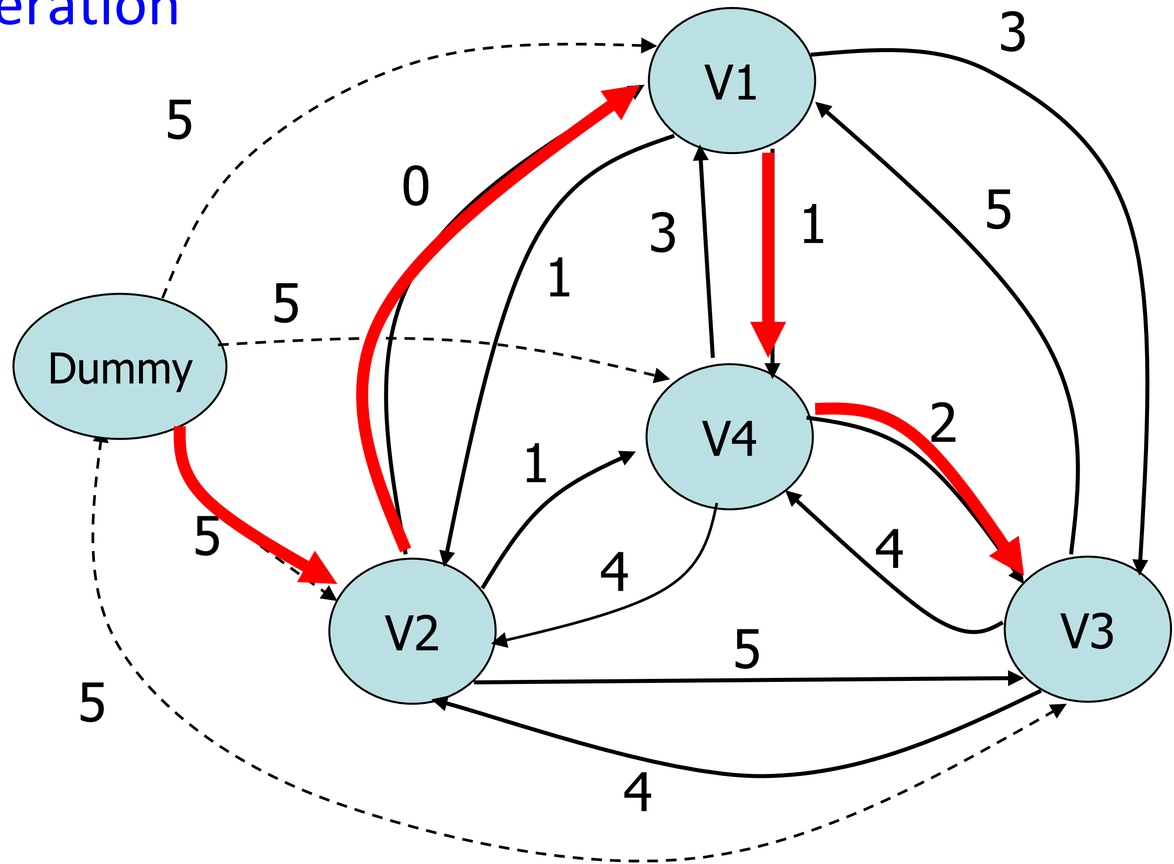
Total number of scan operation = 15



Test Vector Ordering

- Test data volume and Test application time is proportional to the random access scan operation
- Goal: Reduce # scan operation

Test	PPI(i_j)	PPO(o_i)
t1	00101	00110
t2	00100	00101
t3	11010	11010
t4	00111	01011



Scan operation = 8

Hamming Distance Reduction

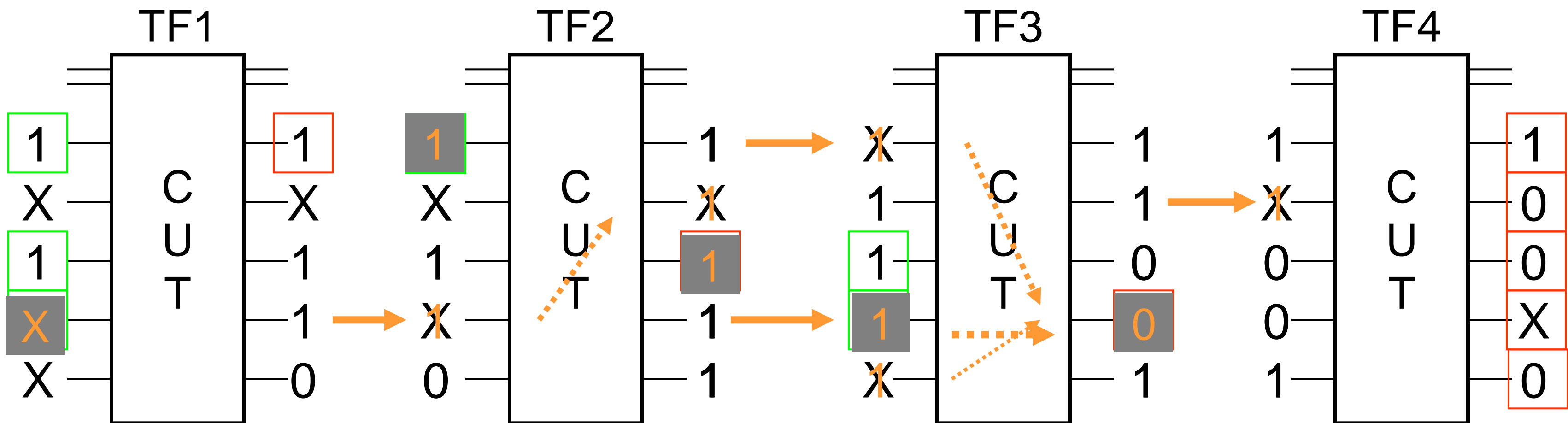
- Don't care values in PPI do not need scan operation
  - Use Don't care identification method

    Fully specified test vector → Vectors w/ X values on targeted bit positions without loss of fault coverage

  1. Before vector ordering: Identify don't cares in PPI
  2. Vector ordering
  3. Simulate test vector in order / Fill X's with previous vectors PPO
  4. Identify more X's on targeted bit in PPI
     - odd vector
     - even vector
  5. Repeat 3,4 until no more X's are identified

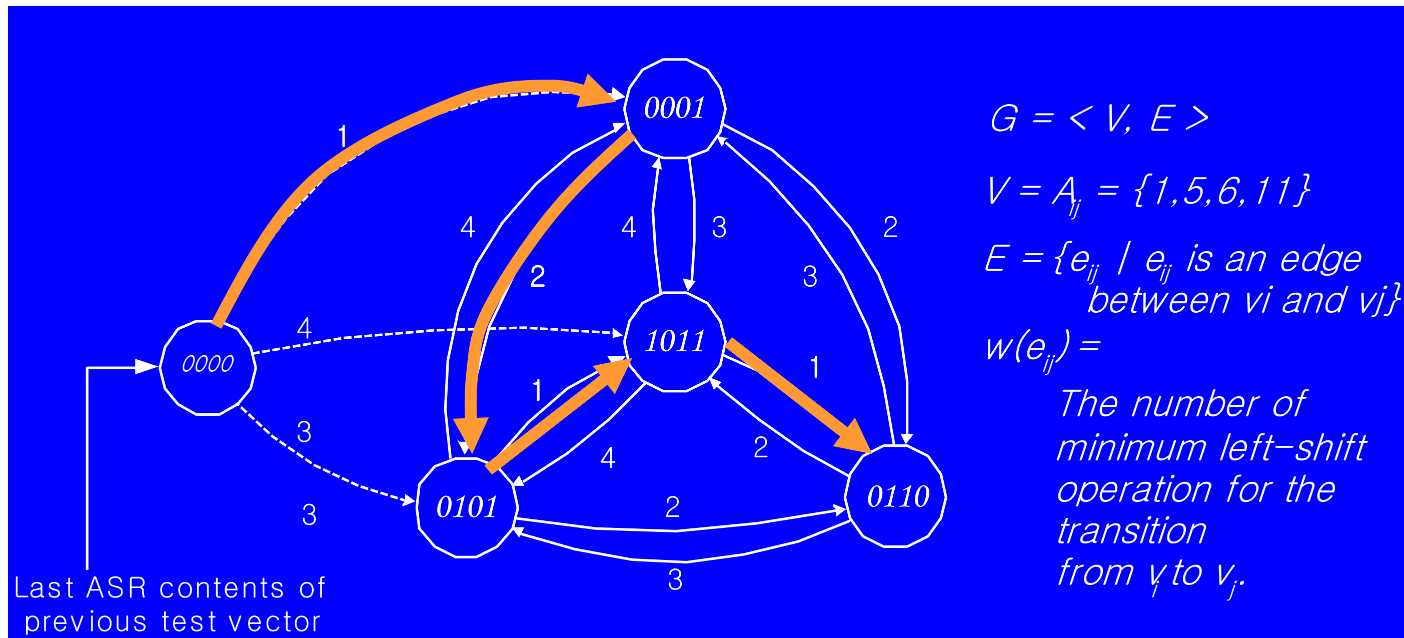
Change allowed

Targeted

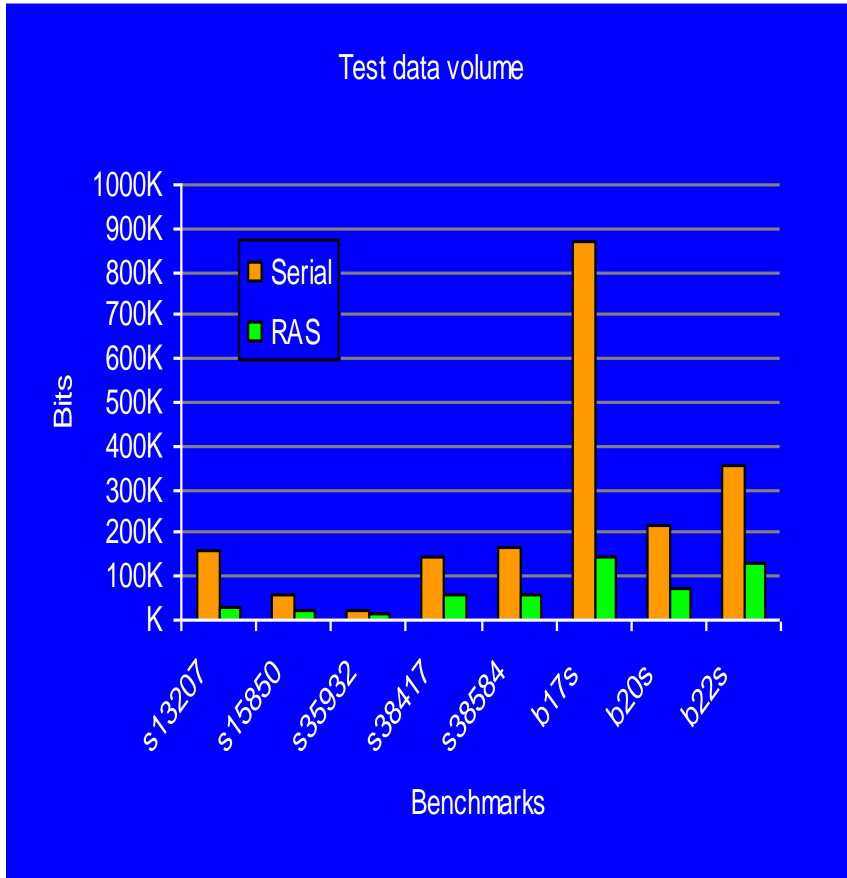


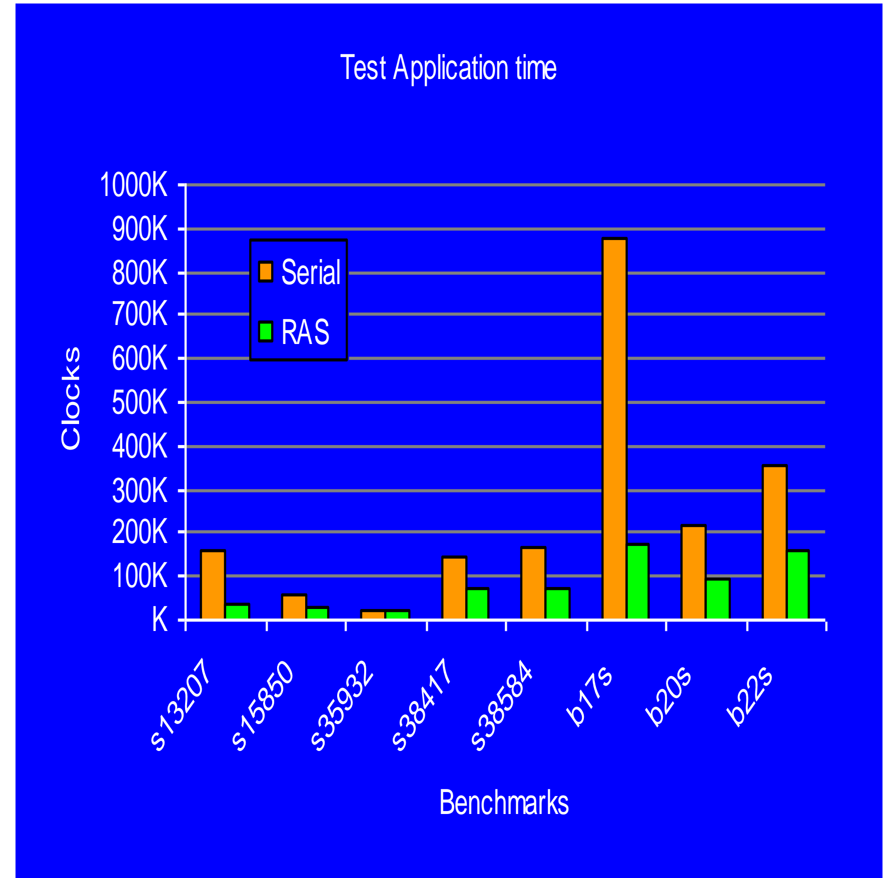
Optimizing Address Scan

- The cost of address shifting
  - # of scan operation x ASR width
  - Example address set = { 1, 5, 6, 11 } for 4-bit ASR
  - 4 X 4 = 16
- Proper ordering of address can minimize shifting cost
  - Apply 11(1011) after 5(0101) → needs only 1 left-shift
- Minimizing address shifting cost
  - Construct Address Shifting Distance Graph (ASD-graph)
  - Find min-cost Hamiltonian path using ATSP algorithm (Result : 5 shifts)



Result (Test Time/Data)





Thank You