Yield and Fault Modeling

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EE 709: Testing & Verification of VLSI Circuits

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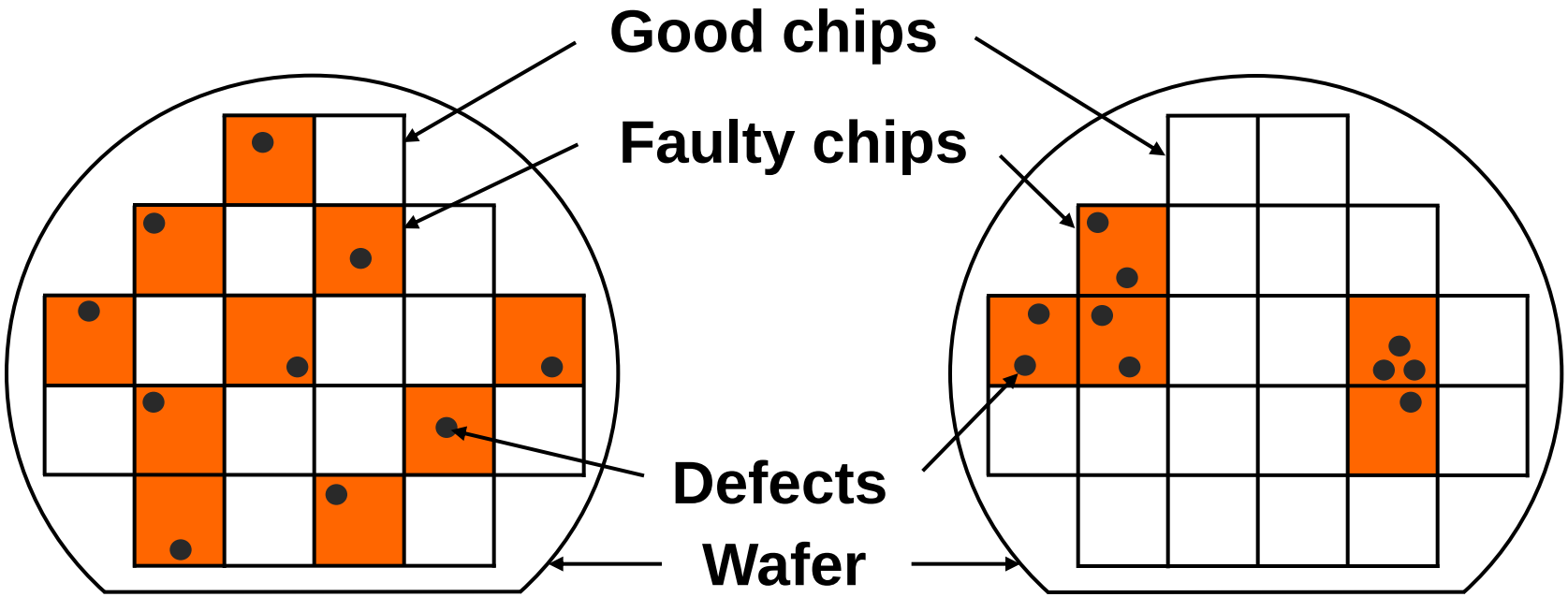
VLSI Chip Yield

- A manufacturing defect is a finite chip area with electrically malfunctioning circuitry caused by errors in the fabrication process.
- A chip with no manufacturing defect is called a good chip.
- Fraction (or percentage) of good chips produced in a manufacturing process is called the *yield*. Yield is denoted by symbol *Y*.
- Cost of a chip:

$$\frac{\textbf{Cost of fabricating and testing a wafer}}{\textbf{Yield x Number of chip sites on the wafer}}$$

Clustered VLSI Defects



Unclustered defects
Wafer yield = 12/22 = 0.55

Clustered defects (VLSI)
Wafer yield = 17/22 = 0.77

Yield Parameters

- **Defect density (*d*) = Average number of defects per unit of chip area**
- **Chip area (*A*)**
- **Clustering parameter (α)**
- **Negative binomial distribution of defects,**
  p (*x*) = Prob (number of defects on a chip = *x*)

$$= \frac{\Gamma(\alpha + x)}{x!\,\Gamma(\alpha)} \cdot \frac{(Ad/\alpha)^{x}}{(1 + Ad/\alpha)^{\alpha + x}}$$

where Γ is the gamma function

α = 0, *p* (*x*) is a delta function (maximum clustering)

α = ∞ , *p* (*x*) is Poisson distribution (no clustering)

Yield Equation

Y = Prob (zero defect on a chip) = p (0)

$$Y = (1 + Ad / \alpha)^{-\alpha}$$

Example: Ad = 1.0, α = 0.5, Y = 0.58

Unclustered defects: α = ∞, $Y = e^{-Ad}$

Example: Ad = 1.0, α = ∞, Y = 0.37

***too pessimistic* !**

Defect Level or Reject Ratio

- *Defect level* (DL) is the ratio of faulty chips among the chips that pass tests.
- DL is measured as *parts per million* (ppm).
- DL is a measure of the effectiveness of tests.
- DL is a quantitative measure of the manufactured product quality. For commercial VLSI chips a DL greater than 500 ppm is considered unacceptable.

Determination of DL

- From field return data: Chips failing in the field are returned to the manufacturer. The number of returned chips normalized to one million chips shipped is the DL.

- From test data: Fault coverage of tests and chip fallout rate are analyzed. A modified yield model is fitted to the fallout data to estimate the DL.

Modified Yield Equation

- **Three parameters:**
  - **Fault density, *f* = average number of stuck-at faults per unit chip area**
  - **Fault clustering parameter, β**
  - **Stuck-at fault coverage, *T***
- **The modified yield equation:**

$$Y(T) = (1 + TAf/\beta)^{-\beta}$$

Assuming that tests with 100% fault coverage (*T* =1.0) remove all faulty chips,

$$Y = Y(1) = (1 + Af/\beta)^{-\beta}$$

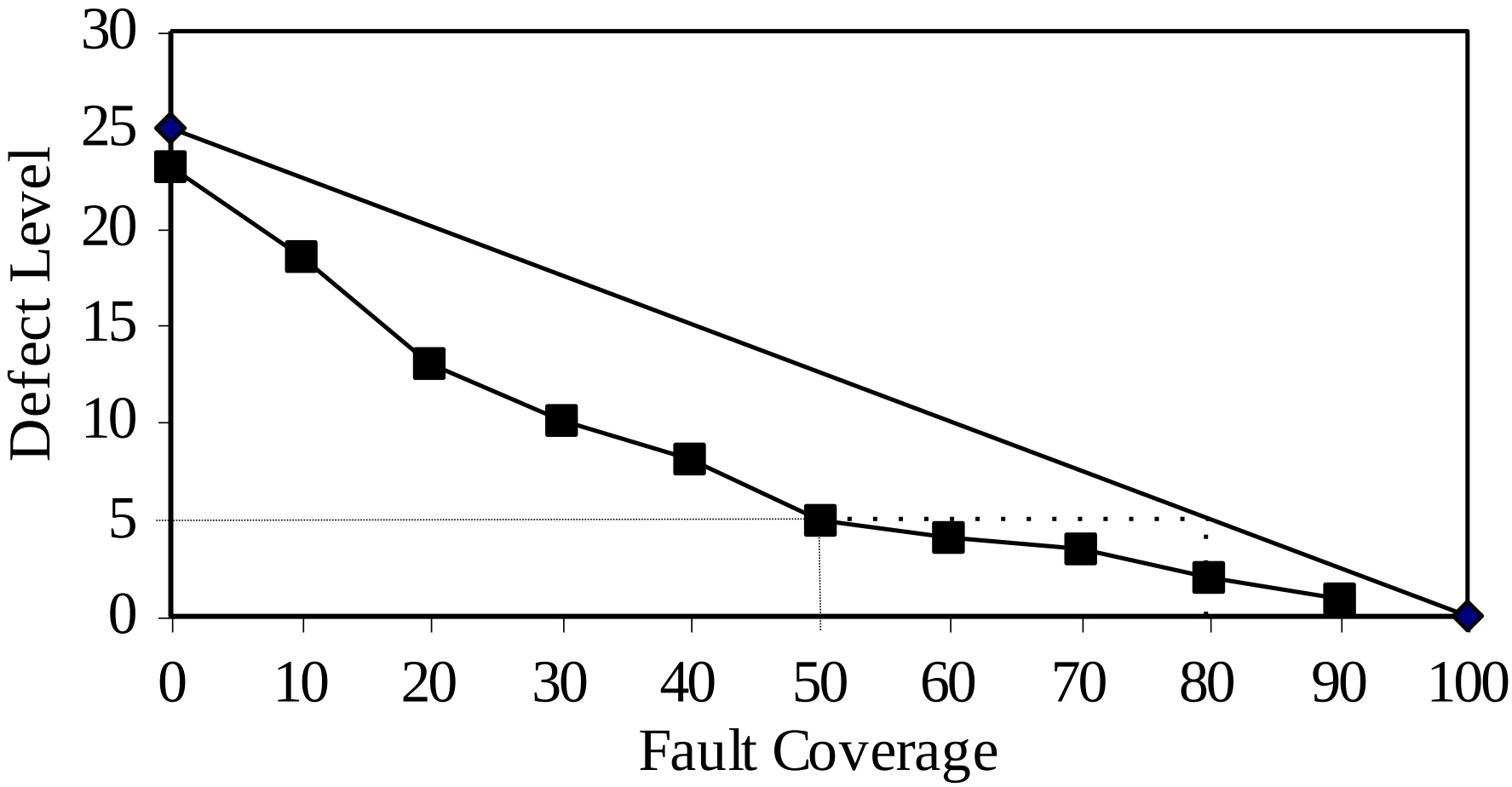
Defect Level

$$DL(T) = \frac{Y(T) - Y(1)}{Y(T)}$$

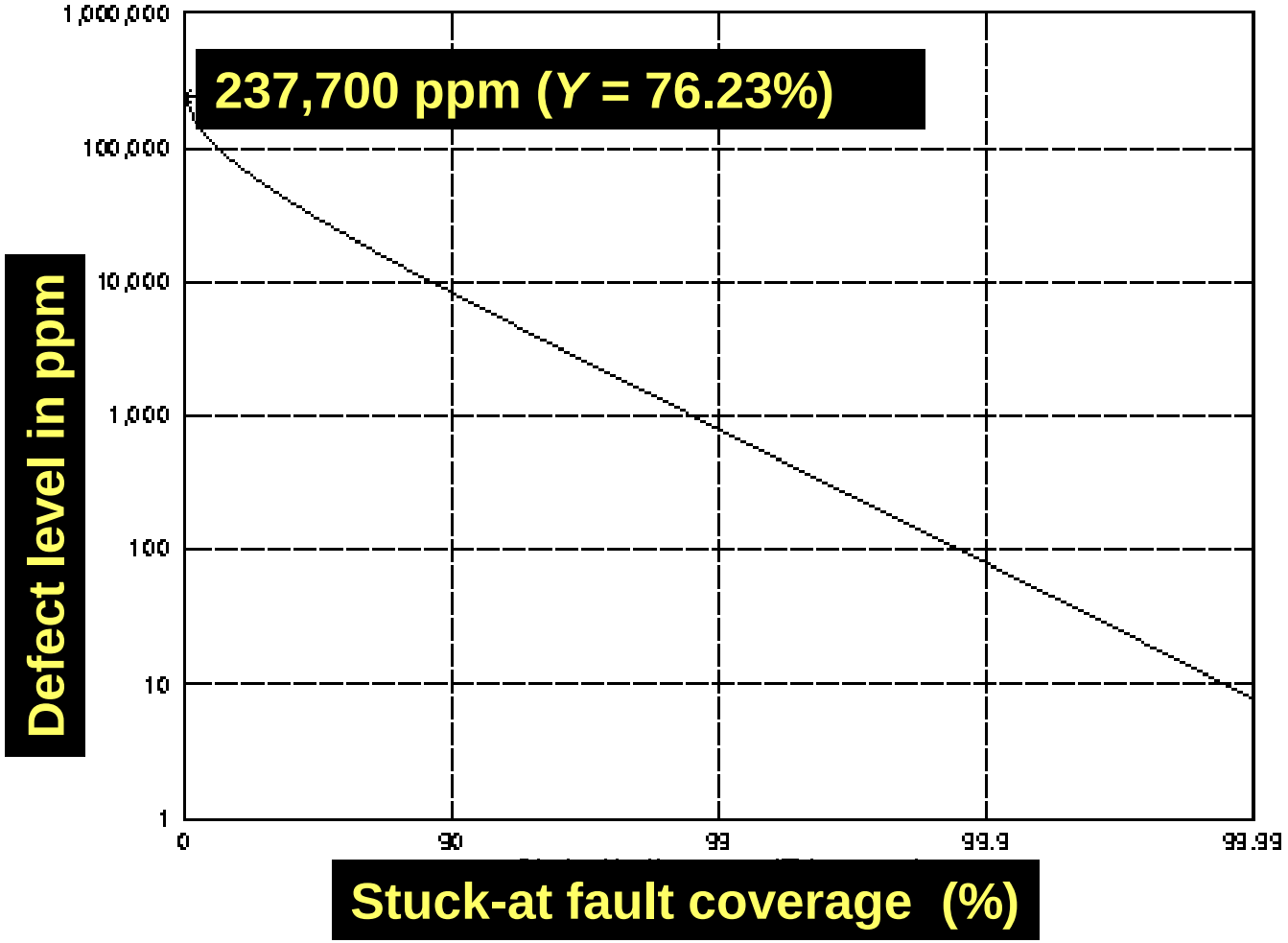
$$= 1 - \frac{(\beta + TAf)^{\beta}}{(\beta + Af)^{\beta}}$$

Where T is the fault coverage of tests, Af is the average number of faults on the chip of area A, β is the fault clustering parameter. Af and β are determined by test data analysis.

Yield and Fault Coverage

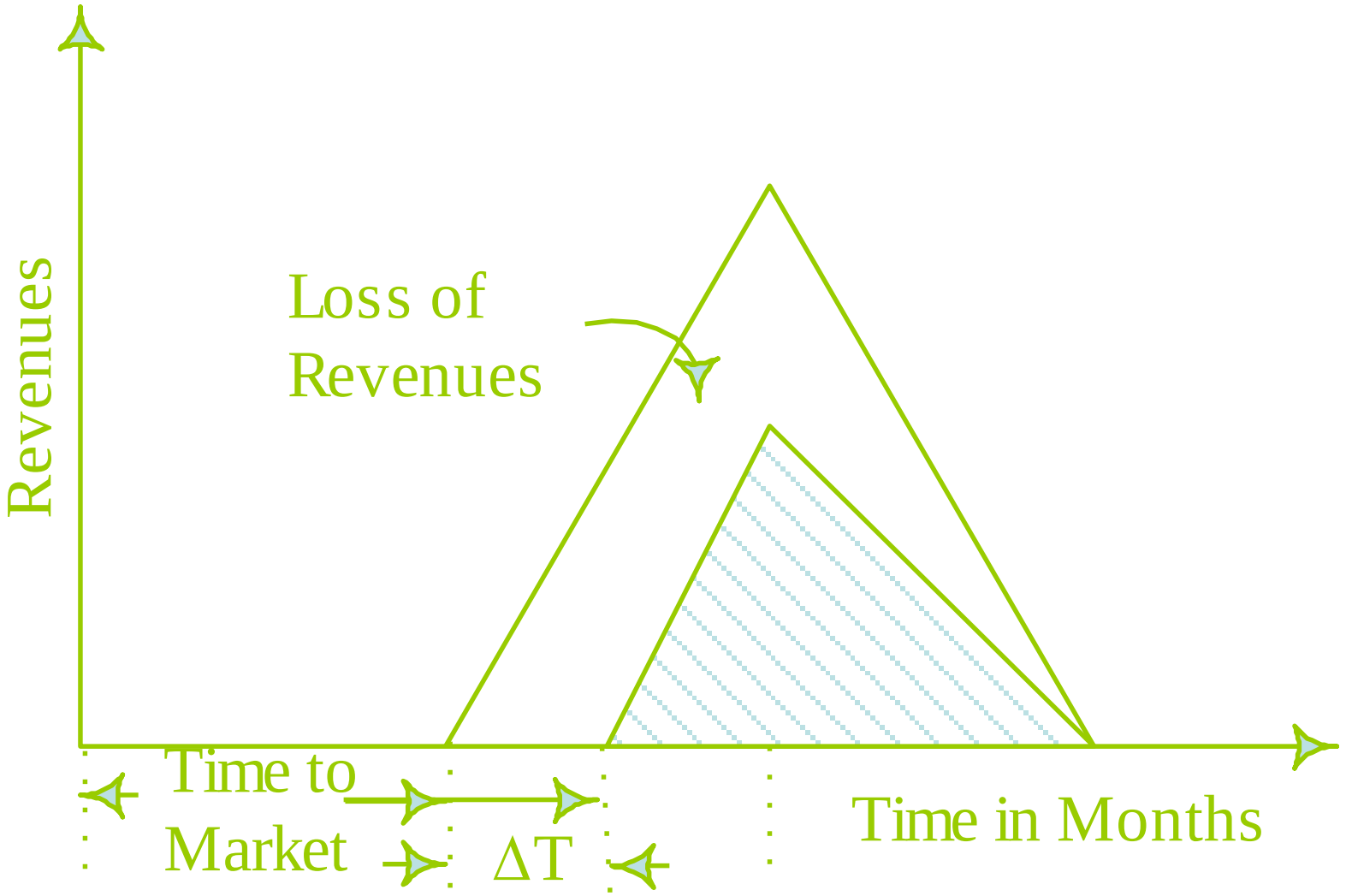


Computed DL

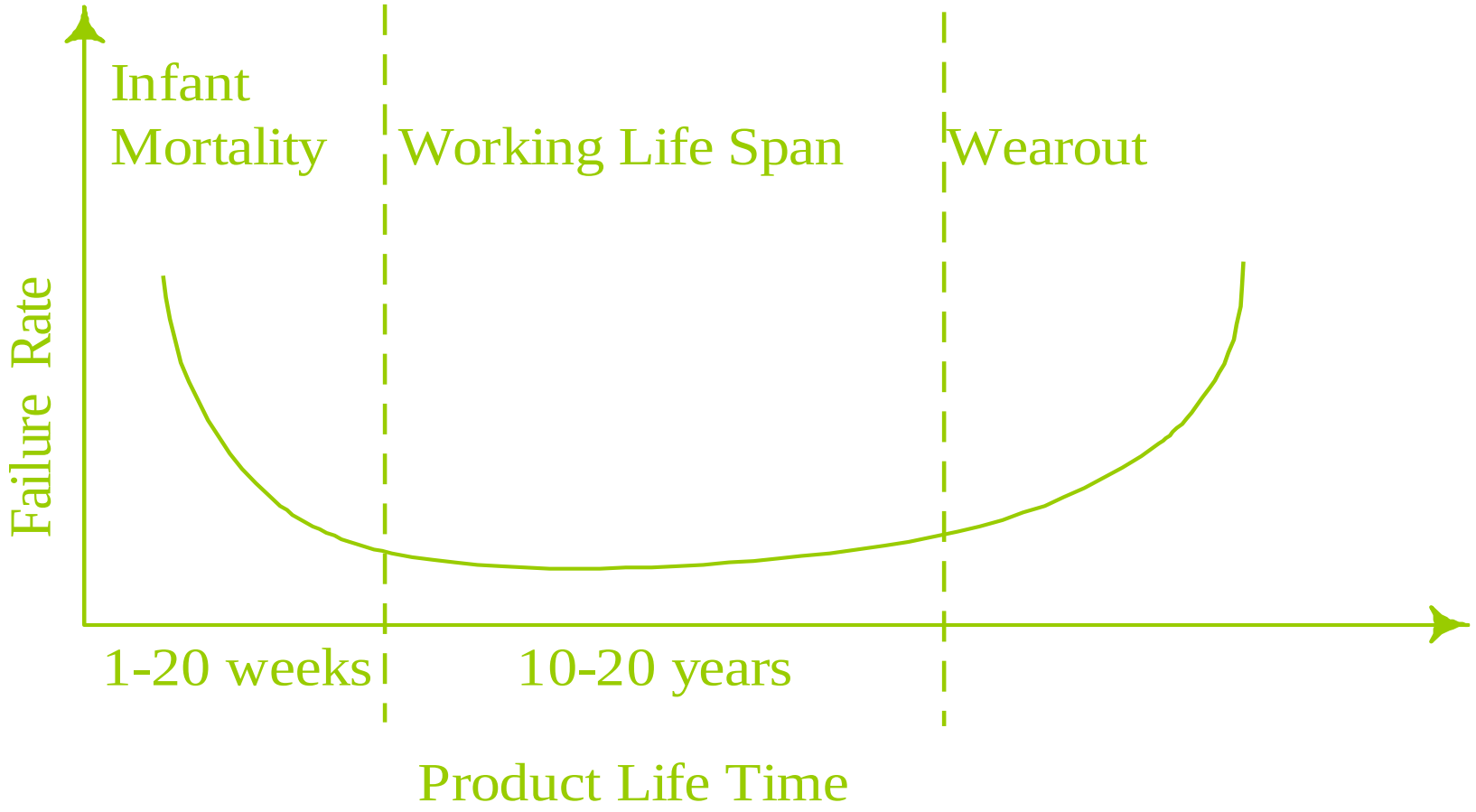


SEMATECH Chip (Courtesy: IBM)

Time to Market



Failure Rate Vs Product Lifetime

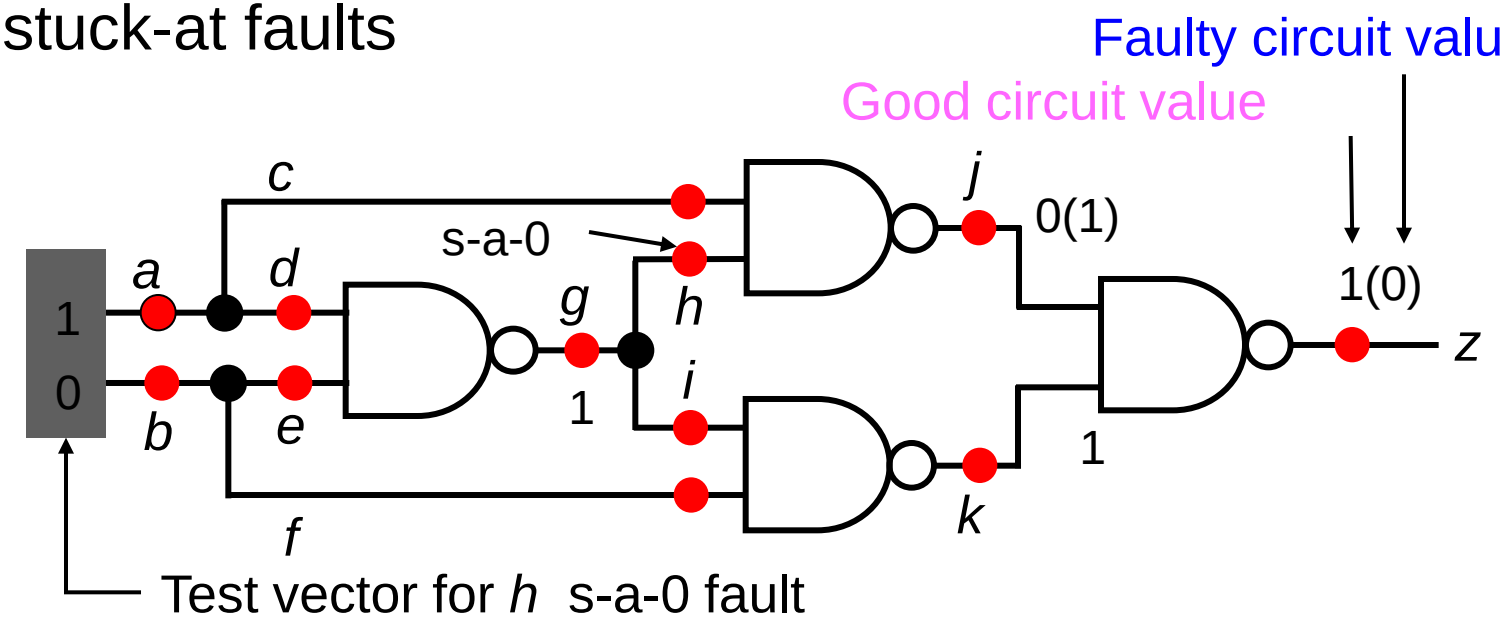


Common Fault Models

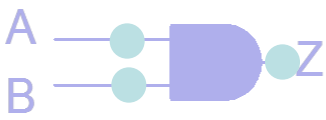
- **Single stuck-at faults**
- **Transistor open and short faults**
- **Memory faults**
- **PLA faults (stuck-at, cross-point, bridging)**
- **Functional faults (processors)**
- **Delay faults (transition, path)**
- **Analog faults**

Single Stuck-at Fault

- Three properties define a single stuck-at fault
  - Only one line is faulty
  - The faulty line is permanently set to 0 or 1
  - The fault can be at an input or output of a gate
- Example: XOR circuit has 12 fault sites (●) and 24 single stuck-at faults

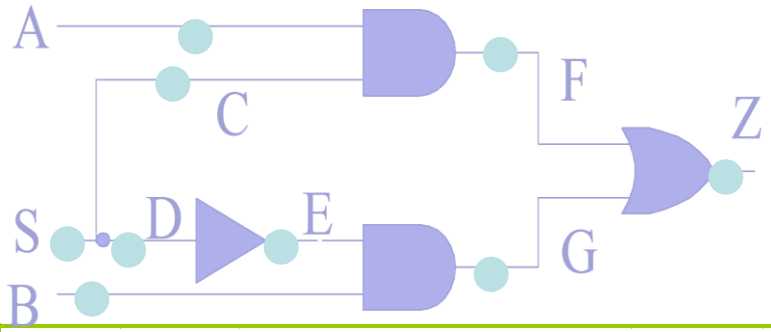


SA Faults



Inputs AB	FF Response	Faulty Response A/0	B/0	Z/0	A/1	B/1	Z/1
00	0	0	0	0	0	0	1
01	0	0	0	0	1	0	1
10	0	0	0	0	0	1	1
11	1	0	0	0	1	1	1

SA Faults

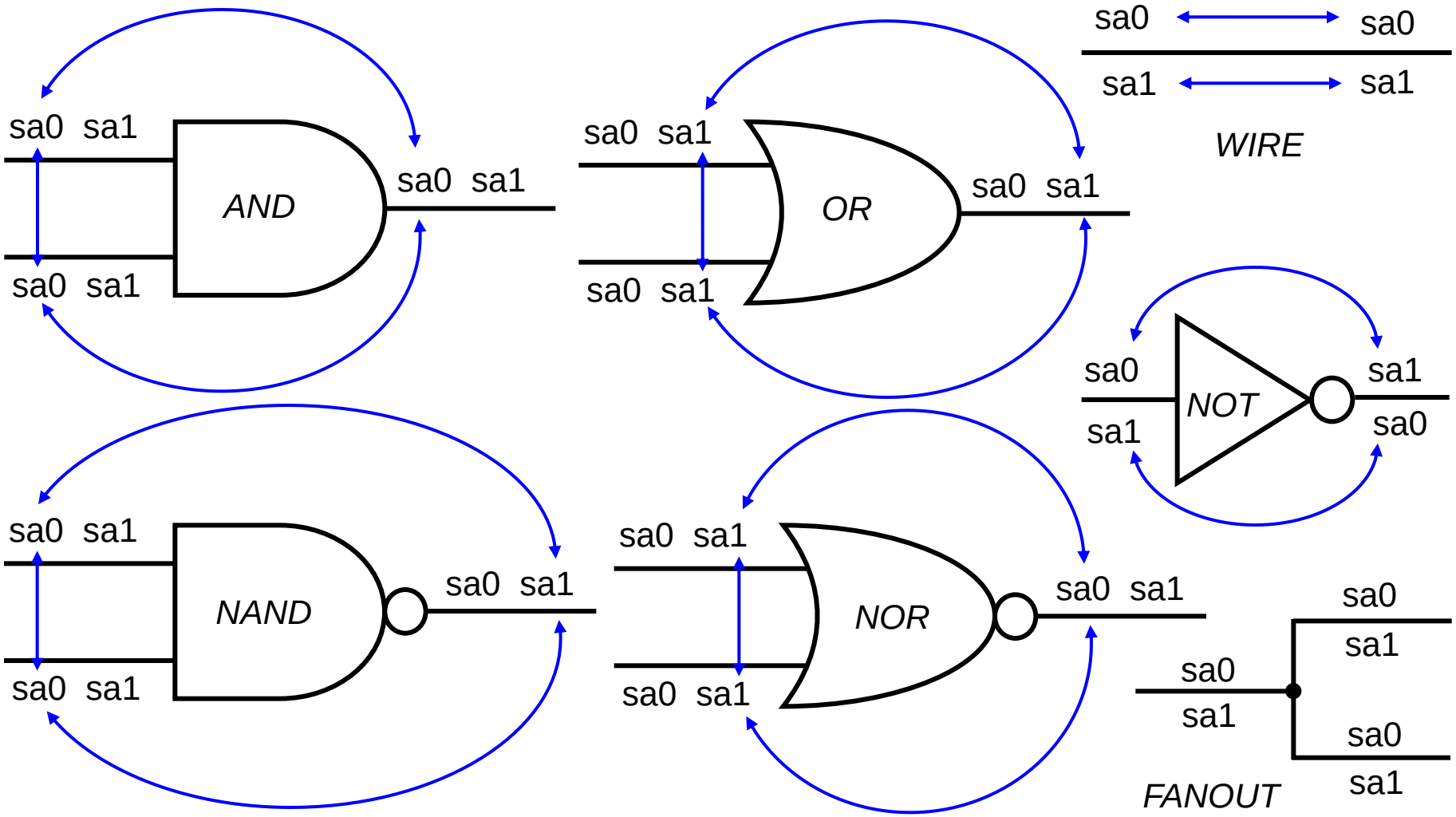


Inp	Response						
SA	FF	S/0	S/1	C/0	C/1	*D*/0	*D*/1
000	0	0	0	0	0	0	0
001	1	1	**0**	1	1	1	**0**
010	0	0	**1**	0	**1**	0	0
011	1	1	1	1	1	1	**0**
100	0	0	0	0	0	0	0
101	0	**1**	0	0	0	**1**	0
110	1	**0**	1	**0**	1	1	1
111	1	1	1	**0**	1	1	1

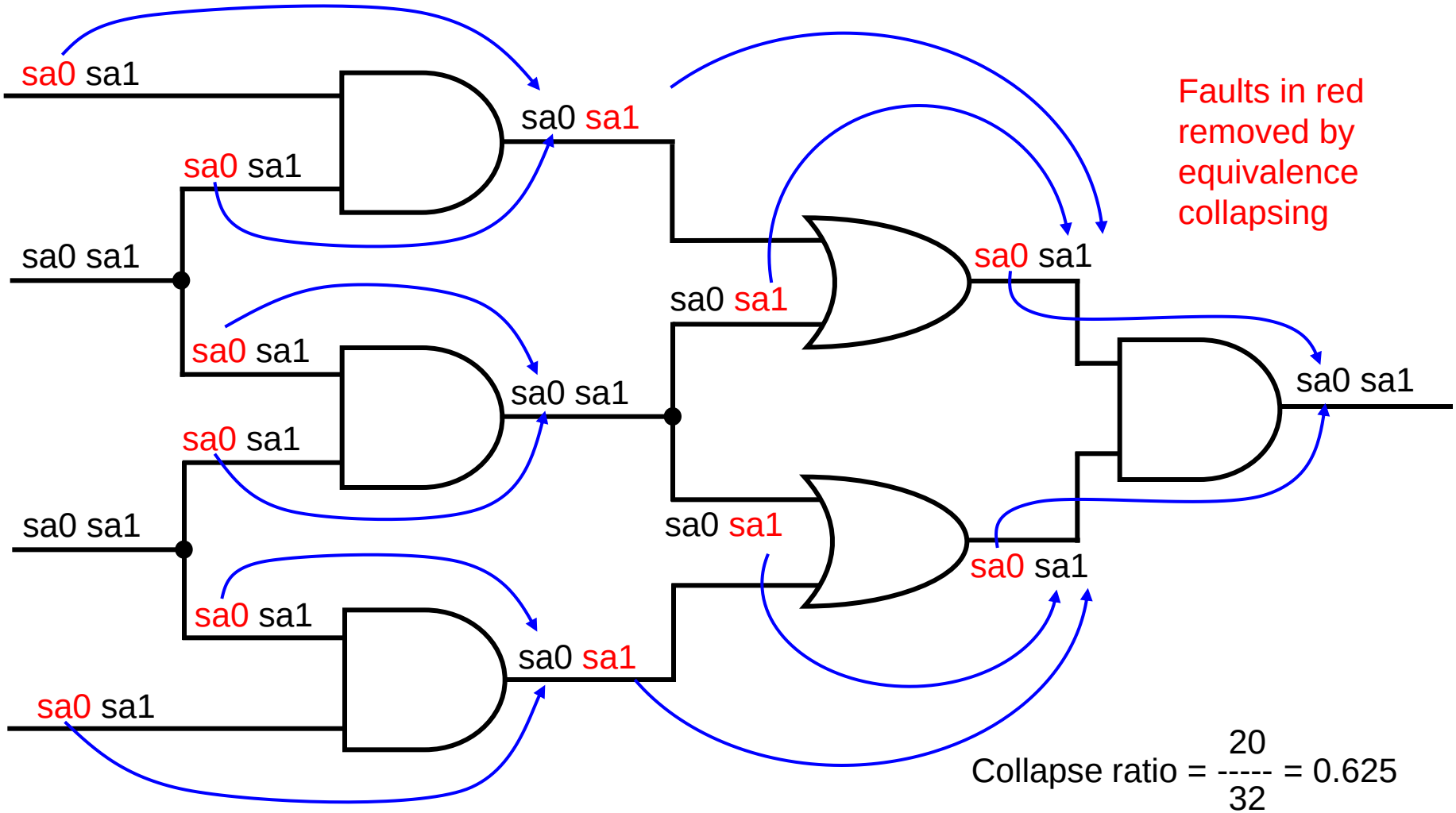
Fault Equivalence

- Number of fault sites in a Boolean gate circuit = #PI + #gates + # (fanout branches).
- Fault equivalence: Two faults f1 and f2 are equivalent if all tests that detect f1 also detect f2.
- If faults f1 and f2 are equivalent then the corresponding faulty functions are identical.
- Fault collapsing: All single faults of a logic circuit can be divided into disjoint equivalence subsets, where all faults in a subset are mutually equivalent. A collapsed fault set contains one fault from each equivalence subset.

Equivalence Rules



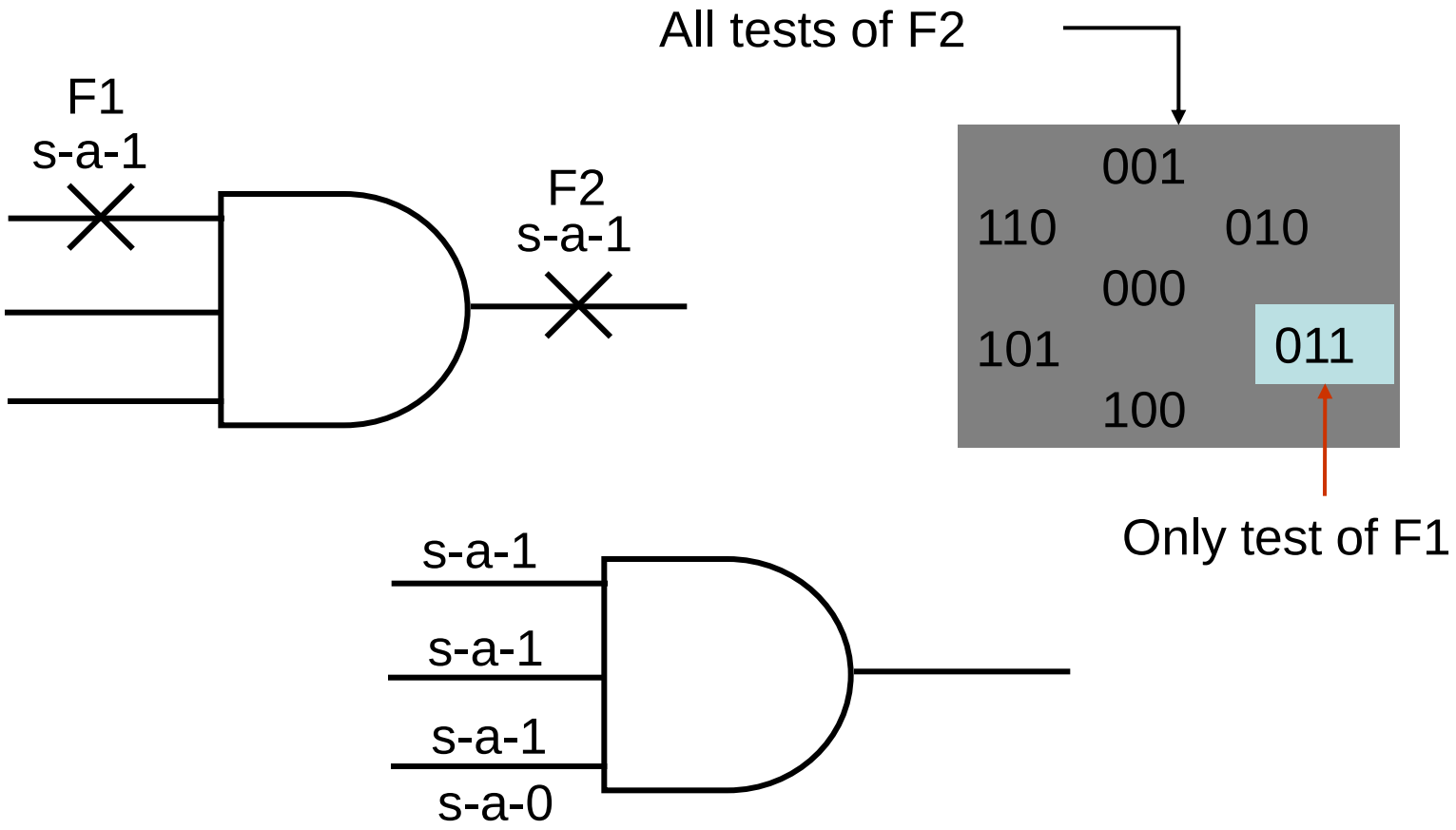
Equivalence Example



Fault Dominance

- If all tests of some fault F1 detect another fault F2, then F2 is said to dominate F1.
- Dominance fault collapsing: If fault F2 dominates F1, then F2 is removed from the fault list.
- When dominance fault collapsing is used, it is sufficient to consider only the input faults of Boolean gates.
- In a tree circuit (without fanouts) PI faults form a dominance collapsed fault set.
- If two faults dominate each other then they are equivalent.

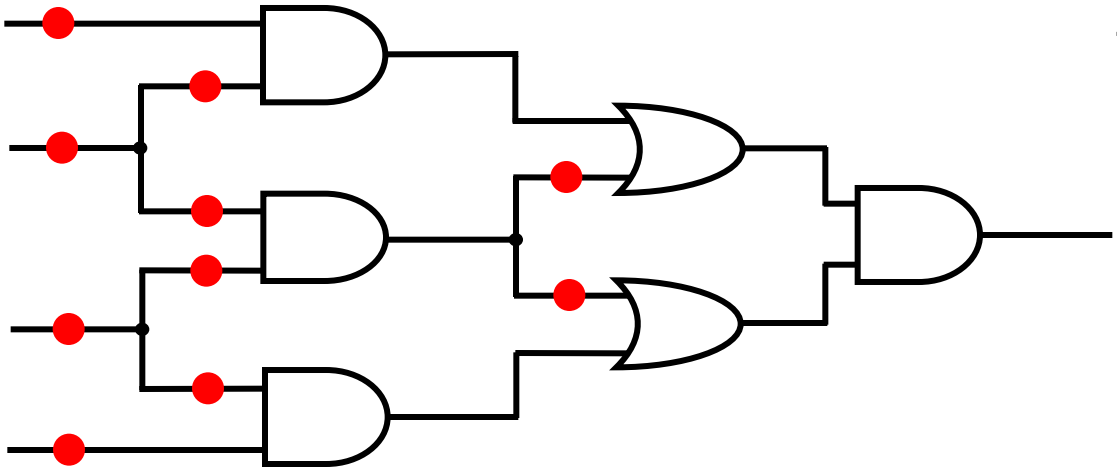
Dominance Example



A dominance collapsed fault set

Checkpoints

- Primary inputs and fanout branches of a combinational circuit are called *checkpoints*.
- Checkpoint theorem: A test set that detects all single (multiple) stuck-at faults on all checkpoints of a combinational circuit, also detects all single (multiple) stuck-at faults in that circuit.



Total fault sites = 16

Checkpoints (●) = 10

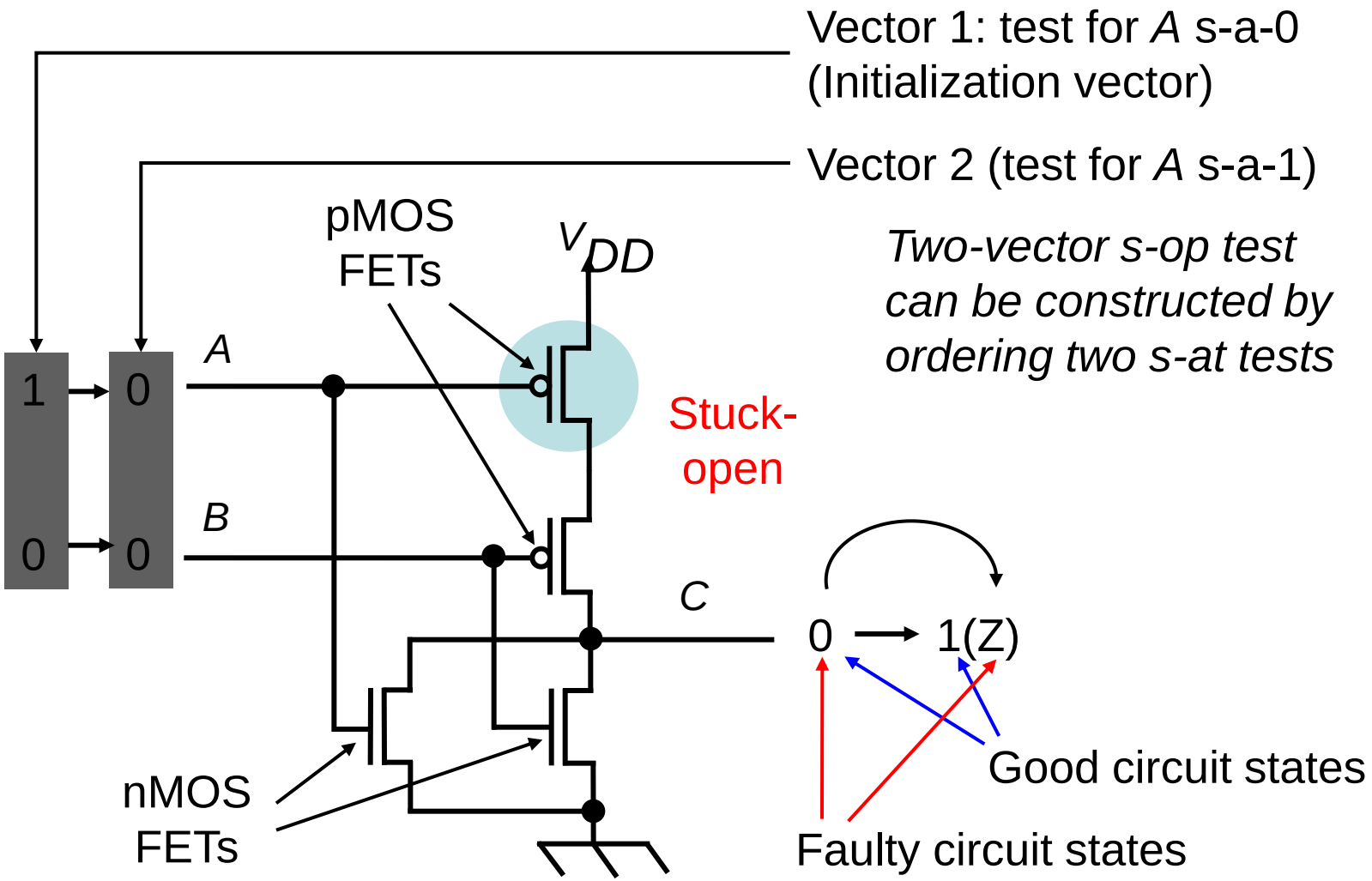
Multiple Stuck-at Faults

- A multiple stuck-at fault means that any set of lines is stuck-at some combination of (0,1) values.
- The total number of single and multiple stuck-at faults in a circuit with *k* single fault sites is 3^k-1.
- A single fault test can fail to detect the target fault if another fault is also present, however, such masking of one fault by another is rare.
- Statistically, single fault tests cover a very large number of multiple faults.

Transistor (Switch) Faults

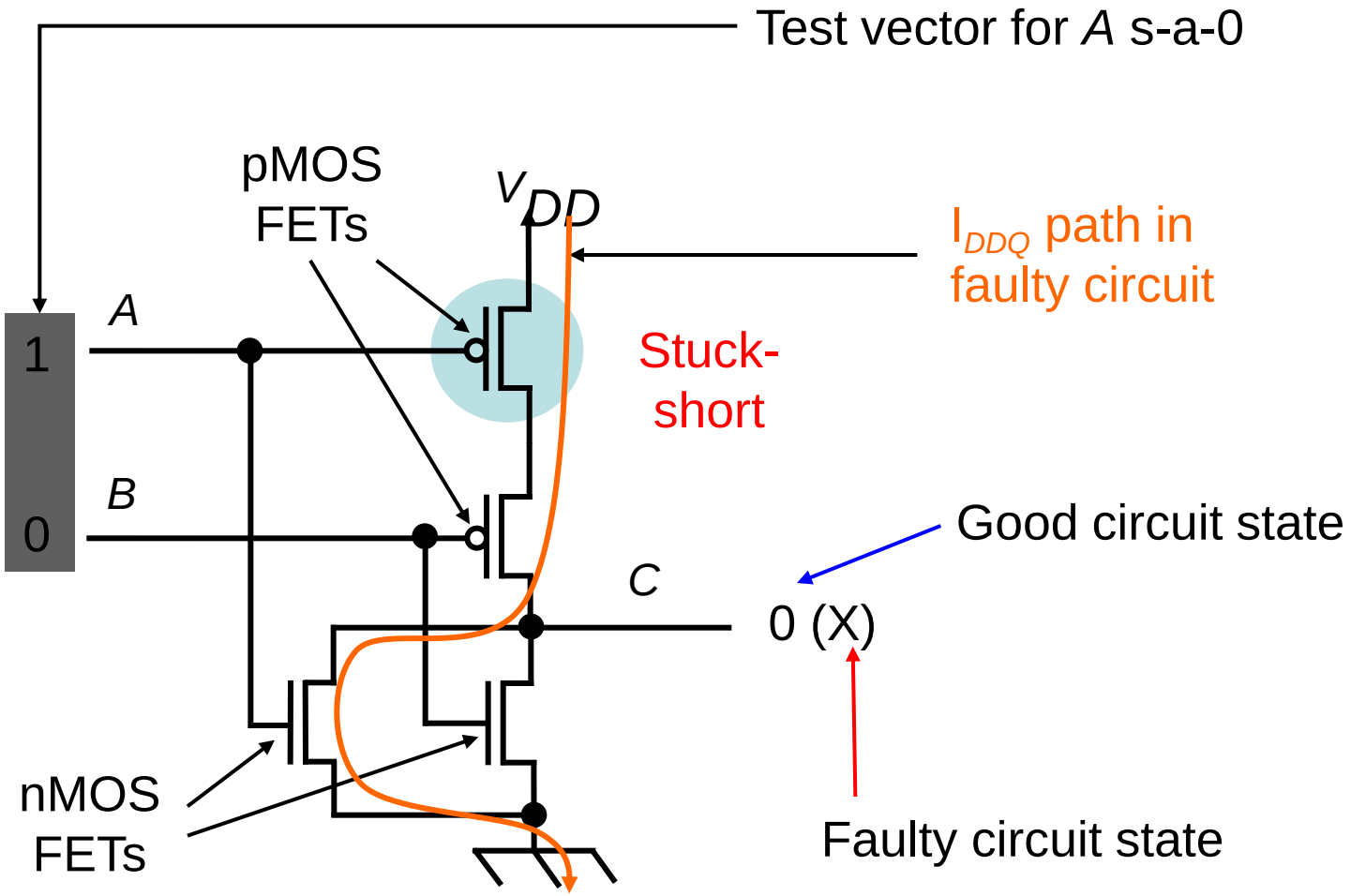
- MOS transistor is considered an ideal switch and two types of faults are modeled:
  - Stuck-open -- a single transistor is permanently stuck in the open state.
  - Stuck-short -- a single transistor is permanently shorted irrespective of its gate voltage.
- Detection of a stuck-open fault requires two vectors.
- Detection of a stuck-short fault requires the measurement of quiescent current (I_{DDQ}).

Stuck-Open Example



Two-vector s-op test can be constructed by ordering two s-at tests

Stuck-Short Example



Fault Model - Summary

- Fault models are analyzable approximations of defects and are essential for a test methodology.
- For digital logic single stuck-at fault model offers best advantage of tools and experience.
- Many other faults (bridging, stuck-open and multiple stuck-at) are largely covered by stuck-at fault tests.
- Stuck-short and delay faults and technology-dependent faults require special tests.
- Memory and analog circuits need other specialized fault models and tests.

Thank You