

Instruction Set Architecture

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Computer Organization & Architecture



Lecture 5 (22 March 2013)

CADSL

Instruction Set Architecture

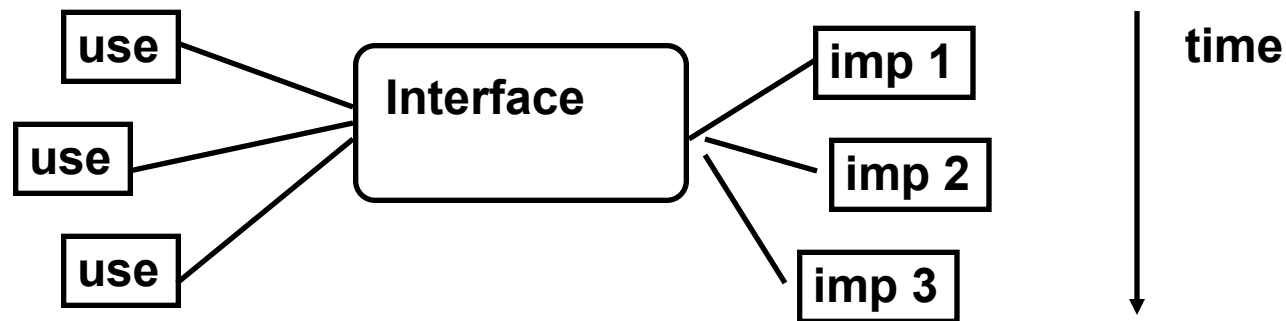
- Instruction set architecture is the structure of a computer that a machine language programmer must understand to write a correct (timing independent) program for that machine.
- The instruction set architecture is also the machine description that a hardware designer must understand to design a correct implementation of the computer.



Interface Design

A good interface:

- Lasts through many implementations (portability, compatibility)
- Is used in many different ways (generality)
- Provides *convenient* functionality to higher levels
- Permits an *efficient* implementation at lower levels



Evolution of Instruction Sets

Single Accumulator (EDSAC 1950)



Accumulator + Index Registers

(Manchester Mark I, IBM 700 series 1953)



Separation of Programming Model
from Implementation



High-level Language Based

(B5000 1963)

Concept of a Family

(IBM 360 1964)

General Purpose Register Machines



Complex Instruction Sets

(Vax, Intel 432 1977-80)

Load/Store Architecture

(CDC 6600, Cray 1 1963-76)



RISC

(Mips, Sparc, HP-PA, IBM RS6000, PowerPC . . .1987)



LIW/"EPIC"?

(IA-64. . .1999)



Evolution of Instruction Sets

- Major advances in computer architecture are typically associated with landmark instruction set designs
 - Ex: Stack vs GPR (System 360)
- Design decisions must take into account:
 - technology
 - machine organization
 - programming languages
 - compiler technology
 - operating systems
- And they in turn influence these



What Are the Components of an ISA?

- Sometimes known as *The Programmer's Model* of the machine
- Storage cells
 - General and special purpose registers in the CPU
 - Many general purpose cells of same size in memory
 - Storage associated with I/O devices
- The machine instruction set
 - The instruction set is the entire repertoire of machine operations
 - Makes use of storage cells, formats, and results of the fetch/execute cycle
 - i.e., register transfers



What Are the Components of an ISA?

- The instruction format
 - Size and meaning of fields within the instruction
- The nature of the fetch-execute cycle
 - Things that are done before the operation code is known



Instruction

- C Statement

$f = (g+h) - (i+j)$

- Assembly instructions

add t0, g, h

add t1, i, j

sub f, t0, t1

- Opcode/mnemonic, operand , source/
destination



Thank You



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