Reduced Instruction Set Computer

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Computer Organization & Architecture

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80x86 Instruction Frequency (SPECint92)

Rank	Instruction	Frequency
1	load	22%
2	branch	20%
3	compare	16%
4	store	12%
5	add	8%
6	and	6%
7	sub	5%
8	register move	4%
9	call	1%
10	return	1%
Total		96%

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# Relative Frequency of Control Instructions

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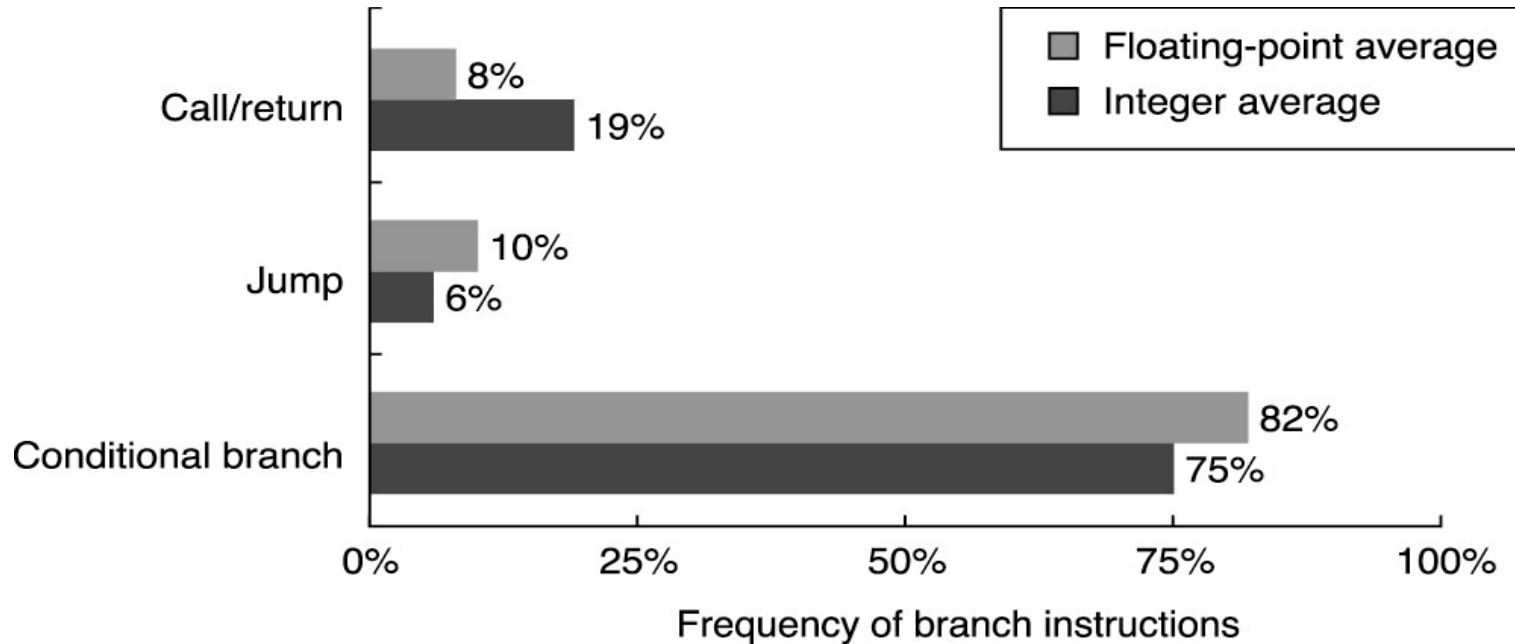
Control instructions (contd.)

- Addressing modes

  ➢ PC-relative addressing (independent of program load & displacements are close by)

    - Requires displacement (how many bits?)
    - Determined via empirical study. [8-16 works!]

  ➢ For procedure returns/indirect jumps/kernel traps, target may not be known at compile time.

    - Jump based on contents of register
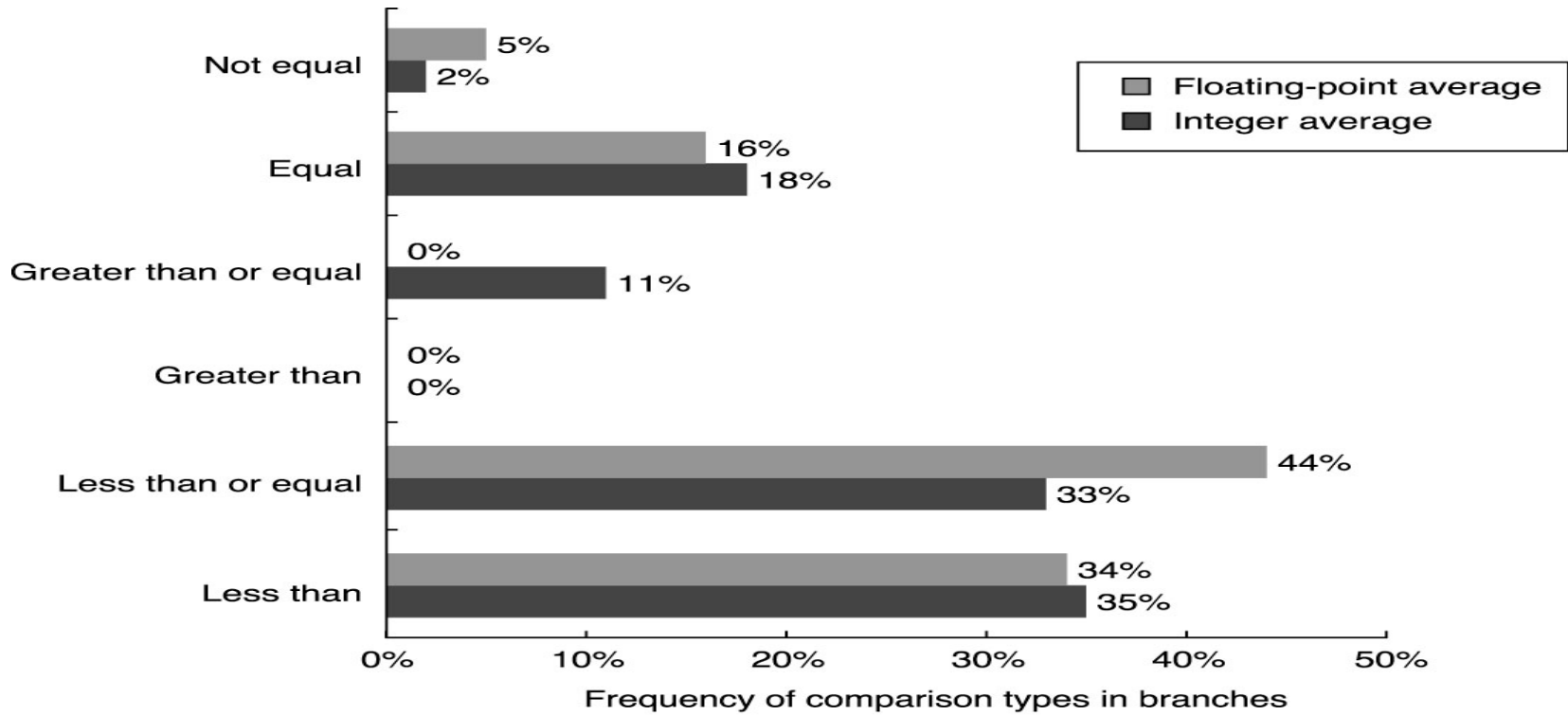   - Useful for switch/(virtual) functions/function ptrs/ dynamically linked libraries etc.

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Branch Distances (in terms of number of instructions)

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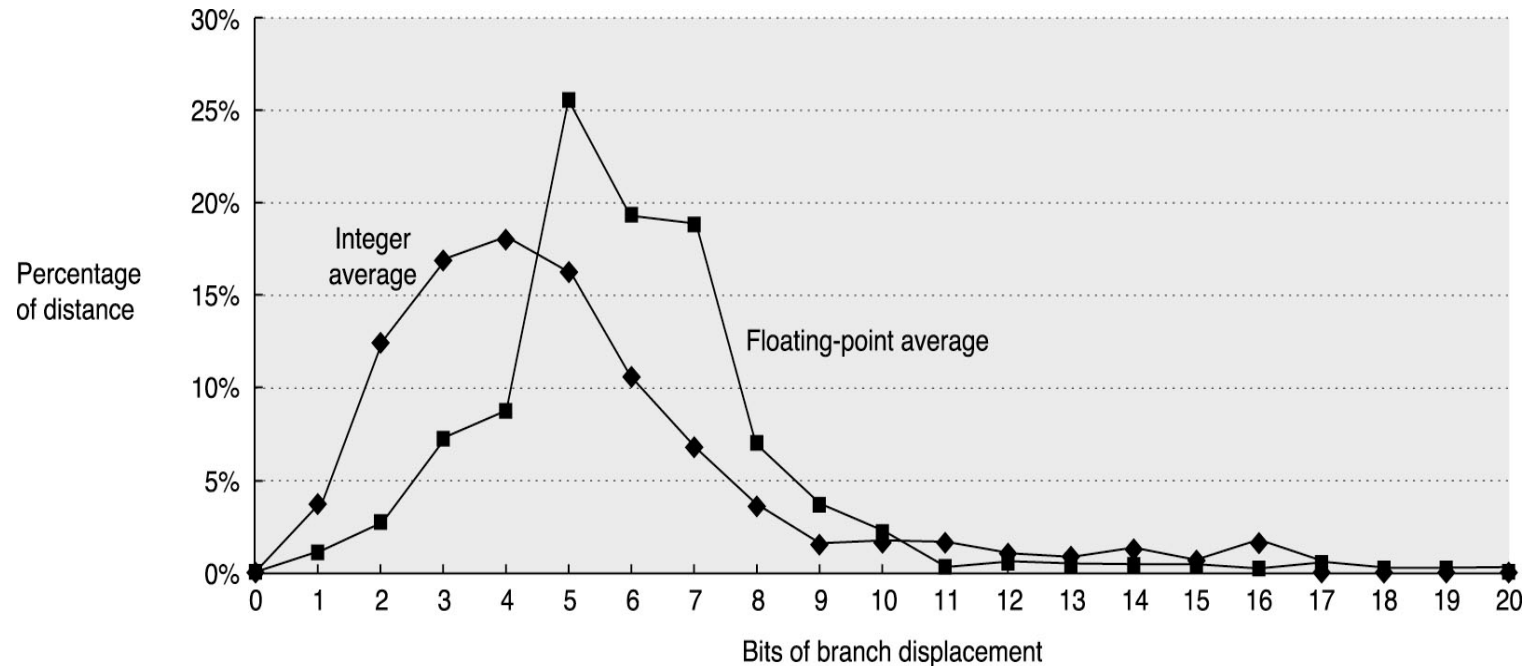
Frequency of Different Types of Compares in Conditional Branches

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Encoding an Instruction set

- desire to have as many registers and addressing mode as possible

- the impact of size of register and addressing mode fields on the average instruction size and hence on the average program size

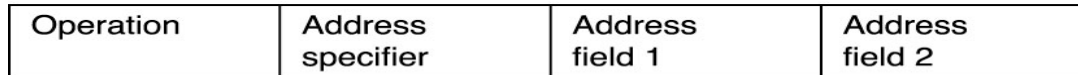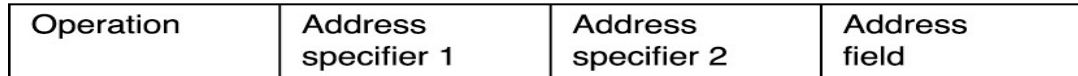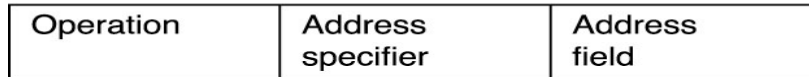- a desire to have instruction encode into lengths that will be easy to handle in the implementation

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Three choice for encoding the instruction set

Operation and no. of operands	Address specifier 1	Address field 1	• • •	Address specifier	Address field

(a) Variable (e.g., VAX, Intel 80x86)

Operation	Address field 1	Address field 2	Address field 3

(b) Fixed (e.g., Alpha, ARM, MIPS, PowerPC, SPARC, SuperH)

Operation	Address specifier	Address field

Operation	Address specifier 1	Address specifier 2	Address field

Operation	Address specifier	Address field 1	Address field 2

(c) Hybrid (e.g., IBM 360/70, MIPS16, Thumb, TI TMS320C54x)

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Thank You

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