CS-683: Advanced Computer Architecture

Course Introduction

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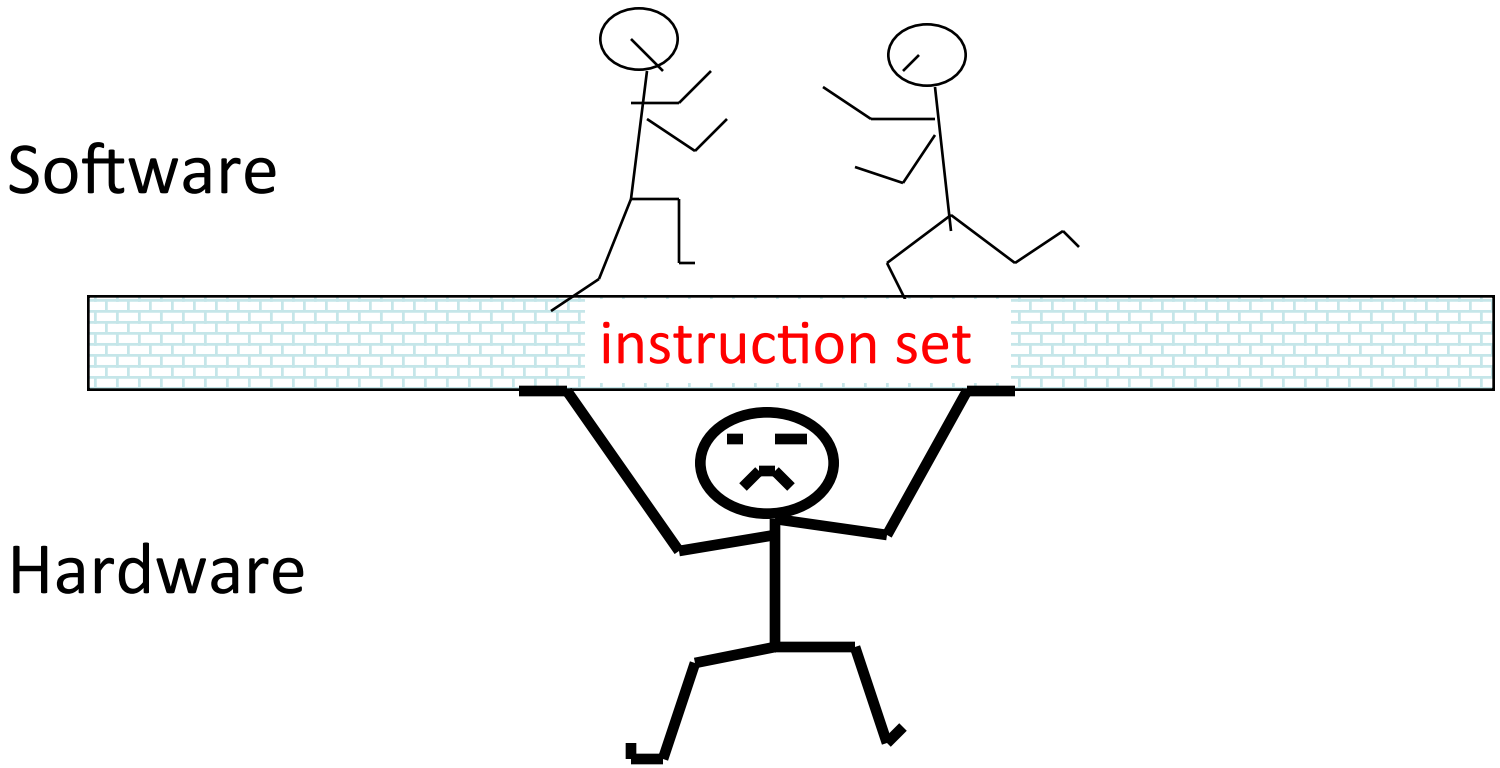
Computer Architecture's Changing Definition

- 1950s to 1960s:
  Computer Architecture Course = Computer Arithmetic
- 1970s to mid 1980s:
  Computer Architecture Course = Instruction Set Design, especially ISA appropriate for compilers
- 1990s onwards:
  Computer Architecture Course = Design of CPU (Processor Microarchitecture), memory system, I/O system, Multiprocessors

Instruction Set Architecture (ISA)



Running Program on Processor

$$\text{Processor Performance} = \frac{\text{Time}}{\text{Program}}$$

$$= \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Time}}{\text{Instruction}}$$

(code size)

Architecture

Compiler Designer

Computer Architecture

- Instruction Set Architecture (IBM 360)
  - *… the attributes of a [computing] system as seen by the programmer. I.e. the conceptual structure and functional behavior, as distinct from the organization of the data flows and controls, the logic design, and the physical implementation. -- Amdahl, Blaaw, & Brooks, 1964*

Running Program on Processor

$$\text{Processor Performance} = \frac{\text{Time}}{\text{Program}}$$

$$= \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Cycles}}{\text{Instruction}} \times \frac{\text{Time}}{\text{Cycle}}$$

(code size) (CPI)

Architecture --> Implementation

Compiler Designer **Processor Designer**

Running Program on Processor

$$\text{Processor Performance} = \frac{\text{Time}}{\text{Program}}$$

$$= \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Cycles}}{\text{Instruction}} \times \frac{\text{Time}}{\text{Cycle}}$$

(code size) (CPI) (cycle time)

Architecture --> Implementation --> Realization

Compiler Designer **Processor Designer** **Chip Designer**

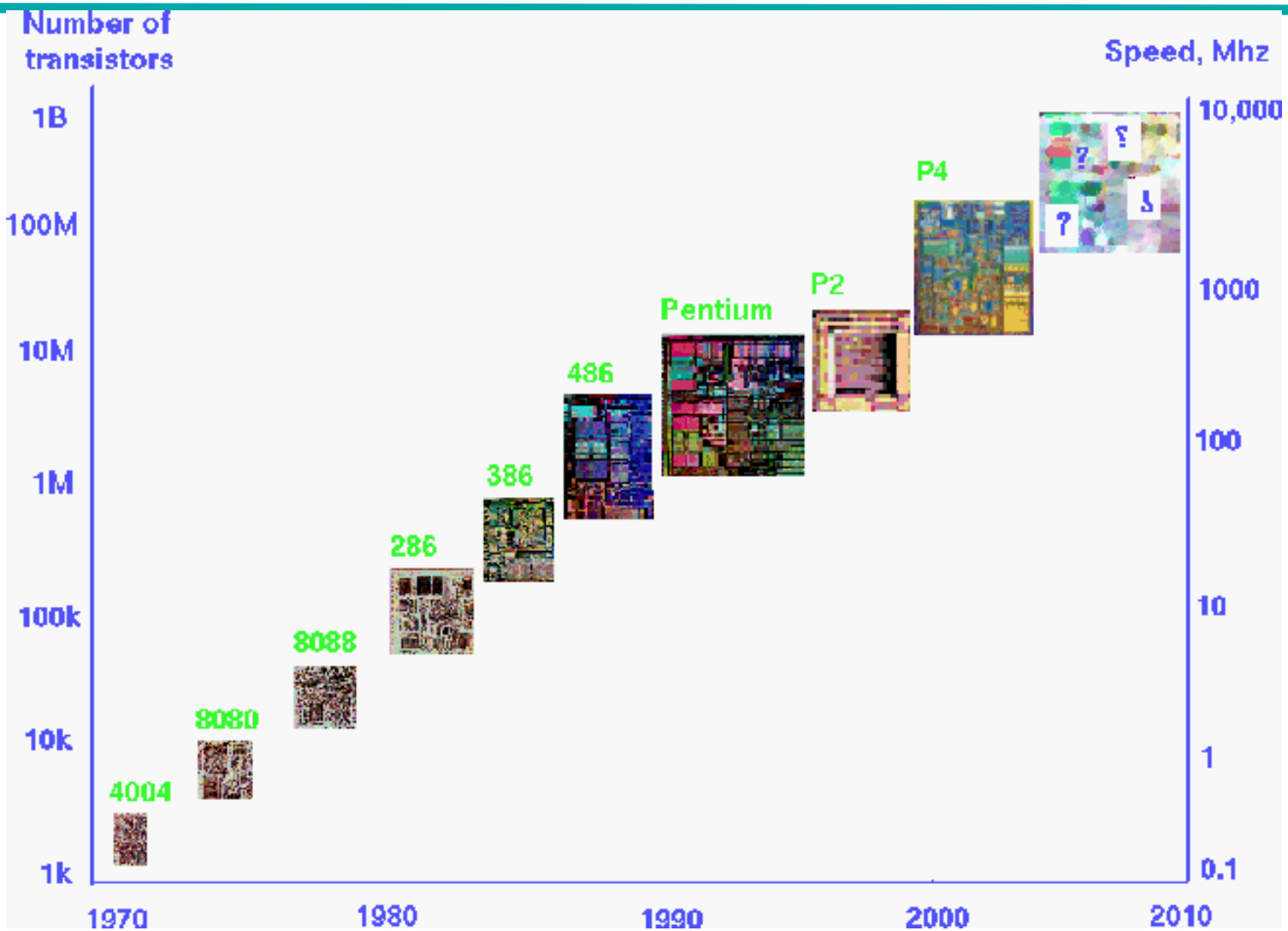
Iron Law

- Instructions/Program
  - Instructions executed, not static code size
  - Determined by algorithm, compiler, ISA
- Cycles/Instruction
  - Determined by ISA and CPU organization
  - Overlap among instructions reduces this term
- Time/cycle
  - Determined by technology, organization, clever circuit design

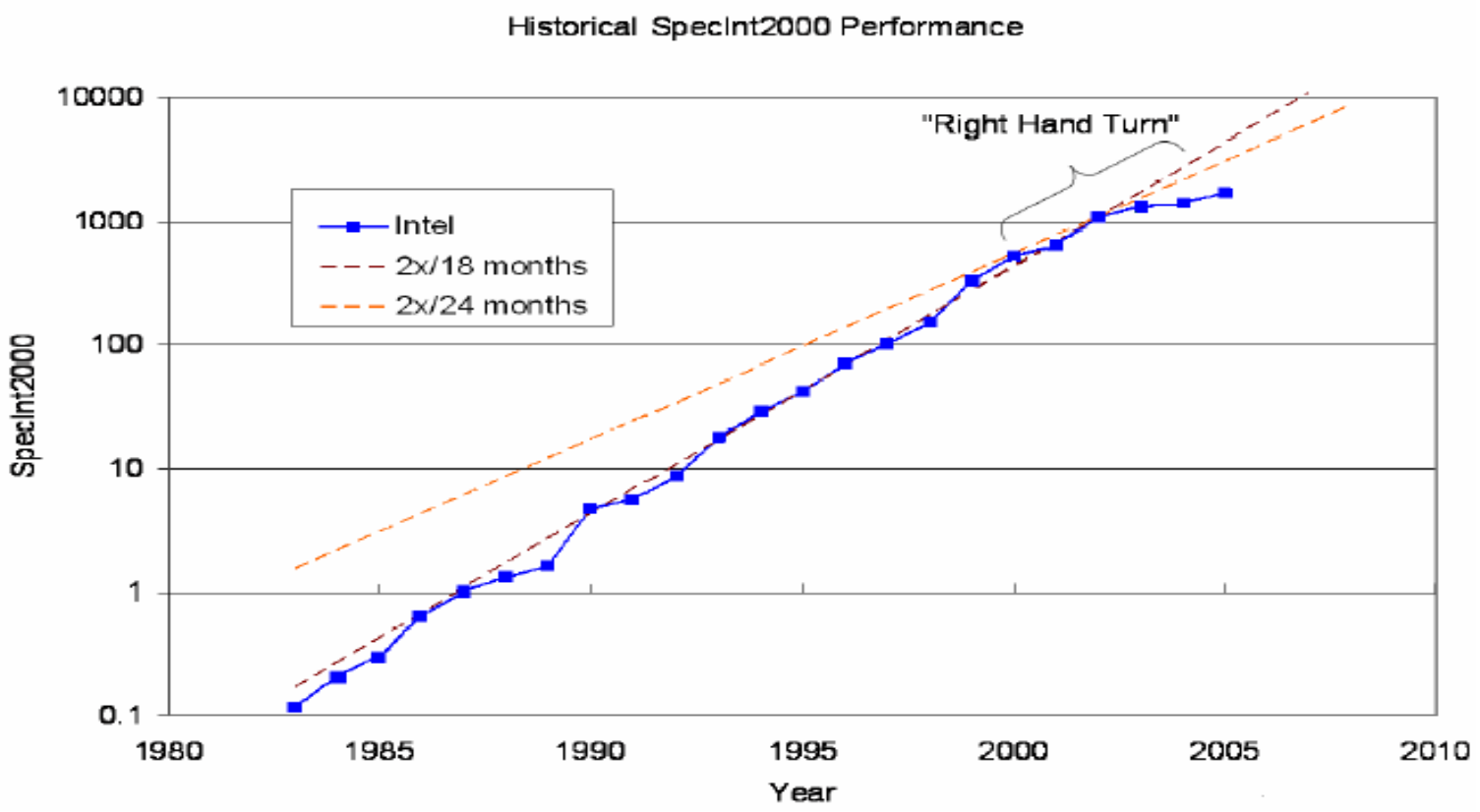
Computer Architecture

- Exercise in engineering tradeoff analysis
  - Find the fastest/cheapest/power-efficient/etc. solution
  - Optimization problem with 100s of variables
- All the variables are changing
  - At non-uniform rates
  - With inflection points
- Two high-level effects:
  - Technology push
  - Application Pull

Microprocessor Designs



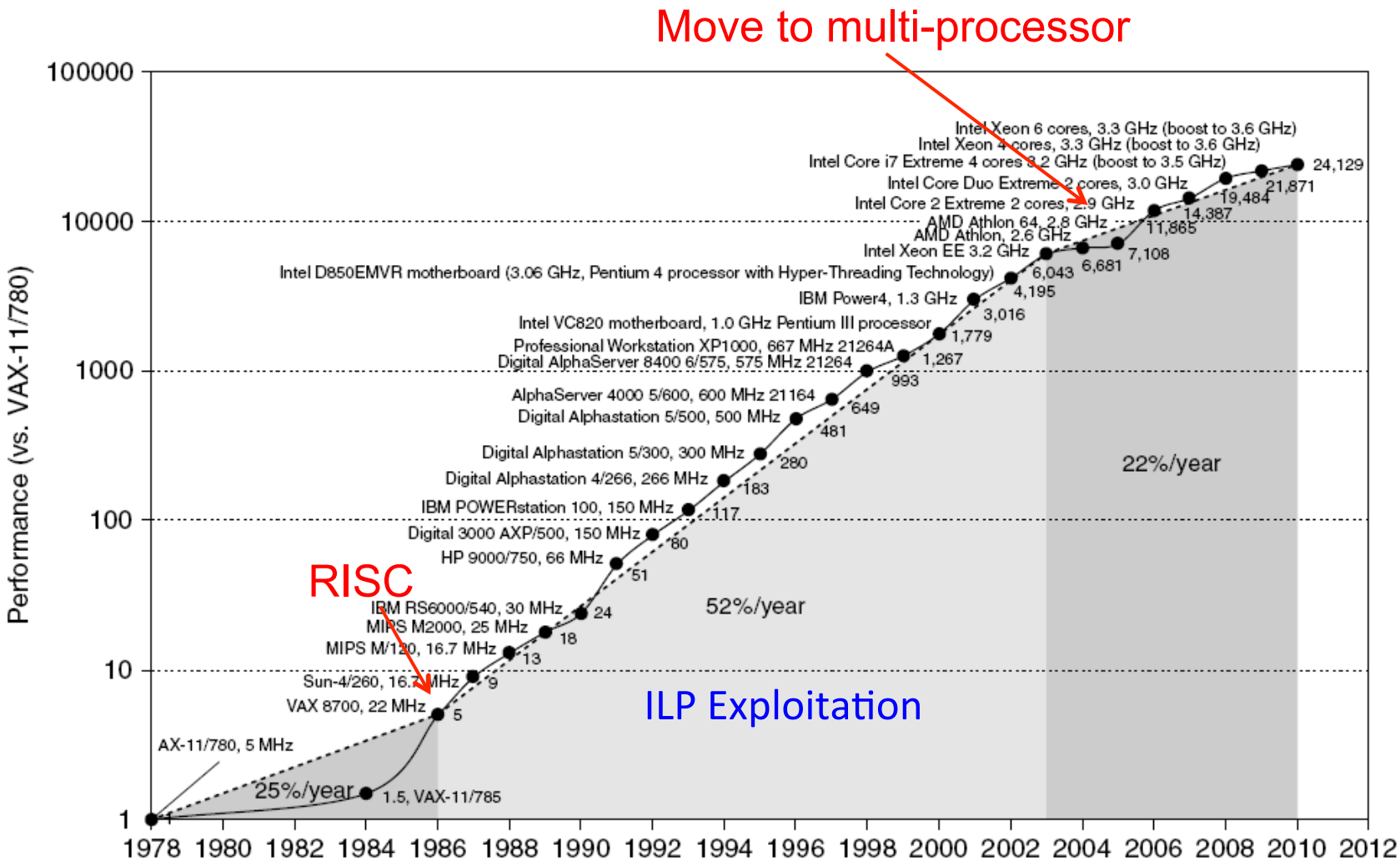
Trends



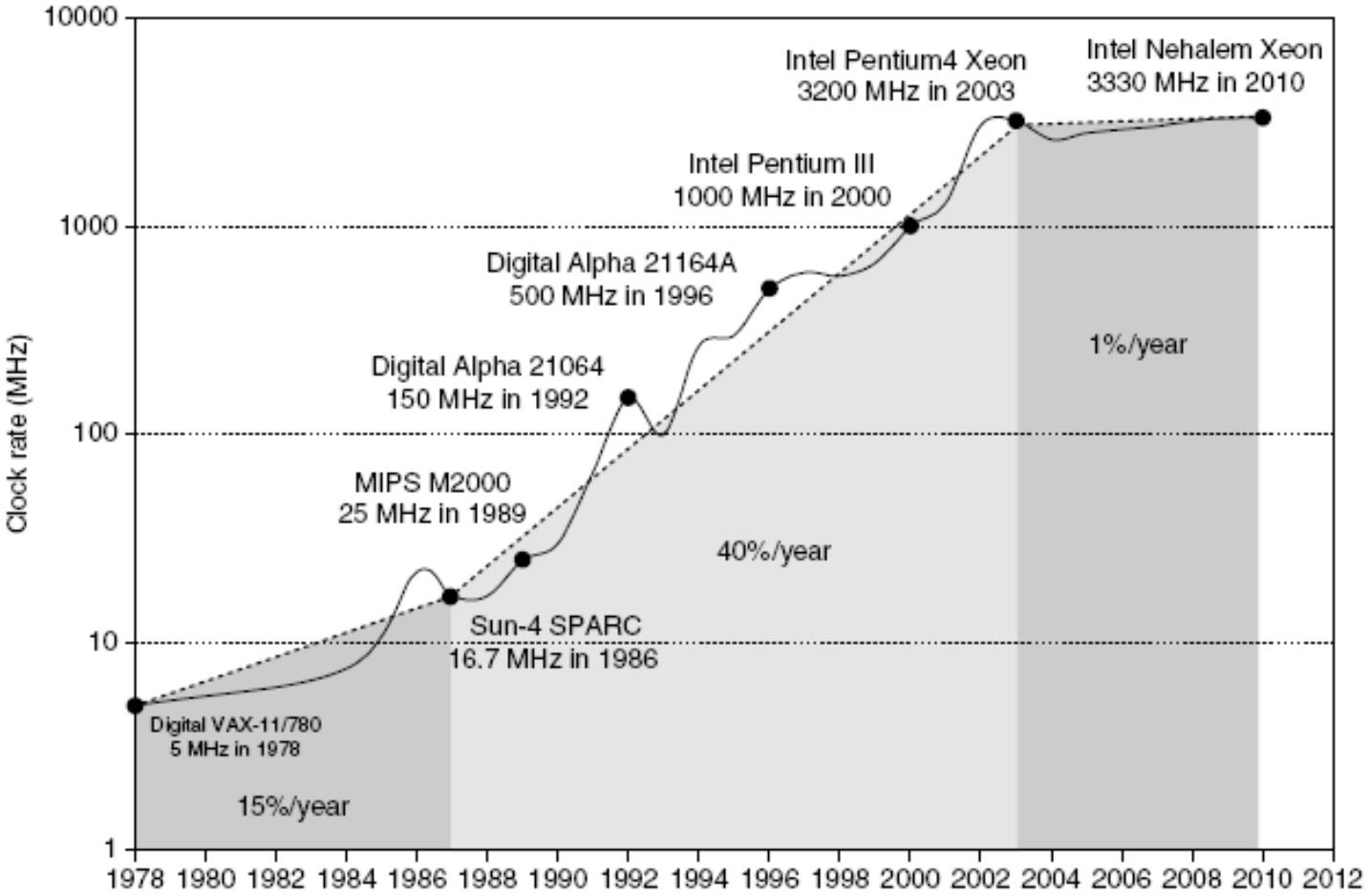
- Moore's Law for device integration
- Chip power consumption
- Single-thread performance trend

[source: Intel]

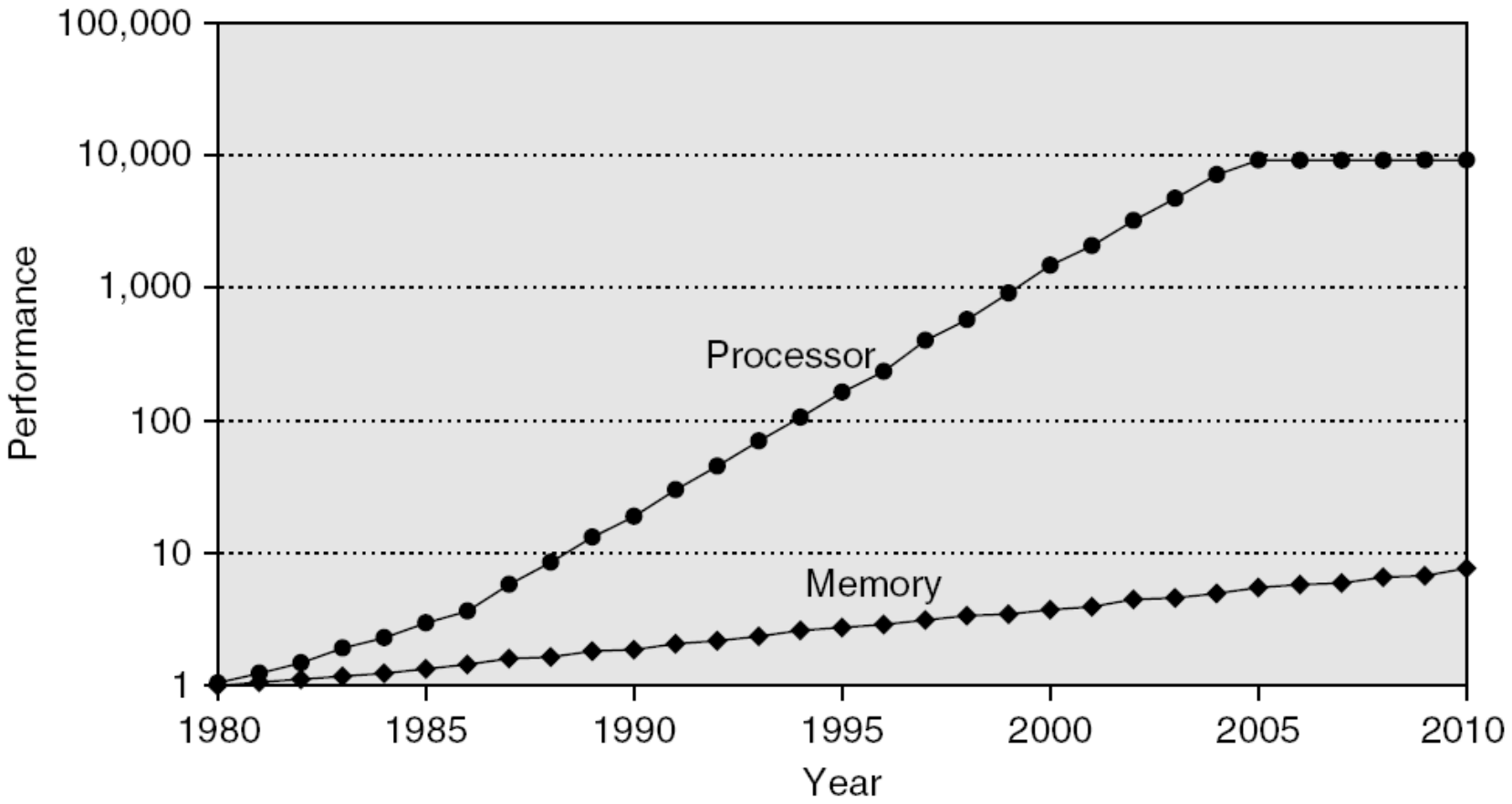
Single Processor Performance



Frequency Scaling



Memory Performance Gap



Express way

Course Outline

- Review: CISC vs. RISC, and Pipelining
- Superscalar Design
- VLIW, Multi-scalar Architectures
- Simultaneous Multi-threaded (SMT) Architecture
- Multi-core Architecture
- Performance Evaluation
- Memory System Design

Course Schedule

Class Hours

- Wednesday: 9:30 am to 11:00 am
- Friday: 9:30 am to 11:30 am

Office Hours:

Course Evaluation

- Mid Term Exam (15%)
  - Open Book/Notes Exam
- Final Exam (30%)
  - Open Book/Notes Exam
- Assignments (15%)
  - Set of assignments will be given periodically
- Course Projects (20%)
  - 1 projects
  - Group (Max size 3)
- Continuous Evaluations (15%) – weekly quiz
  - Weekly Quiz – Open Book (80% best will be counted)
- Presentation and Viva (5%)
- [BONUS] Research Project (15%)
- Saturating counter sums to 100

Books

- Computer Architecture: A quantitative approach
  - Hennessy and Patterson
  - Morgan Kaufman, 5e, 2012
- Modern Processor Design
  - Shen and Lipasti
  - Mc Graw Hill, 2005
- Current Literature (ISCA/Micro/HPCA/ICCD/DSN)

Acknowledgement

- Prof. Mikko Lipasti, Univ. of Wisconsin
- Prof. Kewal Saluja, Univ. of Wisconsin
- Prof. Adit Singh, Auburn Univ.
- Prof. Matthew Jacob, IISc
- Prof. Arun Somani, Iowa State Univ.

Thank You