Rohit Rothe

Personal Information

Address	: 1301 Beal Avenue, Ann Arbor, Michigan - 48109
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Interests	: Low Power Analog & Mixed Signal VLSI Design and RF VLSI Design

Education

University of Michigan, Ann Arbor — Sep 2018 - Present

PhD in Electrical & Computer Engineering
Advisor: Prof. David Blaauw
CGPA: **4.0/4.0**

Indian Institute of Technology Bombay, Mumbai, India — Jul 2013 - Jul 2018

Dual Degree (B.Tech + M.Tech) in Electrical Engineering
CGPA: **9.39/10.00**

Research Experience

Sample and Average Feedback Resistor for Capacitively Coupled Amplifiers — Sep 2018 - Present

Advisors: Prof. David Blaauw & Prof. Dennis Sylvester, *University of Michigan*

- Devising a switched capacitor based feedback structure which ensures DC bias and sets the high pass corner frequency of the amplifier.
- This will be used in lieu of a pseudo resistor which is highly unreliable across temperature, process corners and external illumination conditions.

Dynamic Matching in Direct Conversion Mixers — May 2017 - Jul 2018

Master's Thesis
Advisor: Prof. Rajesh Zele, *IIT Bombay*

- Designing a new topology of Direct Conversion Mixer for RF frequency 2.4 GHz with **improved 2nd order Input Inter-modulation Point (IIP2)** and lower flicker noise making use of Correlated Double Sampling.
- Investigating RF performance improvements using **chopper stabilization** (Correlated Double Sampling) in various topologies for CMOS RF Mixers.

Delta-Sigma ADC for Particulate Measurement System — May 2017 - Jun 2018

Research and Development Project
Advisor: Prof. Maryam S. Baghini, *IIT Bombay*

- Designing a low-voltage, low power and high bandwidth Delta Sigma ADC with **12-bits** resolution
- Aimed to be compatible with requirements of precise **portable energy autonomous instrumentation** systems. Target future application is particulate measurement system with **sensitivity** of **1 ppm** (collaboration with University of Cambridge, UK).

Select Course Projects

Hardware for Chiron Basecaller | EECS 627 : VLSI Design II — Winter 2019

Instructor: Prof. David Blaauw, University of Michigan

- Implemented hardware for a neural network consisting of 3 ResNets and 3 layers of bidirectional RNN layers
- Achieved a performance of 3.2 TOPS/W @ 10 MHz for the CNN. The overall size of the design is 1.68 cm^2 in 130 nm IBM technology.

Wide Bandwidth Tran-Impedance Amplifier | EECS 413 : Monolithic Amplifer Circuits — Fall 2018

Instructor: Prof. Ehsan Afshari, University of Michigan

Designed a 3 stage 4 GHz bandwidth TIA based on inductive peaking for optical fibre communication

Rational Arithmetic Accelerator | EE 705 : VLSI Design Lab — Spring 2017

Instructor: Prof. Sachin Patkar, IIT Bombay

Optimized 8 bit Dadda multiplier to design 13 stage pipeline for 32 bit multiplier using optimal carry save adders & 8 stage pipelined carry select adders to reduce delay. Achieved > 2x increase in maximum operating frequency.

Impedance Meter using Audio I/O | EE 348 : Electronic Design Lab Spring 2016
Instructor: Prof. Joseph John, IIT Bombay

- Developed portable Impedance meter using laptop's audio I/O port for sinusoidal excitation as input
- Implemented design on PCB and made fully functional prototype with an error within 5%.

Academic Achievements

- Awarded the **Certificate of Appreciation for Excellence in Teaching Assistantship** for the graduate level course of CMOS Analog VLSI Design in the Autumn 2017 semester.
- All-India Rank of **136** in Joint Entrance Examination (JEE - Main) among more than 1.3 million candidates.
- Awarded the **Institute Technical Special Mention** for exemplary performance in the year of 2015-16.

Work Experience

Design and Analysis of Phase Locked Loops May 2016 - Jul 2016
Guide: Mr. Rajendrakumar Joish, High Precision Analog Group, Texas Instruments, India

- Investigated the different **architectures** of Phase Locked Loops (PLLs) and characterized their stability using continuous time and discrete time and frequency domain analysis.
- Studied the various designs of individual components constituting a PLL such as Phase Frequency Detector, Charge Pump, Loop Filter, Voltage Controlled Oscillators and Frequency Divider.

Product Development Experience

Design and Fabrication of Electric Vehicle for Formula Student May 2014 - Jul 2016
*Part of IIT Bombay Racing Team of 70 students to build India's Fastest Electric racecar for **Formula Student UK**, an international racecar competition; won **FS Award of £3000** for major design improvements*

- Designed and implemented the team's first **Controller Area Network (CAN)** based sensor network on the ORCA car thereby enabling an efficient bus based system for data collection.
- Enabled higher data speed of 500 kBps with increased accuracy and supplemented seamless system integration by significantly reducing the wiring and hence **reducing the harness size** .
- Headed Data Acquisition Division (DAQ), overseeing the team of 4 Junior Design Engineers

Academic Services - Teaching Assistant

- **EE 619: RF Microelectronics Chip Design**, IIT Bombay Spring 2019
- **EE 618: CMOS Analog VLSI Design**, IIT Bombay Autumn 2017
- **EE 101: Introduction to Electrical and Electronic Systems**, IIT Bombay Summer 2017

Technical Proficiency

Software	Virtuoso, Calibre, Quartus, NgSpice, LTspice, Eagle
Languages	VHDL, Verilog, C++, Python, MATLAB

Relevant Graduate Coursework

University of Michigan	Monolithic Amplifier Circuits, VLSI Design I, VLSI Design II, Advanced Analog and Mixed Signal Circuits
IIT Bombay	RF Microelectronics Chip Design, Mixed Signal VLSI Design, CMOS Analog VLSI Design, Systems Design, Digital VLSI Design, Foundations of VLSI CAD