The 24th Asian Test Symposium (ATS'15)

Indian Institute of Technology Bombay
Mumbai, India, Nov 22 – 25, 2015
https://www.ee.iitb.ac.in/ats15/

Call for Papers

ATS'15 is the twenty fourth in this series of symposia started in 1992 devoted to testing, fault tolerant computing and the design of reliable circuits and systems. ATS is recognized as the main event in Asia that covers the many dimensions of testing and fault-tolerance. The symposium focuses on the key test challenge will arise due to the ability to design complex systems such as robots that encompass sensors, communication systems, processors, transducers and enabling software. In addition to passing post-manufacture test procedures, such systems and relevant devices must exhibit fault-tolerance and survivability characteristics.

REGULAR PAPERS: The ATS'15 Program Committee invites original, unpublished paper submissions on the following topics. Paper submissions should be complete manuscripts, not exceeding six pages (including figures, tables, and bibliography) in a standard IEEE two-column format. The submission will be considered evidence that upon acceptance the author(s) will submit a final camera-ready version of the paper for inclusion in the proceedings, and will present the paper at the symposium. The best paper will be selected by the ATS'15 Program Committee for the *best paper award* based on the criteria of innovation, potential impact, and presentation quality.

INDUSTRY TRACK: ATS'15 also invites 1 page proposals for presentations on state-of-the-art test topics and practices in the industry track. Proposals for individual presentations or a full session should include the title of each presentation, a brief abstract, bio of the speaker (s), and approval status for participation at ATS.

All the submissions including the industry track can be done at ATS-2015 submission site.

Topics of interest include (but are not limited to):

- Test generation & fault simulation
- Fault diagnosis
- Memory testing and FPGA testing
- Delay fault testing / Low power testing
- System-on-a-chip- test/ System-in-package test
- Software testing / verification
- Failure analysis / fault modeling
- Fault tolerance / error correction
- IDDQ testing
- Test standard: IEEE 1500, boundary scan
- Automatic test equipment
- Testing of adaptive circuits and systems
- DfX: Design for testability, reliability, dependability
- Analog & mixed-signal/RF/IO testing
- Wafer-level testing
- Board and system testing / On-line testing
- Network-on-a-chip testing
- CPU testing
- Built-in self-test / Embedded testing
- Functional testing
- Test economics
- Test experience in industry
- Yield Enhancement / Silicon debug
- System level testing

Important Dates

Paper submission: May 25, 2015
Notification of acceptance: Aug 15, 2015
Camera ready manuscript: Sep 5, 2015
Industry track submission: June 30, 2015

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