ATS 2015 Schedule

Day 0 (22 Nov 2015 – Tutorial)

Half Day Tutorial (2:00 pm – 5:00 pm)

Topic: Post Silicon Debug and Patchable Design

Presenter: Masahiro Fujita (Tokyo Univ.), Virendra Singh (IITB), and Rajesh Mittal (Texas Instruments)

ATS 2015 Paper Sessions

Day 1 (23 Nov 2015 – Monday)

1A. Power Aware Testing (11:30 am – 1:00 pm)

Session Chair: Ilia Polian, Univ. of Passau, Germany

Sungyoul Seo, Yong Lee, Hyeonchan Lim, Joohwan Lee, Hongbom Yoo, Yojoung Kim and Sungho Kang: Scan Chain Reordering-aware X-Filling and Stitching for Scan Shift Power Reduction

Zhou Jiang, Dong Xiang and Kele Shen: A Novel Scan Segmentation Design for Power Controllability and Reduction in At-Speed Test

Masayoshi Yoshimura, Yoshiyasu Takahashi, Hiroshi Yamazaki and Toshinori Hosokawa: A Don't Care Filling Method to Reduce Capture Power based on Correlation of FF Transitions

1B. New DFT Approaches (11:30 am – 1:00 pm)

Session Chair: Kuen -Jong Lee, National Cheng Kung Univ., Taiwan

Jyotirmoy Saikia, Industry Talk (Synopsys India): Designing Efficient Multi-Codec Scan Compression

Jerzy Tyszer, Grzegorz Mrugalski, Janusz Rajski, Jedrzej Solecki and Chen Wang: TestExpress – New Time-Effective Scan-Based Deterministic Test Paradigm

Satyadev Ahlawat, Jaynarayan Tudu, Anzhela Matrosova, and Virendra Singh: A New Scan Flip-Flop Design to Eliminate Performance Penalty of Scan

2A. Test Generation (2:00 pm – 4:00 pm)

Session Chair: Stefan Holst, Kyushu Institute of Technology, Japan

Sajjad Pagarkar, Industry Talk (Qualcomm USA): Challenges in High Volume Testing -100M+ Parts

Masahiro Fujita: Detection of test patterns with unreachable states through efficient invariant identification

Tetsuya Masuda, Jun Nishimaki, Toshinori Hosokawa and Hideo Fujiwara: A Test Generation Method for Data Paths Using Easily Testable Functional Time Expansion Models and Controller Augmentation

Chun-Hao Chang, Kuen-Wei Yeh, Jiun-Lang Huang and Laung-Terng Wang: SDC-TPG: A Deterministic Zero-Inflation Parallel Test Pattern Generator

2B. Memory Test and Repair (2:00 pm – 4:00 pm)

Session Chair: Xiaowei Li, Chinese Academy of Sciences, China

Shyue-Kung Lu and Masaki Hashizume: Integration of Hard Repair Techniques with ECC for Enhancing Fabrication Yield and Reliability of Embedded Memories

Guopei Liu, Ying Wang, Huawei Li and Xiaowei Li: A Lightweight Timing Channel Protection for Shared Memory Controllers

Josef Kinseher, Leonardo Zordan and Ilia Polian: On the Use of Assist Circuits for Improved Coupling Fault Detection in SRAMs

Che-Wei Chou, Yong-Xiao Chen and Jin-Fu Li: Testing Inter-Word Coupling Faults of Wide IO DRAMs

3A. Testing 3D Structures (4:30 pm – 6:00 pm)

Session Chair: Madhav Desai, IIT Bombay, India

Rajit Karmakar, Aditya Agarwal and Santanu Chattopadhyay: Test Infrastructure Development and Test Scheduling of 3D-Stacked ICs Under Resource and Power Constraints

Konstantin Shibin, Vivek Chickermane, Brion Keller, Christos Papameletis and Erik Jan Marinissen: At-speed Testing of Inter-Die Connections of 3D-SICs in the Presence of Shore Logic

Jun Zhou, Huawei Li, Tiancheng Wang, Ying Wang and Xiaowei Li: TWiN: A Turn-Guided Reliable Routing Scheme for Wireless 3D NoCs

3B. Standards Test and Security (4:30 pm – 6:00 pm)

Session Chair: Liviu Miclea, TU Cluj-Napoca, Romania

Rajesh Khurana, Industry Talk (Cadence India): The Application of iJTAG (IEEE 1687) for Pattern Re-targeting and IEEE 1500 Core-based Hierarchical Testing

Riccardo Cantoro, Mehrdad Montazeri, Matteo Sonza Reorda, Farrokh Ghani Zadegan and Erik Larsson: On the Testability of IEEE 1687 Networks

Hejia Liu and Vishwani Agrawal: Securing IEEE 1687-2014 Standard Instrumentation Access by LFSR Key

Day 2 (24 Nov 2015 – Tuesday)

4A. Timing and Delay Test (11:30 am – 1:30 pm)

Session Chair: Sybille Hellebrand, Uni. of Paderborn, Germany

Xijiang Lin, Wu-Tung Cheng and Janusz Rajski: On Improving Transition Test Set Quality to Detect CMOS Transistor Stuck-Open Faults

Koji Asada, Xiaoqing Wen, Stefan Holst, Kohei Miyase, Seiji Kajihara, Michael A. Kochte, Eric Schneider, Hans-Joachim Wunderlich and Jun Qian: Logic/Clock-Path-Aware At-Speed Scan Test Generation for Avoiding False Capture Failures and Reducing Clock Stretch

Sybille Hellebrand, Thomas Indlekofer, Matthias Kampmann, Michael Kochte, Eric Schneider and Hans-Joachim Wunderlich: Optimized Selection of Frequencies for Faster-Than-at-Speed Test

Ankush Srivastava, Virendra Singh, Adit D Singh and Kewal K Saluja: A Methodology for Identifying High Timing Variability Paths in Complex Designs

4B. Circuits for Security and Resilience (11:30 am – 1:30 pm)

Session Chair: Vizhinathan Kamakoti, IIT Madras, India

Dooyoung Kim, Muhammad Adil Ansari, Jihun Jung and Sungju Park: SCAN-PUF: PUF Elements Selection Methods for Viable IC Identification

Sabyasachi Deyati, Barry Muldrey, Adit Singh and Abhijit Chatterjee: Challenge Engineering and Design of Analog Push Pull Amplifier Based Physically Unclonable Function for Hardware Security

Adithyalal P M, Shankar Balachandran and Virendra Singh: A Soft Error Resilient Low Leakage SRAM Cell Design

Yuta Kimi, Go Matsukawa, Shuhei Yoshida, Shintaro Izumi, Hiroshi Kawaguchi and Masahiko Yoshimoto: Analysis of Soft Error Propagation considering Masking Effects on Re-convergent Path

Day 3 (25 Nov 2015 – Wednesday)

5A. Test and Diagnosis (10:30 am – 12:30 pm)

Session Chair: Seiji kajihara, Kyushu Institute of technology, Japan

Malav Shah, Industry Talk (Texas Instruments, India): Lowering Test Costs in Low Cost Microcontrollers

Tino Flenker, André Sülflow and Görschwin Fey: Diagnostic Tests and Diagnosis for Delay Faults using Path Segmentation

Srinivasa Shashank Nuthakki and Santanu Chattopadhyay: An Integrated Approach for Improving Compression and Diagnostic Properties of Test Sets

Michael Kochte, Atefe Dalirsani, Andrea Bernabei, Martin Omana, Cecilia Metra and Hans-Joachim Wunderlich: Intermittent and Transient Fault Diagnosis on Sparse Code Signatures

5B. Resilient System Design and Test (10:30 am – 12:30 pm)

Session Chair: Janak Patel, Univ. of Urbana-Champagne, USA

Yoichi Maeda, Industry Talk (Renesas System Design Japan): Application of the embedded power-on-self-test for automotive microcontroller based on ISO26262

Sukrat Gupta, Neel Gala, G. S. Madhusudan Desikan and Kamakoti Veezhinathan: SHAKTI-F: A Fault Tolerant Microprocessor Architecture

Swagata Mandal, Suman Sau, Amlan Chakrabarti, Sushanta Pal and Subhasish Chattopadhyay: FPGA Implementation of High Speed Latency Optimized Optical Communication System Based on Orthogonal Concatenated Code

V Prasanth, Rubin Parekhji and Amrutur Bharadwaj: Improved Methods for Accurate Safety Analysis of Real-life Systems

6A. Testing in FINFET and Emerging Technologies (1:30 pm – 3:30 pm)

Session Chair: Huawei Li, Chinese Academy of Sciences, China

Loganathan Lingappan, Industry Talk (Intel USA): Need for online test generation/manipulation/profiling at advanced process nodes

Kuan-Ying Chiang, Yu-Hao Ho, Yo-Wei Chen, Chien-Mo Li and Cheng-Sheng Pan: Fault Simulation and Test Pattern Generation for Cross-gate Defects in FinFET Circuits

Joyati Mondal, Debesh Kumar Das and Bhargab B. Bhattacharya: Design-for-Testability in Reversible Logic Circuits based on Bit-Swapping

Ashwin Chintaluri, Abhinav Parihar, Arijit Raychowdhury, Helia Naeimi and Suriyaprakash Natarajan: A Model Study of Defects and Faults in Embedded Spin Transfer Torque (STT) MRAM Arrays

6B. Design Analysis, Verification and Validation (1:30 pm – 3:30 pm)

Session Chair: Supratik Chakravarty, IIT Bombay, India

Masahiro Ishida, Toru Nakura, Akira Matsukawa, Rimon Ikeno and Kunihiro Asada: A Technique for Analyzing On-chip Power Supply Impedance

Payman Behnam and Bijan Alizade: In-circuit Mutation-based Automatic Correction of Certain Design Errors

Raphael Viera, Rodrigo Bastos, Jean-Max Dutertre, Olivier Potin, Marie-Lise Flottes, Giorgio Di Natale and Bruno Rouzeyre: Validation Of Single BBICS Architecture In Detecting Multiple Faults

Saikat Dutta, Soumi Chattopadhyay, Ansuman Banerjee and Pallab Dasgupta: A new approach for minimal environment construction for modular property verification

Keynotes:

1. Subhasish Mitra (Stanford University): The Next Big Thing in Test

2. Friedrich Hapke (Mentor Graphics): Cell Aware Test and Diagnosis

3. Harry Chen, Mediatek (Taiwan): Adaptive System-Level Test for High-Volume Mobile Phone Chips
4. Masahiro Fujita (University of Tokyo): Unified Logic Framework for Synthesis, Testing, and Diagnosis

(6 Industry talks embedded in program)

Panel:
Research Collaboration in Test and EDA –International Perspectives
Panelists: TBD