

Buck converter

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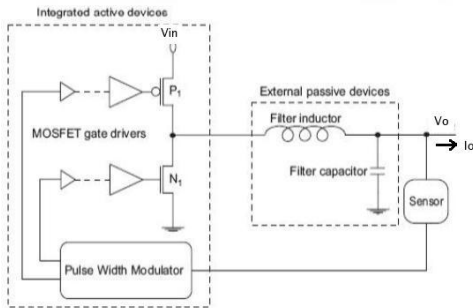
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DC-DC Converters

- DC to DC converter provides regulated output voltage level(s).
- They are used in battery powered applications like Cell phones, PDAs and Laptops etc.
- There are three main types of DC-DC converters namely switched capacitor converters or charge pumps as they are commonly called, Linear regulators and Switching converters or switchers.

	Charge Pumps	Linear Regulators	Switchers
SOC Feasibility	worst	better	worst
Output Power	Low	Low	High
PCB area	High	Lowest	highest
Efficiency	Good	Worst	Best

Block diagram of a Buck Converter



- Ideally, transfers energy from input to output in a lossless fashion.
- Choice of switching frequency and inductor are important with respect to efficiency.

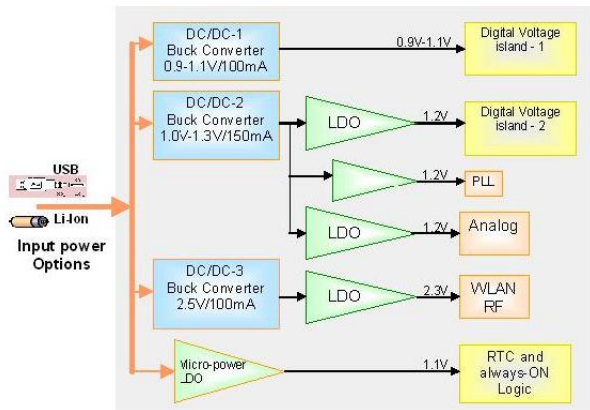


Figure: Typical Power on SoC⁰

⁰ Source : CosmicCircuits

Issues in power management

- Multiple voltage levels i.e power islanding
- Multiple clock frequencies
- Efficiency optimization
- Proper allocation of power based on noise tolerance
- Power sequencing

Important Issues in Buck Converter

- Efficiency and drive strength
- Effect of load variation on efficiency
- Effect of PVT on efficiency
- EMI
- PowerON transients

Different losses in Buck converter

- Load dependent conduction losses
 - Transistor on resistances
 - Diode forward voltage drop
 - Inductor winding resistance
 - Capacitor equivalent series resistance

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 - $F_{sw} \cdot CV^2$ loss
 - Reverse recovery loss

Different losses in Buck converter

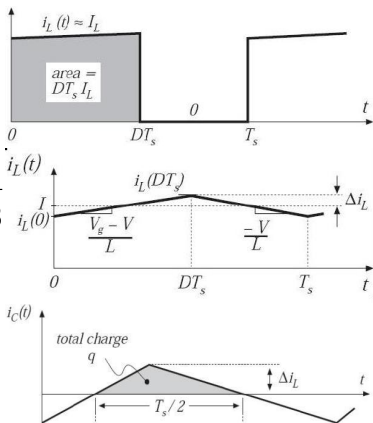
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- Gate drive loss and controller power.
- Fixed losses due to transistor leakage current and controller standby current

Sources of conduction loss in Buck Converter

- In PMOS $I_{RMS} = I_o \cdot \sqrt{d} \cdot \sqrt{1 + (\Delta I / I_o)^2 / 3}$
- In NMOS $I_{RMS} = I_o \cdot \sqrt{(1 - d)} \cdot \sqrt{1 + (\Delta I / I_o)^2 / 3}$
- In inductor $I_{RMS} = I_o \cdot \sqrt{1 + (\Delta I / I_o)^2 / 3}$
- In output capacitor $I_{RMS} = \Delta I^2 / \sqrt{3}$



Switching losses

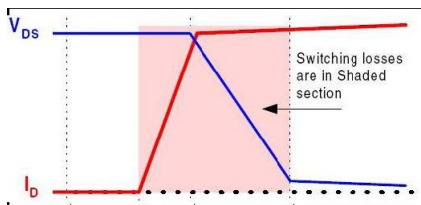


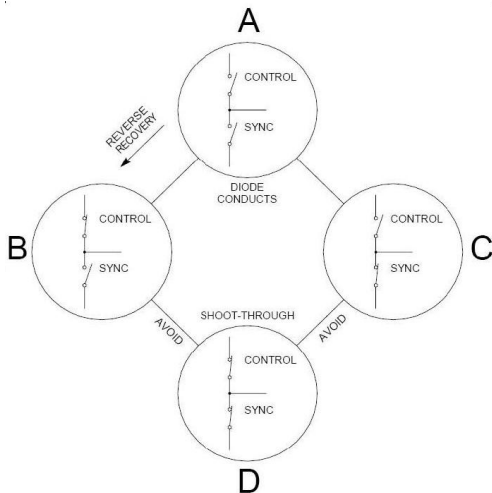
Figure: I-V overlap loss in a switch

- Comprise of I-V overlap losses in the switch and FCV^2 losses
- Directly proportional to F_{SW}
- Dominant at low load conditions

Reverse Recovery of Body diode

- Dead time is introduced to prevent current shoot through
- Dead time contributes to conduction losses in the body diode of NMOS switch
- Power dissipated due to reverse recovery:

$$P_{rr} = Q_{rr} \cdot F_{sw} \cdot V_{in}$$
- External Schottky diode can be used to alleviate the problem



Gate Drive Losses and Controller Power

- Power is also lost in charging and discharging of gate capacitors during switching
- Gate drive losses are considerable at low values of load current
- Some power is also dissipated in the controller

Introduction

Losses in Buck Converter

Loss Modeling in MATLAB

Comparison of Cadence and MATLAB results

Variation of Losses with V_{in}, I_o, W_n, W_p

Continuation of the work: Model-based design

Motivation for Loss modeling and related issues

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MOTIVATION

- Tradeoff between losses with respect to width of switching transistors, I_o , V_{in} and F_{sw}
- Inefficiency of circuit simulators
- Generating design information

Motivation for Loss modeling and related issues

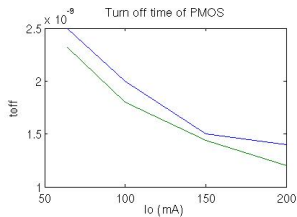
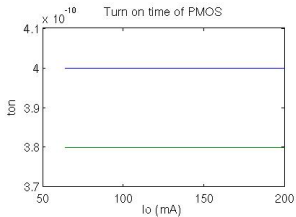
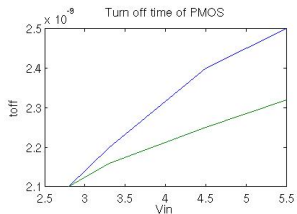
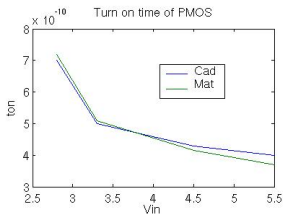
MOTIVATION

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ISSUES

- Modeling of the on resistance of switches
- Modeling of the loss due to reverse recovery charge of the body diode
- Modeling of the on/off time of MOS switches
- Modeling of the driver to estimate switching times

PMOS switching times



Comparison of Spectre and MATLAB results

Technology :0.35um MM TSMC process (I/O devices)

Aspect ratio : PMOS=45000 NMOS=22500

Conduction losses in MOSFETs at $I_o=100$ mA

V_{in}	Pcpm (mW)		Pcnm (mW)		Pbd (mW)	
	Cadence	MATLAB	Cadence	MATLAB	Cadence	MATLAB
3.3 V	10.5	12.5	4.36	4.4	2.14	2.4
5 V	1.75	1.6	1.47	1.4	1.12	1.3

Conduction losses in MOSFETs at $V_{in}=5V$

I_o	Pcpm (mW)		Pcnm (mW)		Pbd (mW)	
	Cadence	MATLAB	Cadence	MATLAB	Cadence	MATLAB
64 mA	0.8	0.98	0.7	0.74	0.82	0.84
100 mA	1.75	1.6	1.47	1.4	1.12	1.3

Comparison of Spectre and MATLAB results

Technology :0.35um MM TSMC process (I/O devices)

Aspect ratio : PMOS=45000 NMOS=22500

Losses at $I_o=100$ mA

V_{in}	Ponp (mW)		Poffp (mW)		Prr in Body diode (mW)	
	Spectre	MATLAB	Spectre	MATLAB	Spectre	MATLAB
3.3 V	0.24	0.26	.21	0.23	0.075	0.08
5 V	0.3	0.28	0.34	0.42	0.121	0.125

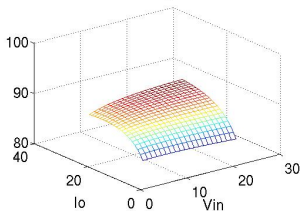
Losses at $V_{in}=5V$

I_o	Ponp (mW)		Poffp (mW)		Prr in Body diode (mW)	
	Spectre	MATLAB	Spectre	MATLAB	Spectre	MATLAB
100 mA	0.3	0.28	0.34	0.42	0.121	0.125
64 mA	0.28	0.25	0.32	0.33	0.125	0.125

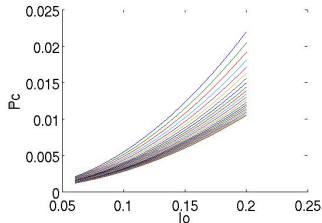
Losses scale with V_{in} and I_o (more sensitive to V_{in}).

Loss variation with I_o and V_{in}

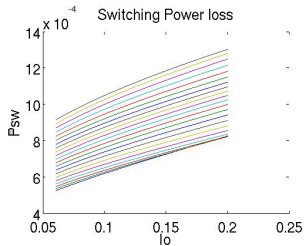
Estimation of efficiency of buck converter



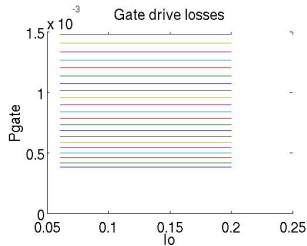
Conduction Power loss



Switching Power loss

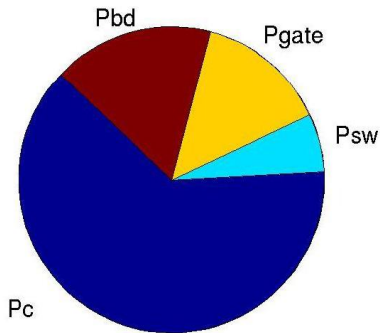


Gate drive losses

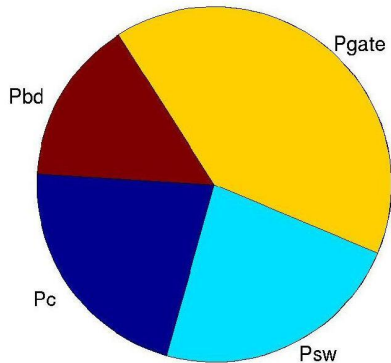


Breakup of losses at high and low load conditions

Generated from loss model developed in MATLAB



At high load

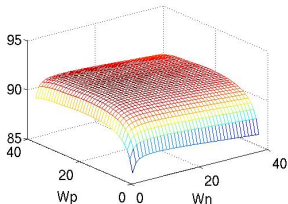


At low load

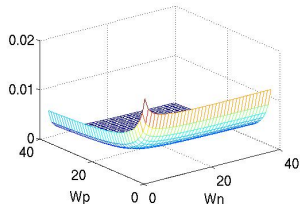
Variation of Efficiency with transistor widths

$V_{in} = 3V$ and $I_o = 100mA$

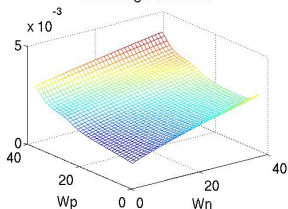
Estimation of efficiency of buck converter



Conduction Power loss



Switching Power loss



Continuation of the work: Model-based design

- Design objective is "optimum efficiency".
- Modeling provides the design data for optimizing efficiency.
- Next stage aims at design of driver and controller to maximize efficiency.
- Process variations will be taken into account (effect?).