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ACTIVE ANTENNA INVOLVING WIDE BAND AMPLIFIER FOR VHF AND UHF RANGE

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Abstract

An active antenna includes electronics to optimise the performance of the antenna. An important feature of many types of active antenna is to allow efficient operation across a broad frequency range, and to provide a low noise amplifier for weak signals. The low noise amplifier in an active antenna is mounted with the antenna itself to minimise the impact of interfering signals. Unlike other types of antenna, an active antenna requires its own power supply. While the terminology of active antenna means that the active device are employed in the passive antenna elements to improve antenna performance, the terminology of active integrated antennas indicated more specifically that the passive antenna elements and the active circuitry are integrated on the same substrate. To provide a better impedance matching and prevent loading of an amplifier, a double stage amplifier circuit is considered.

The objective is to design an active antenna involving wide band amplifier. The circuit has been designed to amplify the signals received from the antenna over a band width of 30 MHz to 3 GHz.

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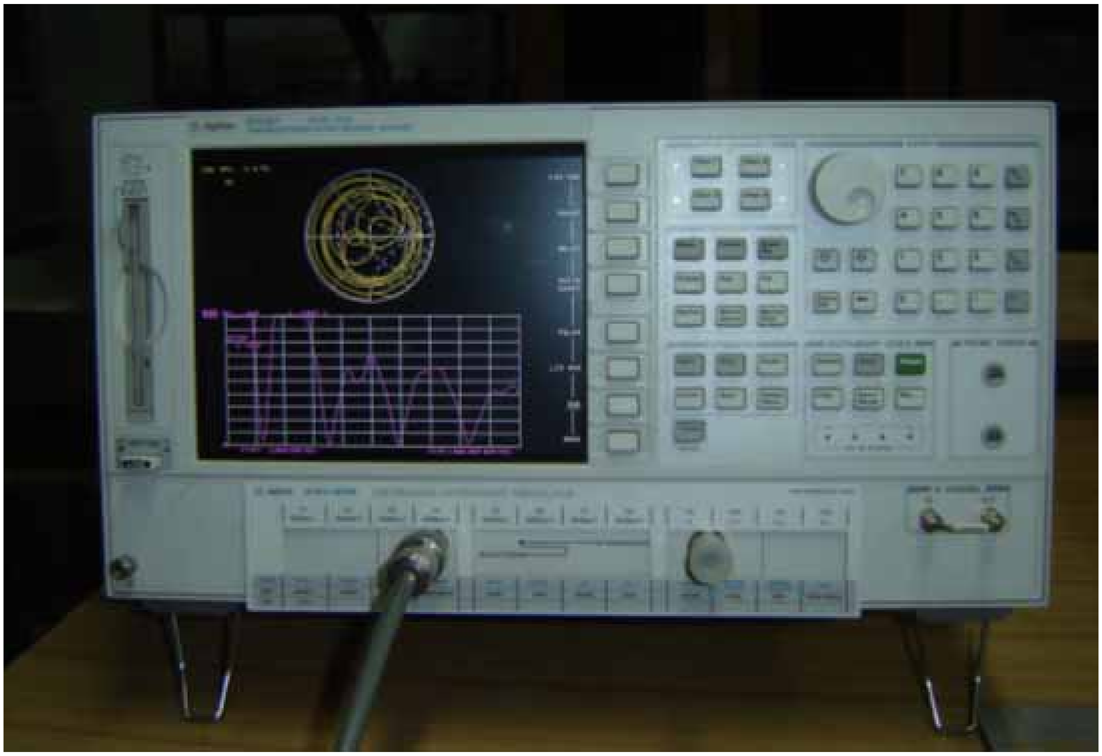
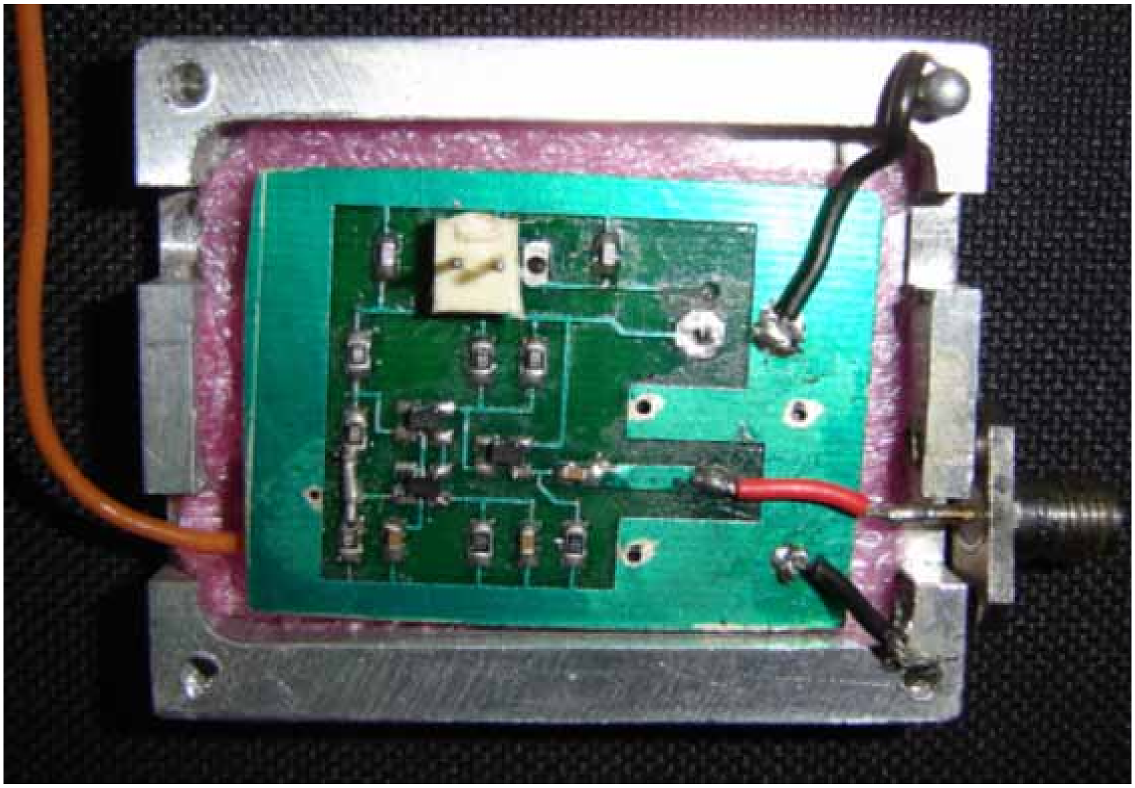


Photograph 1. The photograph of the Network Analyzer used.

Photograph 2. The photograph of the Spectrum Analyzer (left) and the Signal generator (right) used



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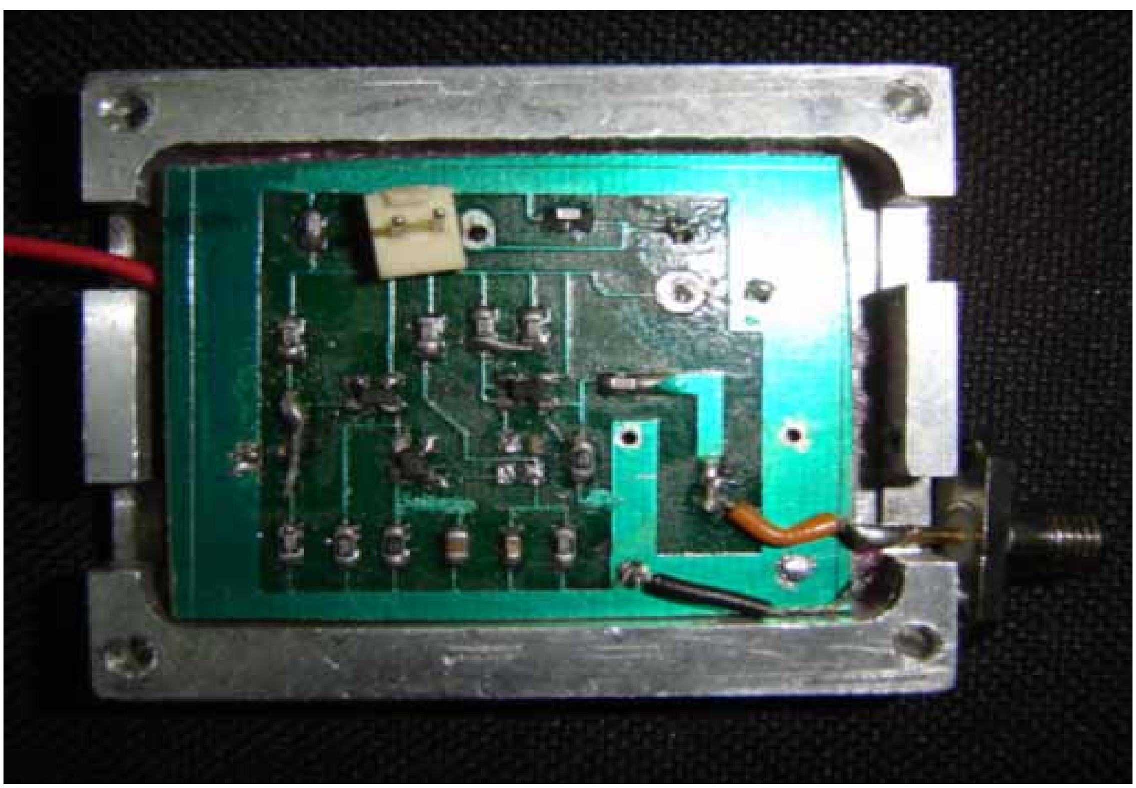

Photograph 4. The photograph of the circuit in the range of 1MHz to 1 GHz (Actual dimension of the box is 4.5 cm X 5cm)

1. Introduction

1.1 Antenna

1.1.1 Dipole antenna

A linear dipole antenna is simply a piece of wire of length (say 2H) excited by a voltage or current source at its center (as shown in the Figure1.). The gap at the center of the dipole is assumed to be small. The current spreads on the length of the dipole and attains a steady state distribution and is symmetric about the center. At the ends of the antenna since there is no path for the current to flow, the current at the end points is zero.

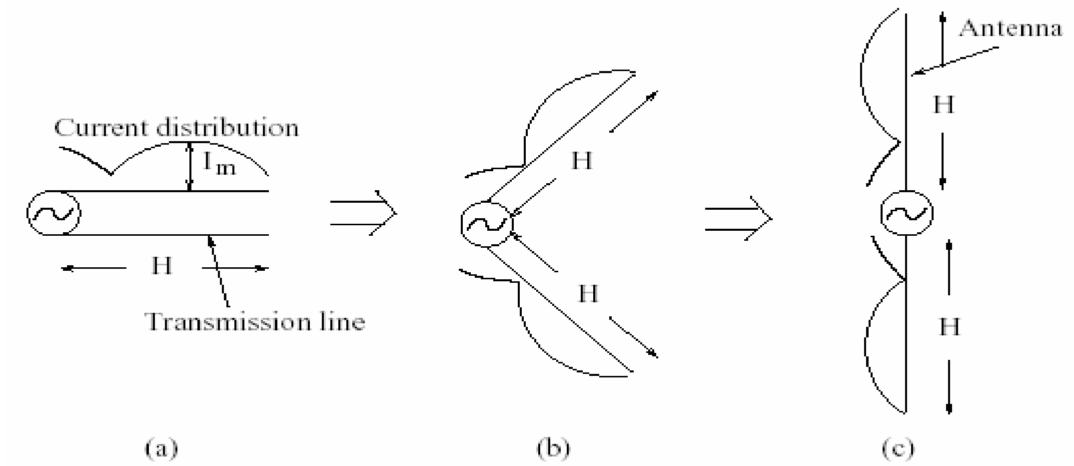

Figure 1. An overview of a dipole antenna

Most of the time we deal with half wave dipoles. For a particular wavelength each side of the half wave dipole will be ¼ of the wavelength of the receiving or transmitting signal.

Thus, Wavelength (metres) = 300 / frequency (MHz)

$$\text{Half side length of the antenna} = \frac{\text{Wavelength}}{4}$$

Any antenna which is a multiple of ¼ of the physical wavelength is a resonant antenna. Currents and voltages will occur along the length of the dipole antenna and their distribution is as shown in Figure2.

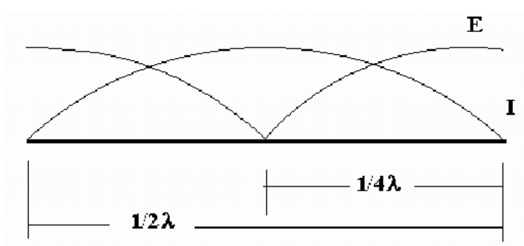

Figure 2. Current and voltage distribution on an antenna

1.1.2 Monopole Antenna

The radiation characteristics of a monopole antenna are identical to that of a dipole antenna of double length except the power radiated by the monopole is half of that of the corresponding dipole of the same length. Since the power can be controlled by the exciting current a monopole antenna can appropriately replace a dipole antenna.

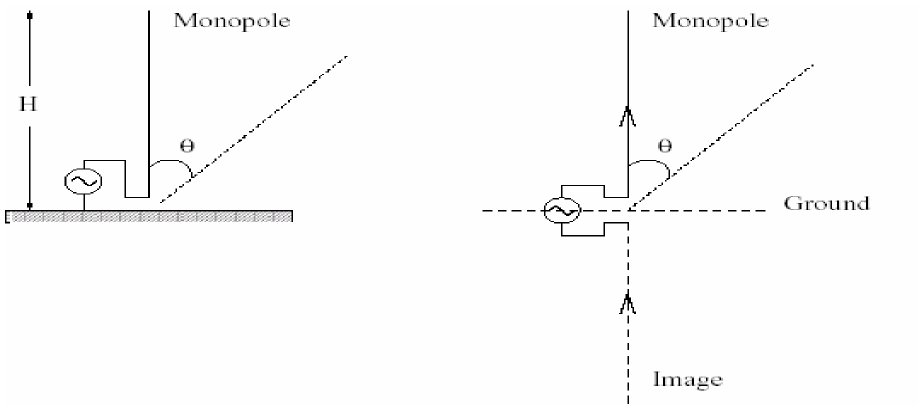

Figure 3. A monopole antenna

For a monopole antenna the ground plane is equivalent to having an image of it below the ground surface. For every charge above the conduction ground, an image charge of opposite sign is produced. The charges and currents and their image is as shown in Figure4.

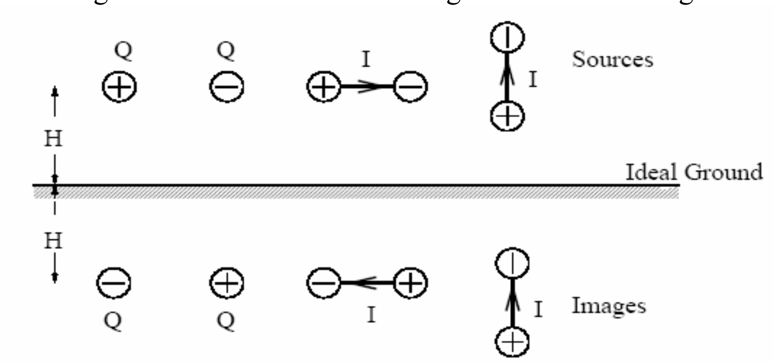

Figure 4. The image at the ground plane

Thus from Figure4 above it is clear that for a vertical current element having upward current, the image current is also in the upward direction. Now since the monopole is resemble of vertical current elements, the image will have current flowing in the same direction as that of the monopole. The current distribution on a monopole and its image is then identical to a dipole of length 2H. Since the radiation pattern is uniquely related to the current distribution, a monopole and dipole have exactly identical radiation patterns.

1.2 Impedance matching

A receiving antenna can be approximated as a voltage source with some internal impedance. The impedance of a short monopole antenna is capacitive with small resistive component.

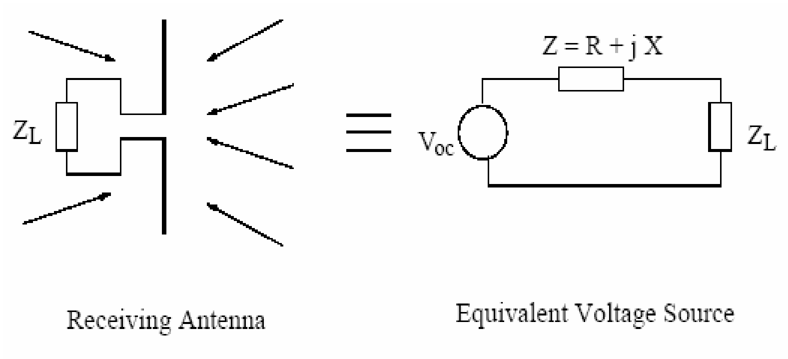

Figure 5. Antenna as equivalent voltage source

The capacitance, C_a of a single monopole antenna is given by

$$C_a = \frac{24.2\ h}{\log(2h/a) - 0.7353} \quad \text{.......................................} (1)$$

where,
C_a = Capacitance of the antenna in pF
a = Diameter of the antenna
h = Height of the monopole antenna

and the radiation resistance, R_r is given by,

$$R_r = 40\ \pi^2 (h/\lambda)^2 \quad \text{..} (2)$$

For an antenna with fixed height and diameter we get the value of radiation capacitance as constant and the radiation resistance as a function of frequency.

The capacitance normally varies from 12 pF to 20 pF. For a small monopole antenna of height 1m and diameter 5mm, the capacitance as calculated from equation (1) is 12.963 pF. At high frequencies the capacitive reactance increases and when the antenna is connected to the receiver through a cable, the signal gets grounded due to the 50 ohm loading and is lost. Hence there need to be some kind of impedance matching to prevent the signal from getting lost and transmitting it to the receiver. This impedance matching makes an antenna active.

1.3 Bandwidth of impedance matching and Efficiency

There are limitations on the bandwidth of impedance matching between a resonant circuit (antenna) and generator or load. The bandwidth of matching within any specified tolerance of reflection is proportional to the resonance bandwidth of the resonant circuit. A small bandwidth is logically expressed in terms of the radiation resistance to its reactance. The input impedance of antenna may be capacitive or inductive, and to make it a resonant configuration a reactance of the opposite kind may be placed. The dissipation (other than radiation) is ignored.

Radiation Efficiency is given by,

$$\eta = \frac{\text{Radiation resistance}}{(\text{Radiation resistance} + \text{Loss power factor})} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

$$= \frac{R_r}{(R_L + R_r)}$$

We know that for a short dipole, the radiation resistance is given by,

$R_r = 200\, l_\lambda$ (ohm)

If

$l_\lambda = 0.1$, then $R_r = 2$ ohm, and if,

$l_\lambda = 0.01$, then $R_r = 0.2$ ohm

With such low values of radiation resistance it is apparent that even small values of loss resistance can result is low radiation efficiency. To increase the radiation efficiency requires an increase in the radiation resistance or a decrease in loss resistance R_L or both. The loss resistance involves losses in the ground system, antenna insulators, turning coils, conductors (including the tower itself) and corona.

The figure of merit for an electrically small antenna is

$$\frac{\text{Radiated power}}{\text{Reactive power}} = \frac{\text{Radiation resistance}}{\text{Reactance}} = \frac{R_r}{X} << 1 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

This is not the same as 1/Q since

$$Q = \frac{\text{Energy stored per unit time}}{\text{Energy lost per unit time}} = \frac{X}{R_r + R_L} = \frac{\text{Centre frequency}}{\text{Bandwidth}} \quad \ldots\ldots\ldots (5)$$

Thus, increasing either R_r or R_L, or both, reduces Q and broadens the bandwidth. However, only an increase in R_r decreases efficiency. The radiation power factor, PF for a small antenna is equal to the ration of the antenna volume to a radiansphere.

$$\text{Power Factor, PF} = \frac{\text{Antenna volume}}{\text{Radiansphere}} = \frac{(4/3)\,\pi\, r^3}{(4/3)\,\pi\,(\lambda/2\,\pi)^3} \ldots\ldots\ldots\ldots\ldots\ldots (6)$$

According to equation (6) , the power factor or figure of merit of a small antenna varies as the cube of its dimension. If RL = 0 in equation (5), we have from equation (4) and equation (6) that

$$Q = 1/\,(2\pi r_\lambda)^3 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (7)$$

Thus, and electrically small lossless antenna ($(2\pi r_\lambda)^3 << 1$) has inherently high Q and narrow bandwidth. We note from equation that losses decrease Q and increases bandwidth. Hence it can be appreciated that if RL is higher in a small antenna, it will exhibit a higher bandwidth but poor efficiency.

1.4 Gain

Gain also is an important parameter. Theoretically, the smallest antenna that could be designed is a point, i.e. an isotropic antenna. Say this receives energy from the electromagnetic spectrum equivalent to 0 dBm. An ordinary half-wave dipole antenna receives 2.5 dBm (or 1.6 times) more energy than an isotropic antenna. For a small active antenna, this gives 1.76 dB more than an isotropic antenna, or 1.5 times the energy. The difference between the standard and small active antenna elements is therefore just 0.39 dB, insignificant in fact. Unlike a small antenna, a large aerial can be directly matched to a 50 ohm cable, which is why an active antenna uses an electrical solution to change the impedance. Most active antennas have some form of amplification with their impedance matching unit. The active antenna itself may take many forms such as a miniature dipole, a loop, or some type of whip. But there are some disadvantages in using an active antenna.

1.5 Miller Effect

At high frequencies the parasitic capacitance, C_μ starts providing feedback between base and collector of the BJT. The Miller Theorem provides the means for replacing this bridging capacitance into two grounded capacitances, one between the base and ground and the other between collector and ground.

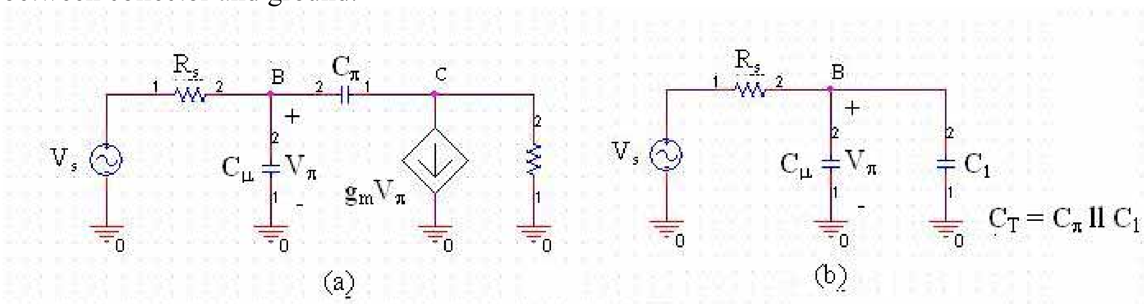

Figure 6. (a) High frequency model of BJT (b) Equivalent Miller Capacitance

Where $C_1 = C_\mu(1 - K)$,

K is the gain of the circuit,

C_μ is the parasitic capacitance.

Consider $K = -100$ V/V and $C_\mu = 1$pF

or, $C_1 = 1[1 - (-100)] = 101$pF

Thus the input capacitance between the base and ground increases, which limits the high frequency response of the transistor. From the figure 6(b) above, the upper 3 dB frequency is given by,

$$\omega_H = \frac{1}{C_T R_S} \quad \text{...(8)}$$

Thus for high upper cut off frequency, $C_T R_S$ should be small.

R_S is the source resistance and changing R_S might not always be possible and hence we need to consider C_T . Thus for designing a wide band amplifier one has to consider the circuit configuration which does not suffer from Miller multiplication effect such as cascode configuration, cascade of Common Collector and Common Emitter (CC-CE) and Emitter follower etc.

1.6 Design criteria and options

We need an impedance matching and also an amplifier which has a sufficiently low noise figure that it will amplify the signal without introducing significant noise. It will have sufficiently high input impedance so that the signal does not get lost due to loading (50 ohm characteristic impedance of the cable). The output impedance should be similarly low as to comfortably drive a coaxial cable with a receiver attached.

Thus we are to design a wide band amplifier which takes input from the antenna end and after amplifying it feeds to the coaxial cable connected to the receiver.
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The design criteria of the amplifier are:-

1. High input impedance
2. Low output impedance
3. Reasonable gain
4. Less Miller multiplication effect
5. Less number of stages
6. Cost effective

1.6.1 Design propositions

i. ***Differential amplifier at the input stage:*** The differential amplifier configuration, because of its high input impedance and high gain can be used at the input stage. However it suffers DC imbalance due to absence of base resistance (R_{B2}) in the common base transistor (Q_2). The collector resistance (R_{C1}) in the common collector transistor (Q_1) forms a low pass filter with the Miller capacitance($C\mu$) of Q_1 which results in poor frequency response

The above imperfections can be met by substituting differential amplifier by common emitter amplifier. However the gain in the common emitter amplifier is half of the gain in the Differential amplifier configuration.

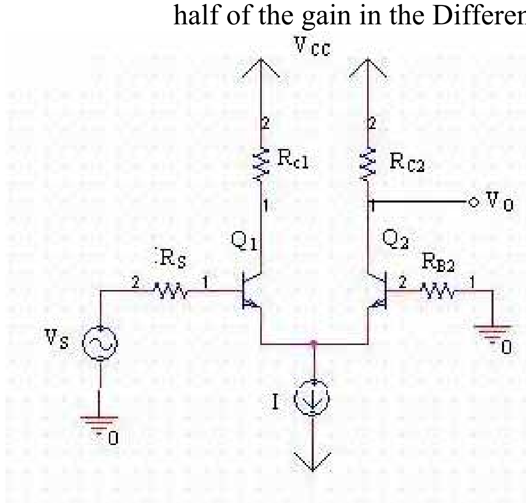

Figure 7 Differential amplifier forming low pass filter

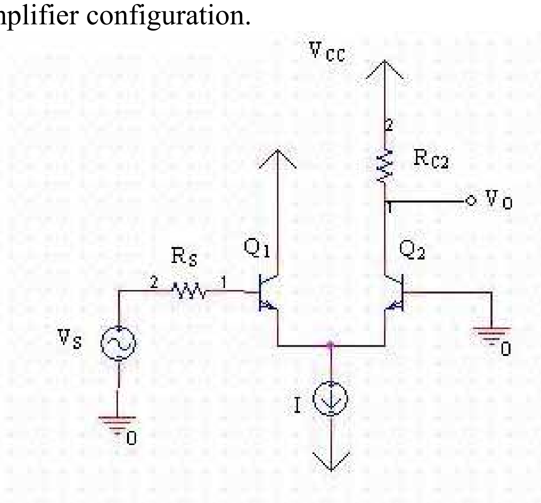

Figure 8 Differential amplifier having good frequency response but DC Imbalance

ii. ***Cascode amplifier configuration:*** The cascode amplifier consists of common emitter stage (Q1) followed by common base stage (Q2). The transistor Q1 provides a relatively high input resistance to the signal source. Cascode configuration can be used as an intermediate stage to provide substantial voltage gain with excellent high frequency response because the transistor Q2 (CB) does not suffer from “The Miller Effect”. The load resistance seen by Q1 is the input resistance (r_e) of Q2. This low load resistance of Q1 considerably reduces the Miller multiplier effect of capacitor $C\mu$ and thus extends the upper cut off frequency (ω_H). This is achieved without reducing the mid band gain (A_v) because the collector of Q2 carries a current almost equal to the collector of Q1.

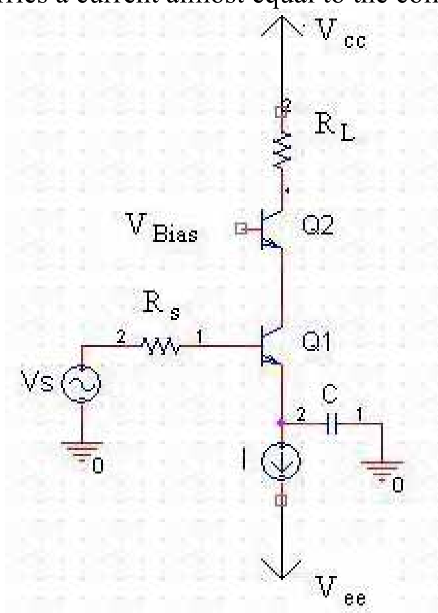

Figure 9 Cascode configuration

iii. ***MOSFET at the input stage:*** Since MOSFET have high input impedance, they can be used at the input stage. However it can be substituted to BJT because of low noise generation in the circuit, but the gain due to MOSFET is less than the gain due to BJT.

iv. ***Common collector amplifier at the output stage:*** The common collector exhibits a high input resistance, low output resistance, a voltage gain that is smaller than but close to unity and a relatively large current gain. Therefore it is ideally suited for applications in which high resistance source is to be connected to a low resistance load.

2. Design of the circuit

2.1 The circuit design of the amplifier in 30 MHz to 3 GHz

2.1.1 Stages of the circuit

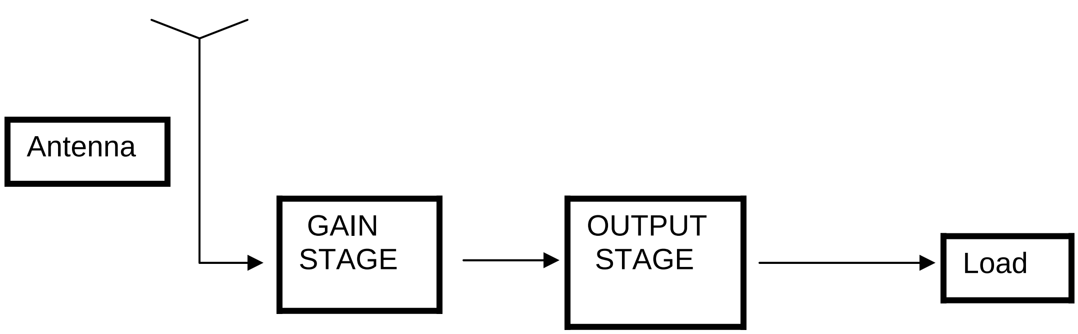

Figure 10. Block diagram of the circuit

The design consists of 2 stages.

1. Gain stage
2. Output stage

2.1.2 Gain stage

The gain stage which we have chosen consists of cascode amplifier configuration. As discussed in 1.5.1 (ii) there is no Miller effect in the common base configuration of the cascade amplifier configuration and gain is achieved without sacrificing the mid band gain. As required at the antenna end the cascode amplifier configuration has high input impedance. The gain of the amplifier amplifies the signal by a considerable amount. The amplification of the signal we get at this stage is the overall amplification of the circuit. The output impedance of the cascode configuration is very high and to match it we cascade it with a common collector amplifier which has high input resistance and low output resistance.

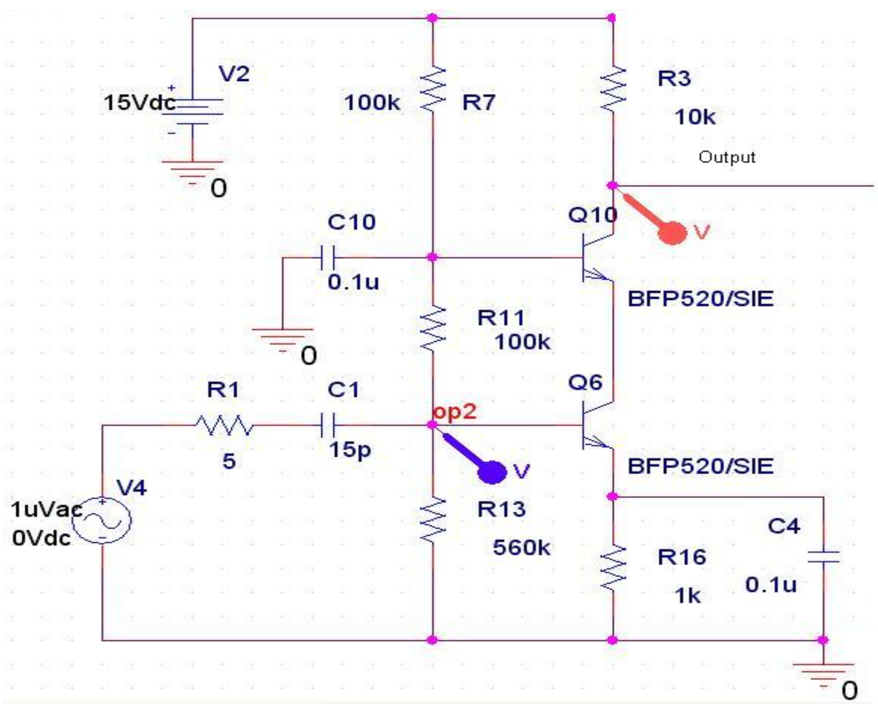

Figure 11 Cascode amplifier as applied in our circuit

2.1.3 Output stage

The output stage consists of common collector amplifier. The main purpose of this stage is to match the output impedance of the gain stage with that of the load line. The common collector amplifier has high input impedance, large current gain, low output impedance and no voltage gain. Hence it is able to match the amplified signal from the gain stage to the 50 ohm cable connected to the receiver. The bandwidth extension is further achieved from the shunt feebback and also results in the reduced output resistance.

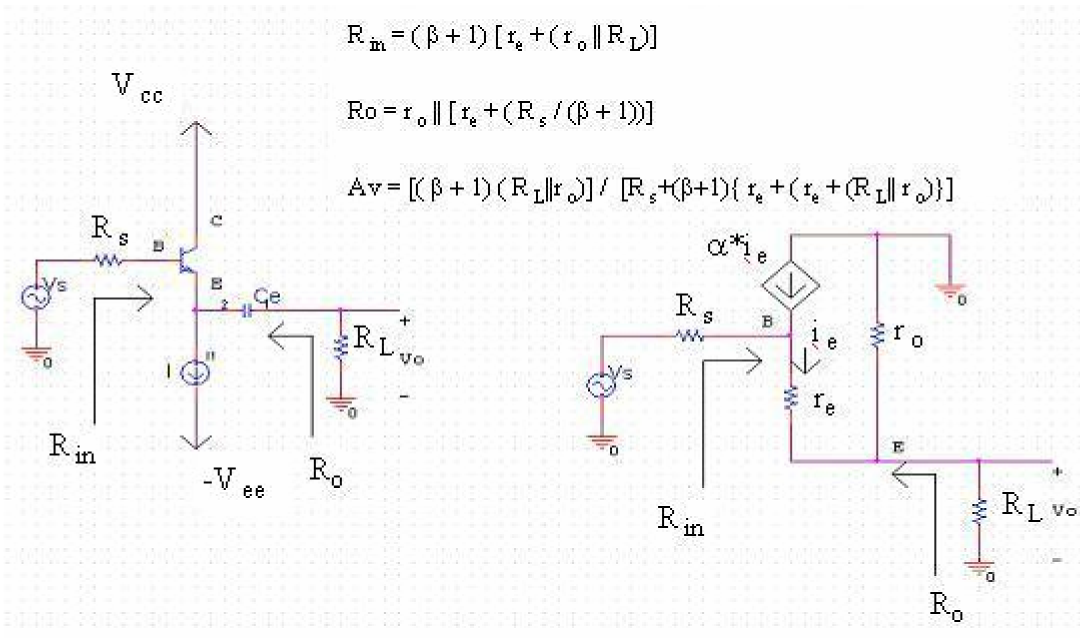

Figure 12 Common Collector amplifier

2.1.4 The final circuit

The final circuit is cascade of cascode amplifier and common collector amplifier. In order to get better high frequency response the common collector amplifier is used in feedback configuration.

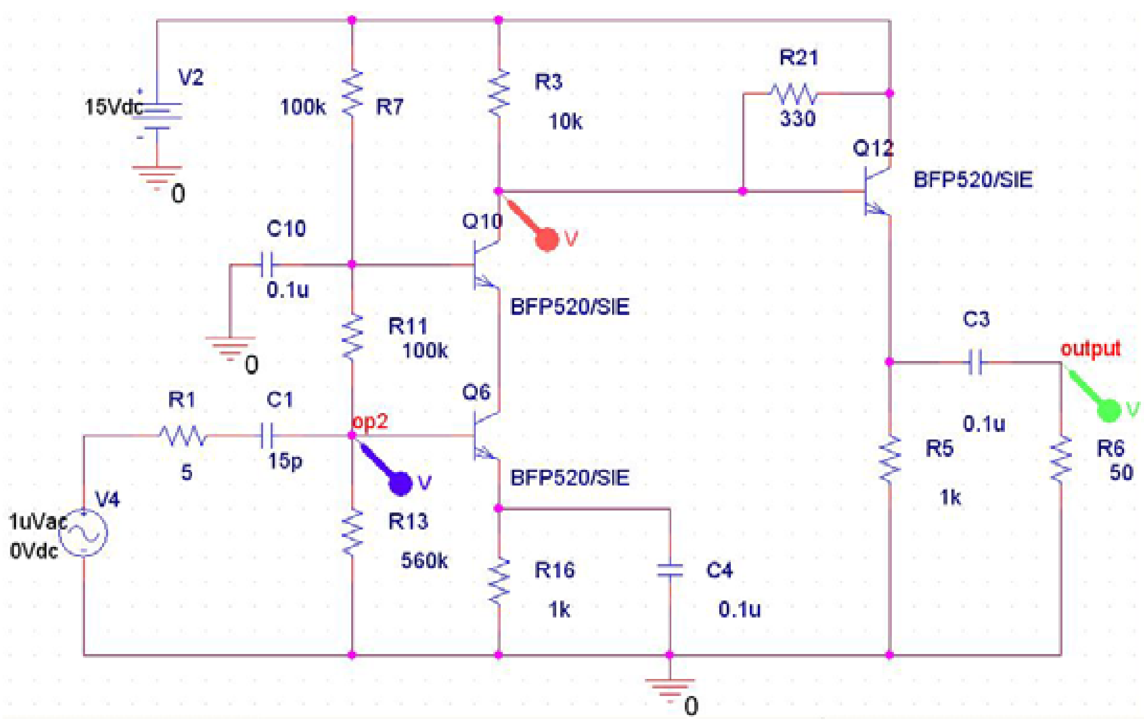

Figure 13 The final circuit

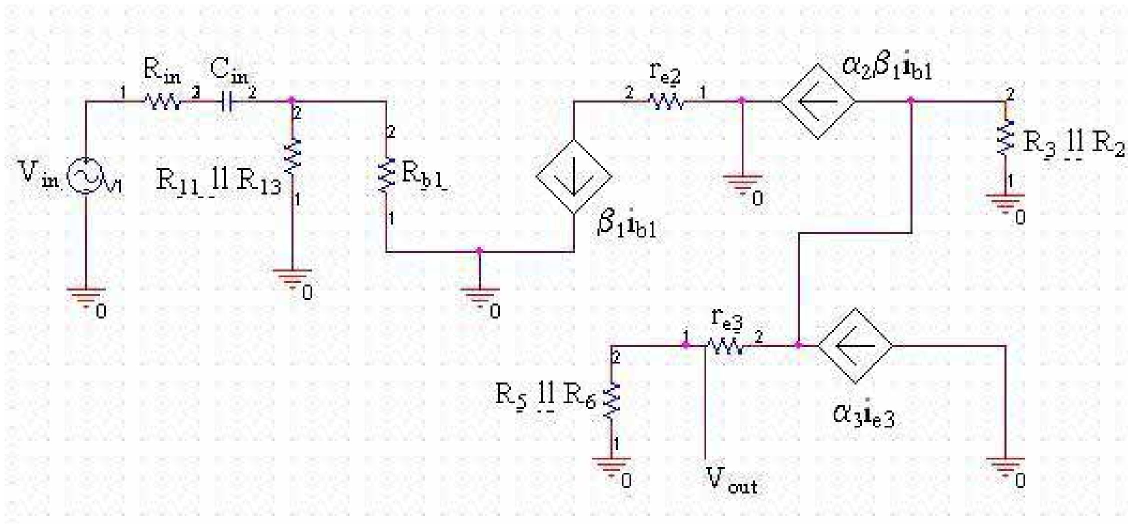

Figure 14. Small signal model of the final circuit

2.1.5 Circuit analysis

$$\text{gain} = \frac{(R_5 \parallel R_6)\alpha_2\beta_1\left(\frac{1}{R_{B_1}}\right)}{\left(\frac{r_{e_3} + (R_5 \parallel R_6)}{R_3 \parallel R_{21}}\right) - \left(\frac{1}{\beta_3 + 1}\right)}$$

$r_{e_3} = 2\ \Omega$, $\beta_3 = \beta_1 = 141.7$ and $\alpha_2 = 0.99$.

Therefore, $\text{gain} = 58$

$$\omega_L = \sum \frac{1}{C_i R_{is}}$$

Where,

C_i is the ith capacitane and,

R_{is} is the equivilant resistance across the ith capacitane considering the other capacitors as short circuit

$C_i = C_3 = 0.1\mu F$

$$R_{is} = \left(\left[\frac{R_3 \parallel R_{21}}{(\beta+1)} + r_{e_3}\right] \parallel R_5\right) + R_6$$

or $f_L = 5.42 MHz$

$$\omega_H = \frac{1}{\sum C_i R_{io}}$$

Where,

C_i is the ith capacitance and,

R_{io} is the equivilant resistance across the ith caparitor considering the other capacitors as open circuit.

$$\omega_H = \frac{1}{\sum\left(C_{be_i}(\beta+1)r_{e_i}\right)}$$

$$= 2\,\text{GHz}$$

Where,

C_{be_i} is the parasatic capacitance across the base and emiiter of ith transistor and,

r_{e_i} is the small signal emitter resistance of the ith transistor.

$C_{be_i} = 0.35\,\text{pF}$,

$r_{e_1} = r_{e_2} = 5\,\Omega$

$r_{e_3} = 2\,\Omega$

2.1.6 The input and output resistance of the circuit

The input and output resistance of the circuit as simulated on spice are as follows:

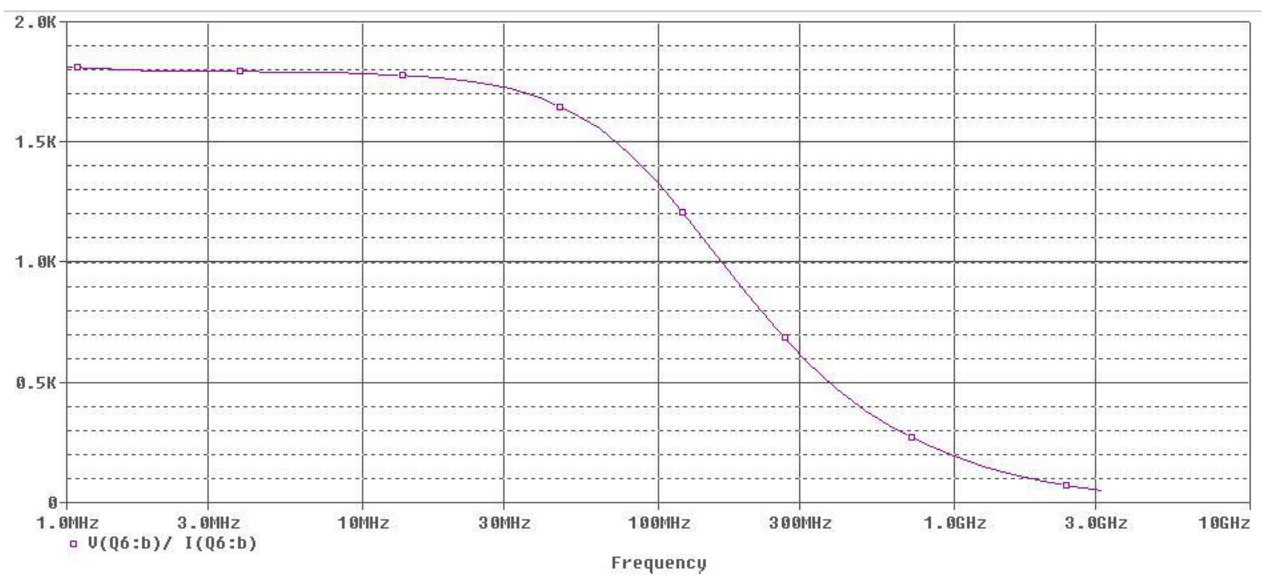

Figure 15. The input resistance of the circuit.

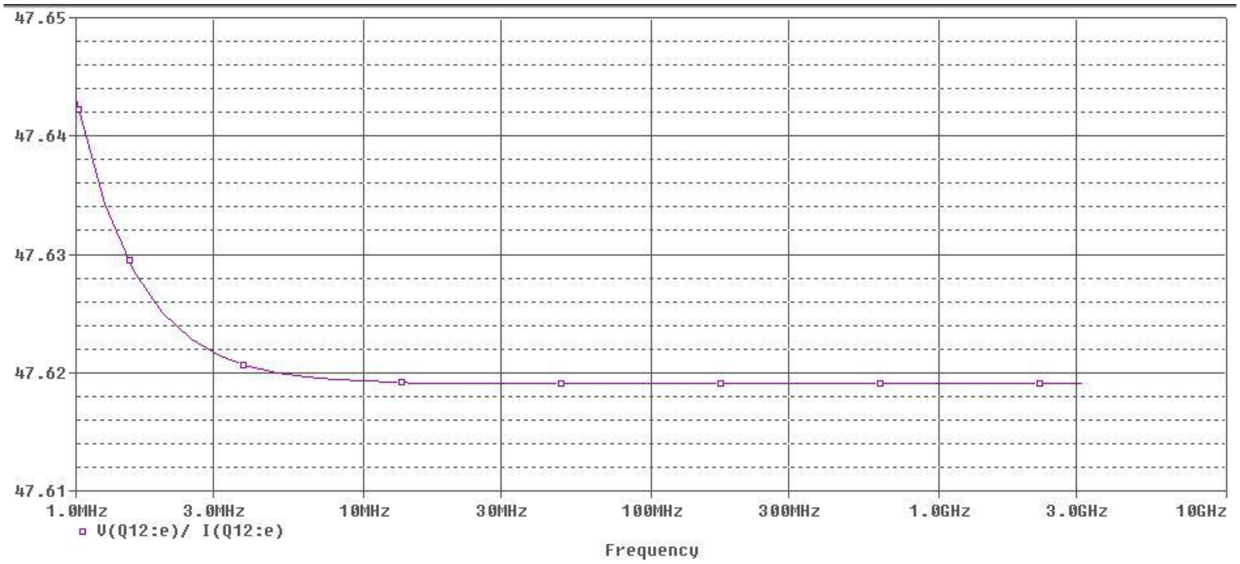

Figure 16. The output resistance of the circuit.

2.1.7 The PCB Layout

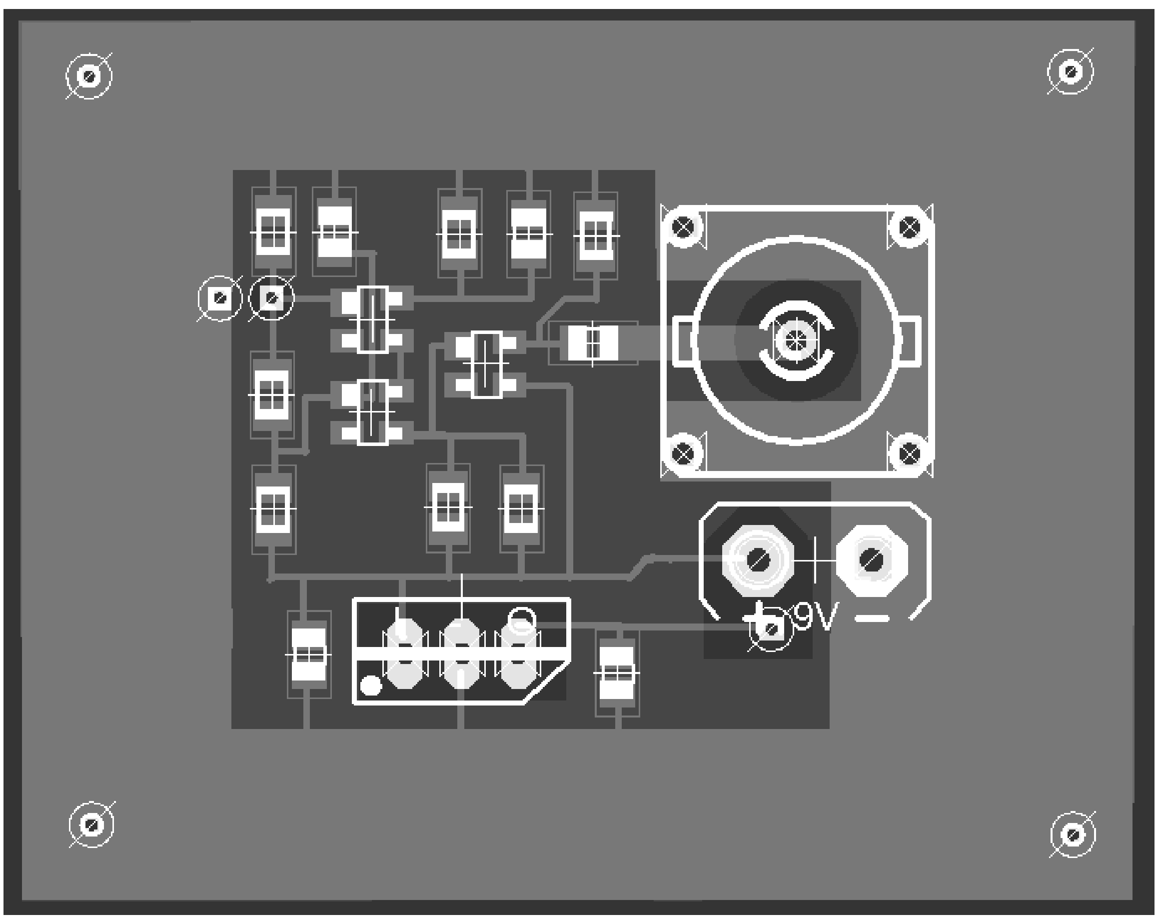

Figure 17 The PCB Layout of the final circuit. Actual size of the PCB is 3.5cm x 4.5cm.

2.2 The circuit design of the amplifier in 1 MHz to 1 GHz

2.2.1 Stages of the circuit

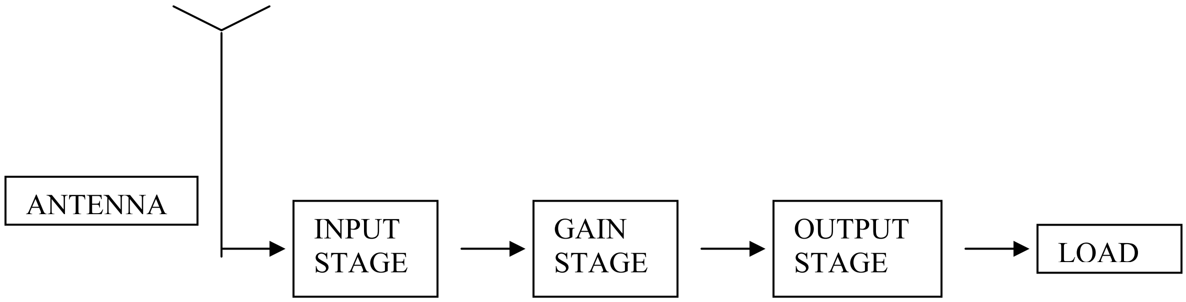

Figure 18. Block diagram of the circuit

The design consists of 3 stages.

1. Input stage
2. Gain stage
3. Output stage

2.2.2 Input stage

It is implemented by a Common collector amplifier to provide a high input impedance and current gain. The transistor Q1 in the input stage does not suffer from Miller multiplication effect and hence gives excellent high frequency response.

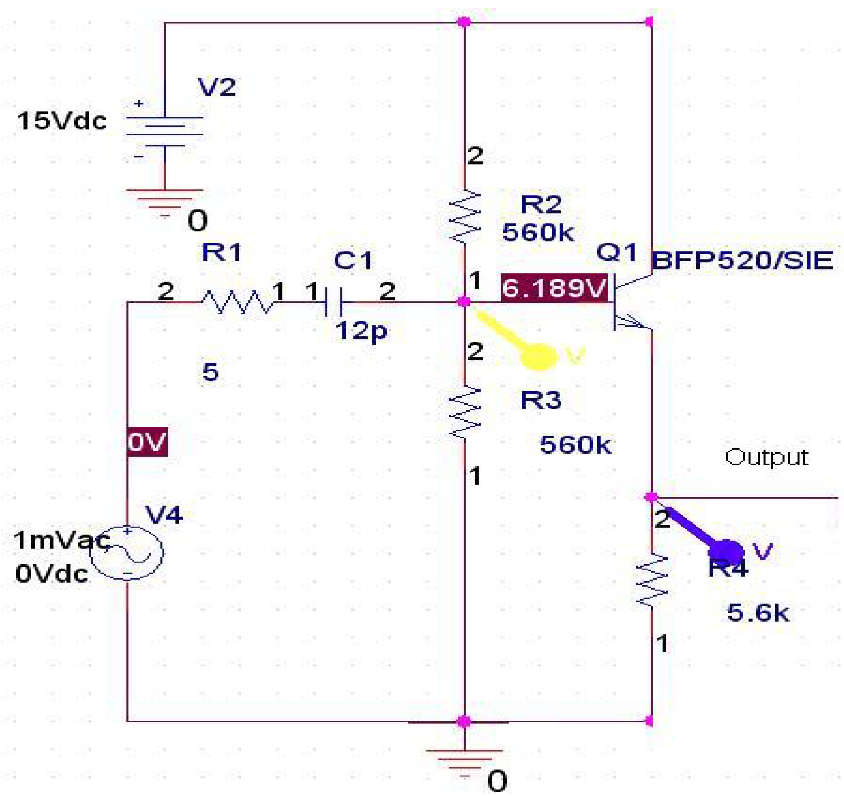

Figure 19. Common collector amplifier being used in the input stage.

2.2.3 Gain stage

The overall gain of the circuit is provided by the common emitter transistor Q2, (shown in figure 18). The transistors Q1 and Q3 minimize the Miller multiplication effect of transistor Q2. Transistors Q1 and Q2 are in Common Collector Common Emitter (CC-CE) cascade configuration and Q2 and Q3 are in Cascode configuration.

In CC-CE configuration due to absence of Miller multiplication effect transistor Q1 provides high frequency response while transistor Q2 provides the gain. The transistor Q2 suffers from Miller multiplication effect and the total effective capacitance between its base and ground is large, but because of low output resistance of the emitter follower Q1 the resistance seen by Q2 is small which increases the frequency response of Q2. (refer equation (8)).

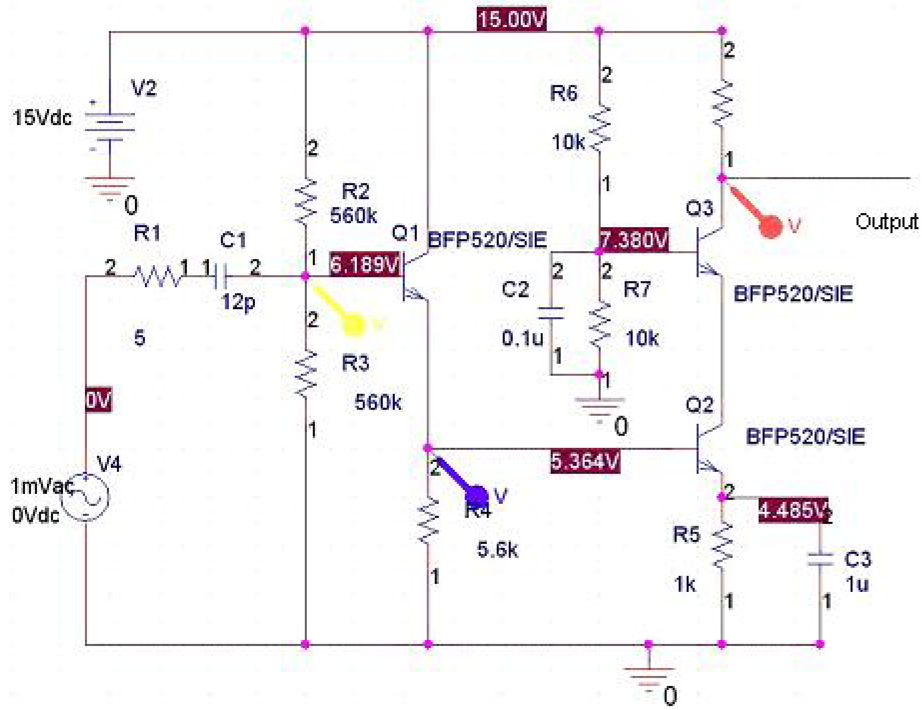

Figure 20. Gain stage

2.2.4 Output stage

It was implemented by a common collector amplifier it has low output resistance because it is required to match low impedance load. The feedback resistance R9 provides the bandwidth extension and also results in reduced output resistance.

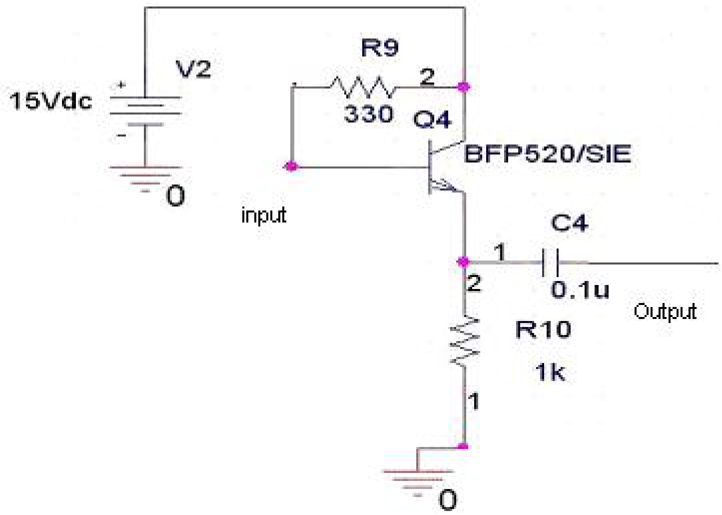

Figure 21. The common collector amplifier implemented as the output stage.

2.2.5 The final circuit

The final circuit is the cascade of the above three stages connected one after another. The impedance matching between the circuits have been taken care of due to "high output resistance and high input resistance" or "low output resistance and low input resistance" with respect to two stages at a given junction.

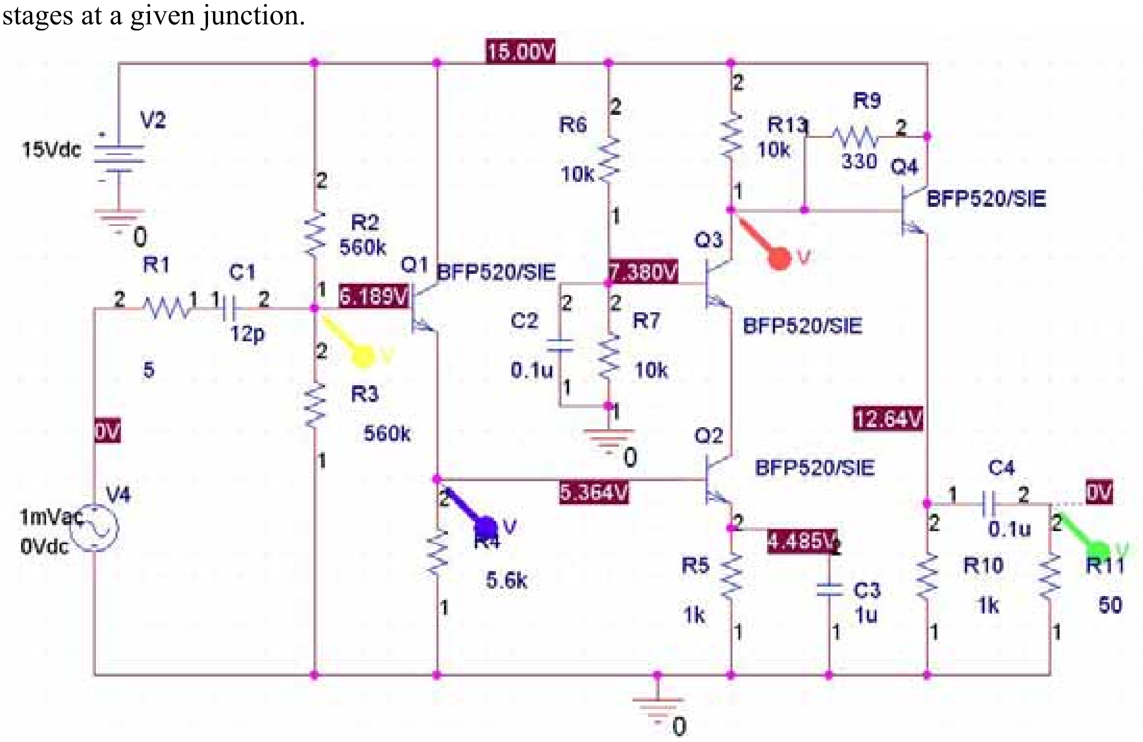

Figure 22 The final circuit.

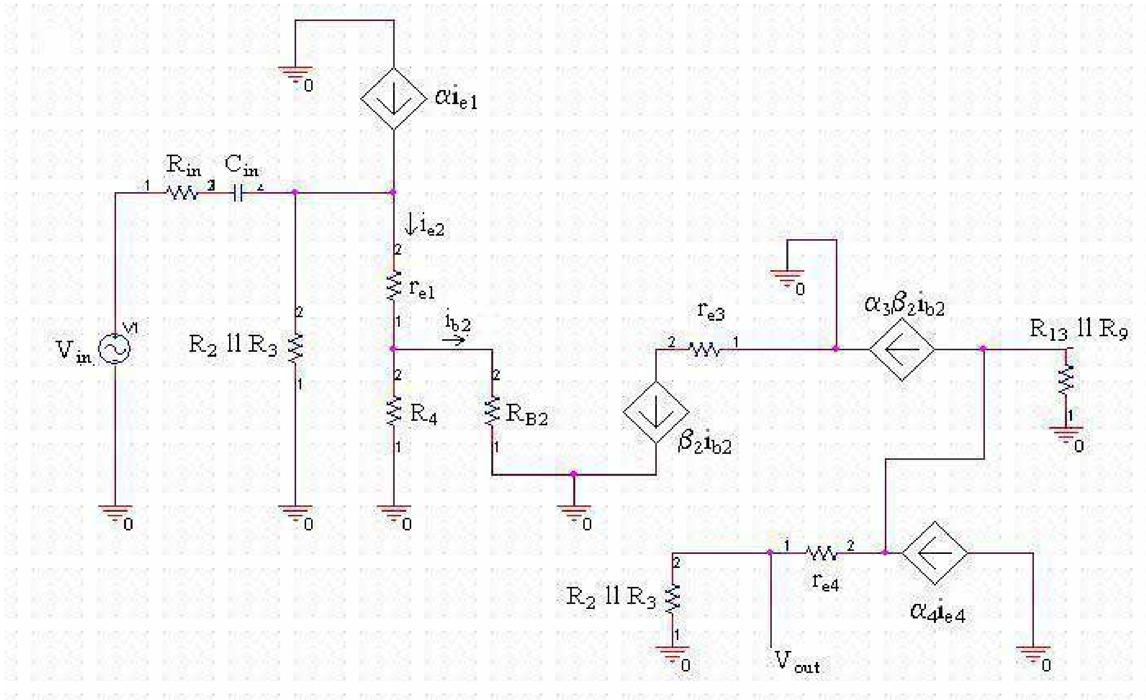

Figure 23. The small signal model of the final circuit.

2.2.6 Circuit analysis

$$\text{gain} = \frac{(R_{10} \| R_{11})}{\left(\dfrac{r_{e_4} + (R_{10} \| R_{11})}{R_{13} \| R_9}\right) - \left(\dfrac{1}{\beta_4 + 1}\right)} \alpha_3 \beta_2 \frac{(R_4 \| R_{B_2})}{\left(r_{e_1} + (R_4 \| R_{B_2})\right) R_{B_2}}$$

$\alpha_3 = 0.99,\ \beta_2 = \beta_4 = 139,\ R_{B_2} = 772\,\Omega,\ r_{e_1} = 25\,\Omega$ and $r_{e_4} = 1.99\ \Omega$

Therefore, gain of the circuit $= 53.7$

$$\omega_L = \sum \frac{1}{C_i R_{is}}$$

Where,

C_i is the ith capacitance and,

R_{is} is the equivalent resistance across the ith capacitance considering the other capacitors are short circuit.

$C_i = C_4 = 0.1\,\mu F$

$$R_{is} = \left[\left(\frac{R_{13} \| R_9}{\beta + 1} + r_{e_4}\right) \| R_{10}\right] + R_{11}$$

Thus $f_L = 0.2\ \text{MHz}$

$$\omega_H = \frac{1}{\sum C_i R_{io}}$$

Where,

C_i is the ith capacitance and,

R_{io} is the equivilant resistance across the ith caparitor considering the other capacitors as open circuit

$$\omega_H = \frac{1}{\sum \left(C_{be_i}(\beta + 1) r_{e_i}\right)} \text{ i.e. } f_H = 1.3\ \text{GHz}$$

Where,

C_{be_i} is the parasatic capacitance across the base and emiiter of ith transistor and,

r_{e_i} is the small signal emitter resistance of the ith transistor.

$C_{be_i} = 0.35\ \text{pF}$,

$r_{e_2} = r_{e_3} = 5\,\Omega$,

$r_{e_4} = 2\,\Omega$

$r_{e_1} = 25\,\Omega$

2.2.7 The input and output resistance of the circuit

The input and output resistance of the circuit as simulated by the spice is as follows:

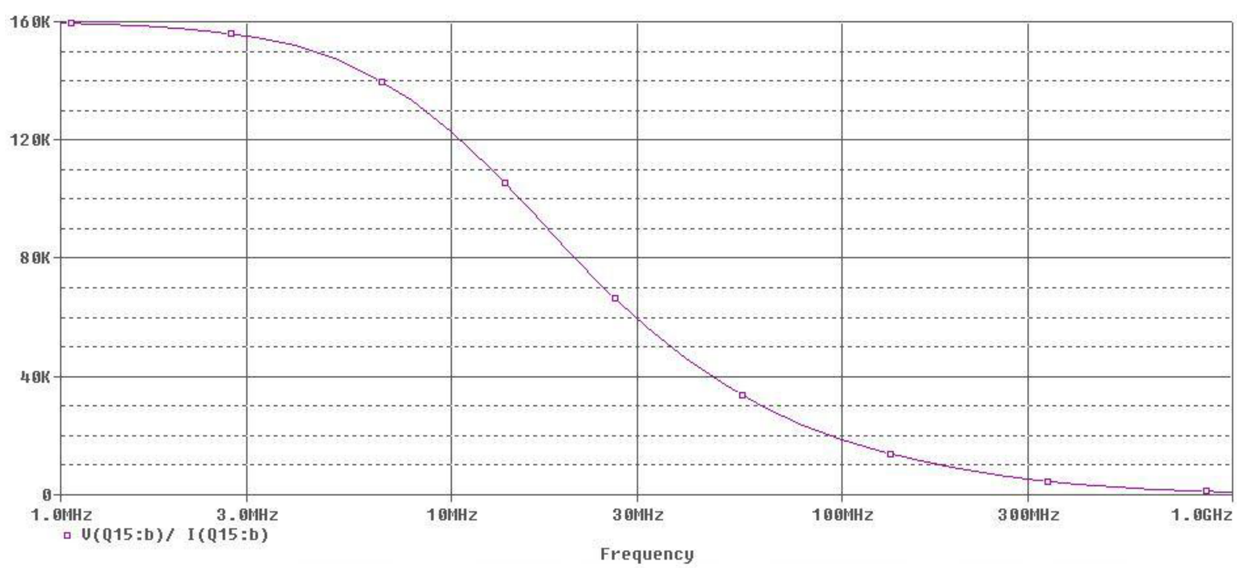

Figure 24 The input resistance of the circuit

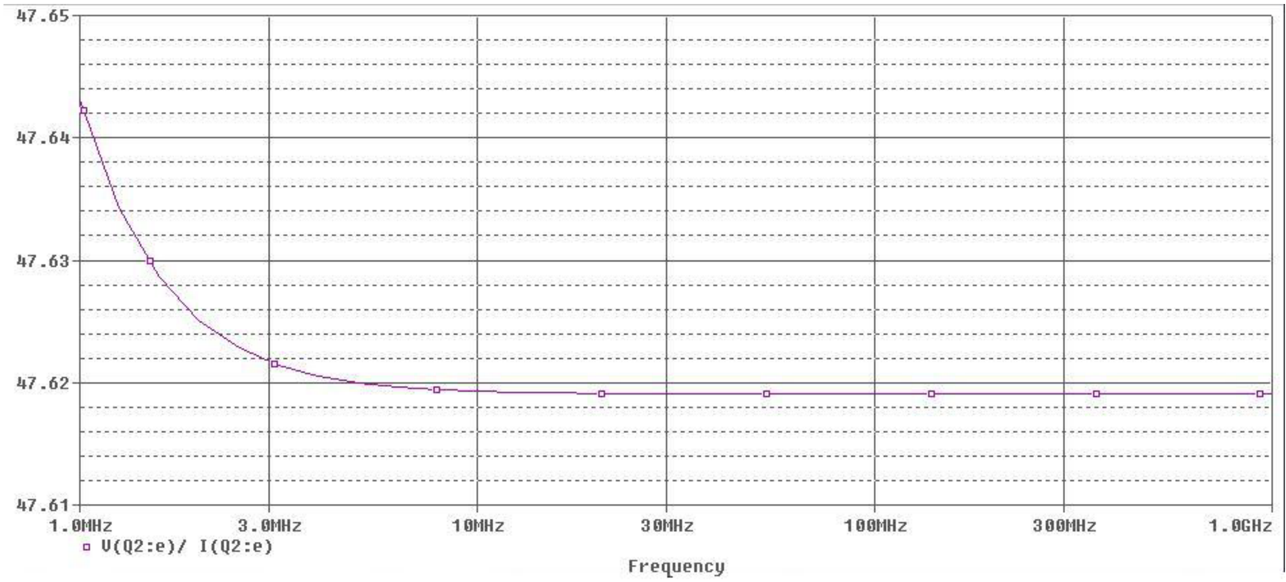

Figure 25 The output resistance of the circuit.

2.2.8 PCB Design

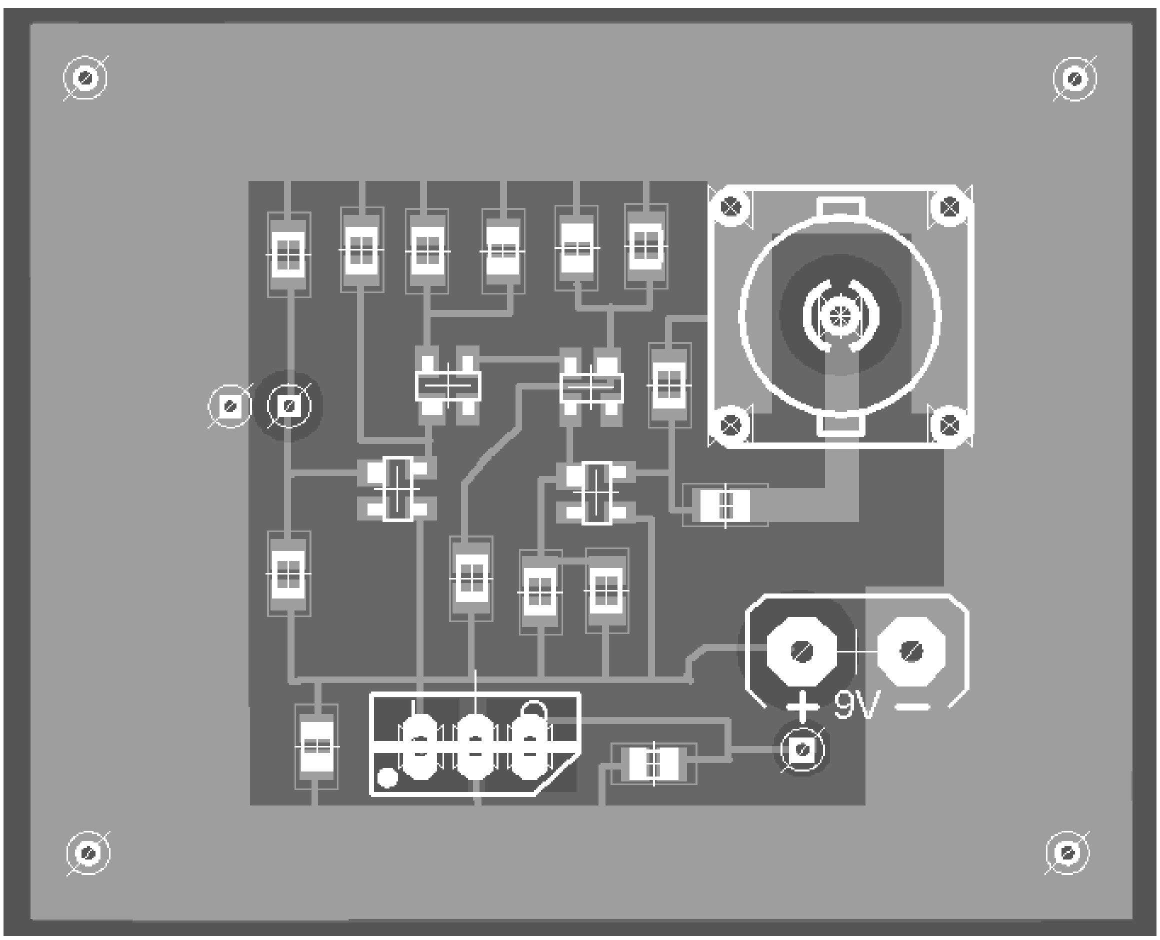

Figure 26. The PCB Layout of the designed circuit. The actual size of the board is 3.5 cm X 4.5 cm

3. Testing of the circuit

3.1 Test set up details

The testing of the circuit was conducted in the lab. A loop antenna was used as a transmitter antenna and power was pumped into it. The transmitter and receiver antenna were placed at the diagonal corners of the lab. The signal received by the active antenna was captured in digital oscilloscope. The signal received at the active antenna end and passive antenna end were then compared.

3.1.1 Test Procedure

i. The resonant frequencies of the transmitting monopole antenna were measured using Network analyser and noted.
ii. The signal was transmitted from the transmitter antenna at the resonant frequency using signal generator.
iii. The signal received at the passive antenna end was noted.
iv. The signal received at the active antenna end was noted.

3.1.2 Equipments used

i. Network Analyser, Model HP 8753E
ii. Signal generator, Model MG 3601A
Range – 0.1 MHz to 1040 MHz
iii. Spectrum Analyzer

3.2 Observations

1.	Transmitting power	= +13.9 dB
2.	Distance between the transmitting and receiving antenna	= 6 m
3.	The diameter of the receiving antenna	= 5 mm
4.	The height of the receiving antenna	= 1 m
5.	Voltage of the power supply at the beginning of the testing	= 16 V
6.	Voltage of the power supply at the end of the testing	= 15.2V
7.	Duration of testing	= 2 Hours

Table 1. The readings at the active and passive antenna end showing the amplification in the signal of Circuit 1

Sl.no	Frequency (MHz)	Signal at the Passive antenna end (dBm)	Signal at the Active antenna end (dBm)
1	60	-80.6	-68.6
2	85	-85.4	-69.8
3	95	-78.6	-59
4	100	-74.6	-49.9
5	105	-68.9	-54.6
6	140	-71.4	-60.6
7	150	-75.4	-63.6
8	158	-65.4	-52.3
9	159	-72.3	-56.6
10	160	-70.2	-54.4
11	165	-70.4	-56.6
12	170	-74.8	-56.4
13	180	-72	-63.2
14	185	-78.3	-66.4
15	190	-82.3	-73.4

3.3 Test results and interpretation

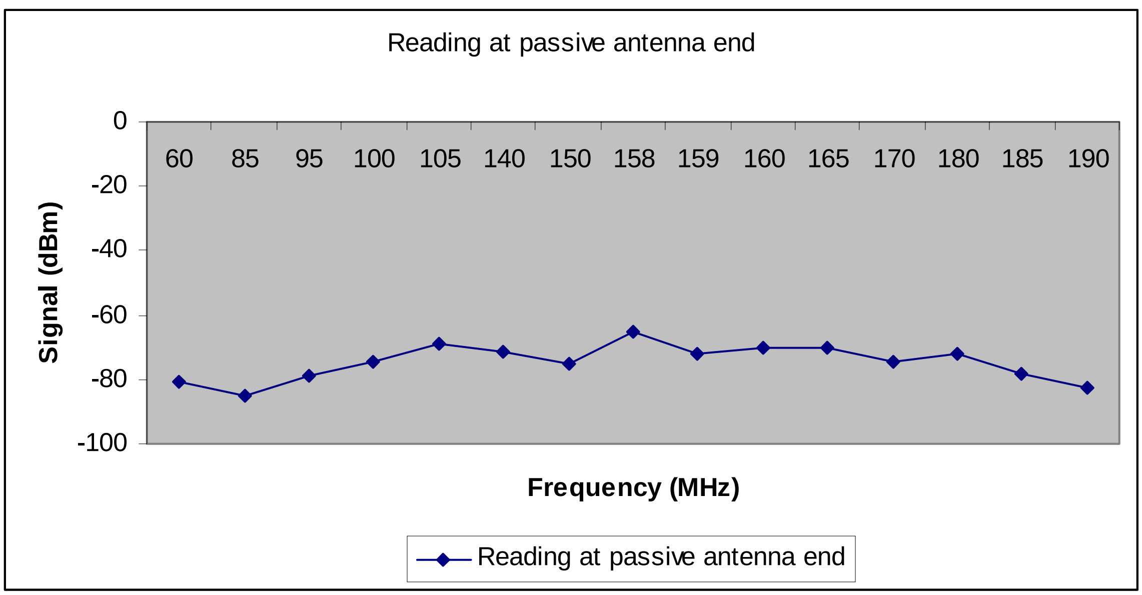

Figure 27. The graph showing the signal strength at the passive antenna end.

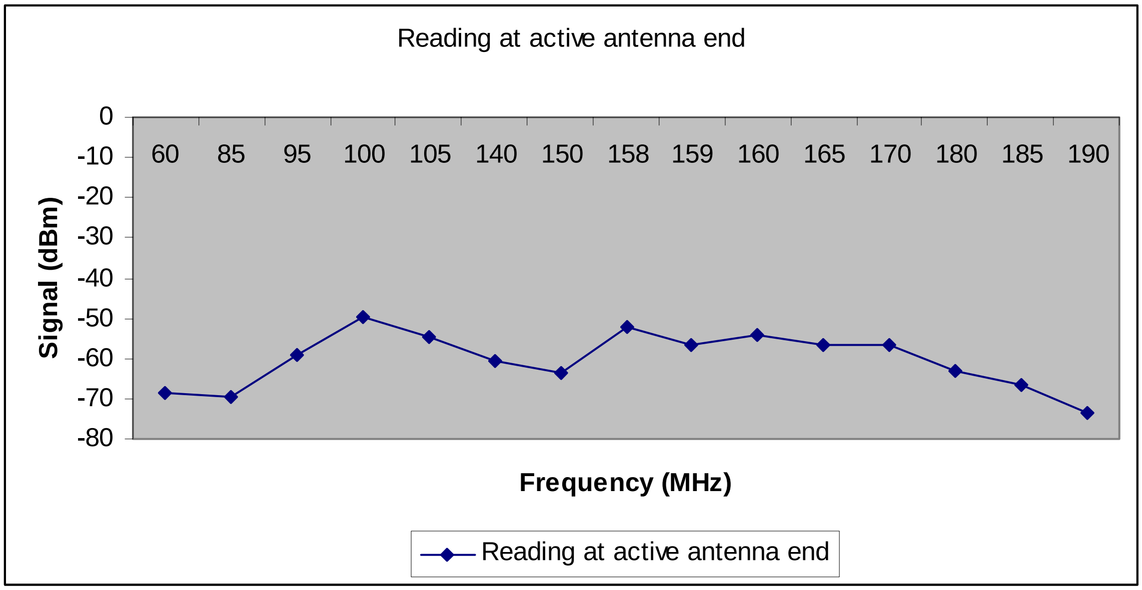

Figure 28. The graph showing the signal strength at the active antenna end.

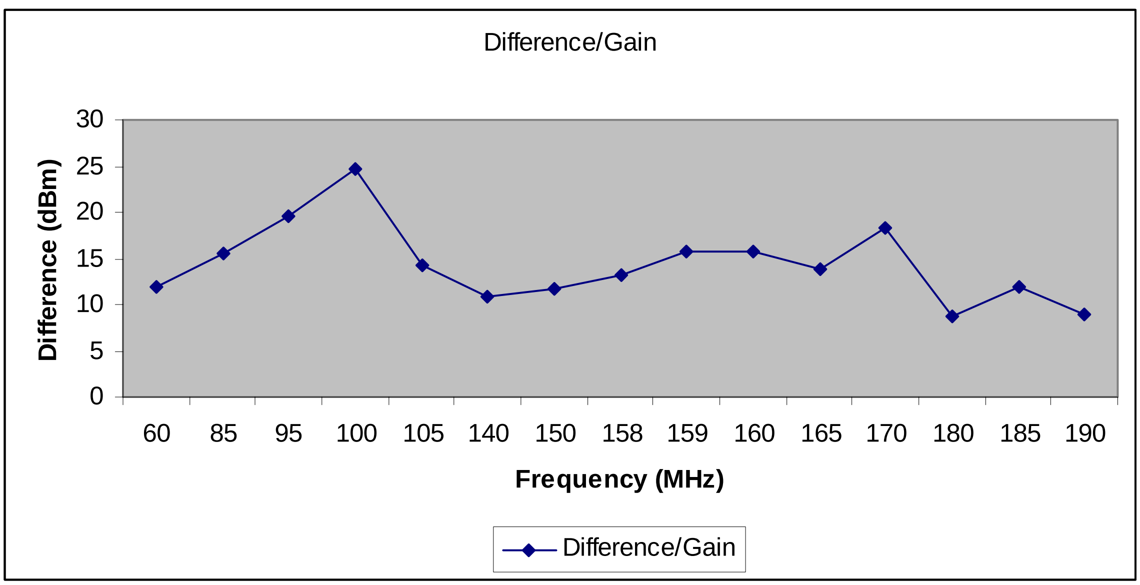

Figure 29. The graph showing the difference between the signals received at the passive antenna end and active antenna end i.e the gain.

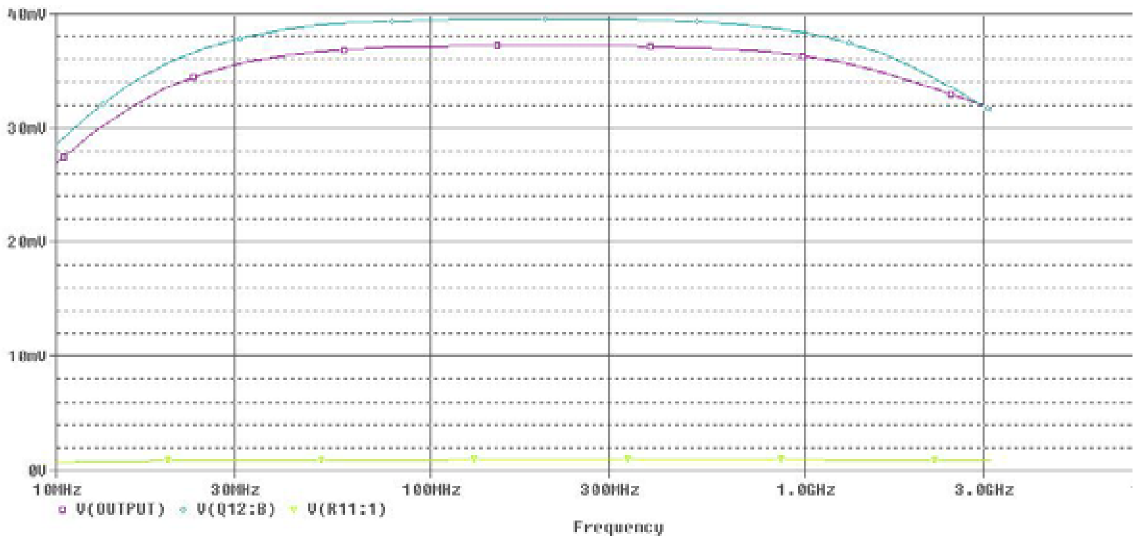

Figure 30 Spice simulation of the circuit shown in Figure13

The readings above 200 MHz could not be taken due to unavailability of transmitting antenna. The circuit works at 800 MHz. The reading at 800 MHz could be checked due to the resonating harmonic frequency of the available transmitting antenna.

4. Conclusion

The size of a resonant antenna is large for lower frequencies of operation. The use of electrically small monopole antennas entails highly capacitive impedance which is difficult to match as any passive element employed for the same would make the system narrowband. A transistor is used to achieve the impedance matching as they have high input impedance and hence it makes their usage favourable. The objective was to design an active antenna involving wide band amplifier in the VHF and UHF range. The frequency response of the circuit is comparable to its spice simulated frequency response.

5. Future Scope

An active antenna could also be used as a receiver to Loop antennas used for NVIS (Near Vertical Incidence Skywave) communications and hence separate the systems for transmit and receive in such a manner that a complex design of duplexer could be done away with. Also the system would be lighter and portable too.

An active integrated antenna could be fabricated which would have extensive usage for GSM, CDMA and GPS application. Active integrated antenna will have versatile applications in the growing area of wireless communications. At millimetre wave frequencies, the antenna size becomes very small so that it is possible to integrate the active antenna on a small chip. It is believed that the full development of active integrated antenna will bring the wireless communications technology into the new era.

6. Precautions

1. The receiving antenna should be aligned along the maxima of the radiation pattern of the transmitting antenna.
2. There should not be any metal structures around the circuit, because even a small piece of wire can act as an antenna and cause interference.
3. The circuit should be properly grounded.

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