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**Network Analyzer**

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## ABSTRACT

The project involved designing and developing a network analyzer for the operation in the range of 120 MHz to 210 MHz. A Network Analyzer is used to determine the VSWR (Voltage Standing Wave Ratio) v/s frequency characteristics of the DUT (Device under Test). The project deals with generating VSWR and reflection coefficient statistics of a load without phase attributes. The basic functioning of the project involves generation of sinusoidal waveform for frequency up to 70 MHz using a DDS (Direct Digital Synthesizer). The frequency generation is controlled by the tuning words sent serially from the computer to the DDS via the microcontroller, in synchronous mode. Using a four matched diode tripler circuit frequencies in the range of 120-210 MHz have been generated. The signal is then passed though a micro strip line directional coupler to which the DUT is attached. Two power detectors measure the power proportional to transmitted and reflected power from the DUT, in terms of DC voltage. This voltage is fed to the ADC which is connected to the microcontroller. Microcontroller waits for the ADC to finish the conversion, takes input from a parallel port and sends the detected data back to the computer. The computer performs data processing to determine the actual power output of the detectors. These power values are used to determine the reflection coefficient and VSWR of the DUT.

## TABLE OF CONTENTS

## 1. INTRODUCTION

The network analyzer is a device which measures the reflection coefficient (γ) and transmission coefficient (τ) of the DUT against a specified set of frequencies.

Reflection coefficient is defined as the amount of power reflected back from the load (DUT) when connected to the source. This parameter is important from the view of performance of the circuit at high frequencies. It gives the VSWR (Voltage Standing wave Ratio).

$$\gamma = \frac{\text{Reflected Power}}{\text{Incident Power}} \qquad (1.1)$$

In terms of characteristic impedance ($Z_0$) of the transmission line, Impedance of the load ($Z_L$) reflection coefficient can be written as

$$\gamma = \frac{Z_L - Z_0}{Z_L - Z_0} \qquad (1.2)$$

The VSWR (Ґ) can be calculated from the reflection coefficient using the following relation

$$\Gamma = \frac{1 + |\gamma|}{1 - |\gamma|} \qquad (1.3)$$

Basic block diagram of the network analyzer is shown in Figure 1.1. AD9951 from Analog Devices is used as a Direct Digital Synthesizer for the purpose of generating RF frequencies. This forms basis for automatic control of the device using computer. The frequency word is generated through the computer and a tuning word is synchronously passed to the DDS. The frequency of the signal is tripled by multiplying the frequency by using a tripler. This frequency is then passed through the coupler. The DUT is connected at the direct port of the coupler. Two power detectors are located at isolated port and coupled port. The coupled port power is proportional to transmitted power while the isolated power is proportional to reflected power from DUT. Power detection is done using AD8313 which gives DC voltage proportional to log of the power detected. ADC connected to a microcontroller receives the DC voltage. Digital data at the output of ADC is passed to the computer through microcontroller. The computer performs operations like finding actual transmitted power, reflected power, calculating reflection coefficient, VSWR, plotting the VSWR vs. frequency. Power measurement is done in computer by interpolating power voltage curve of AD8313.

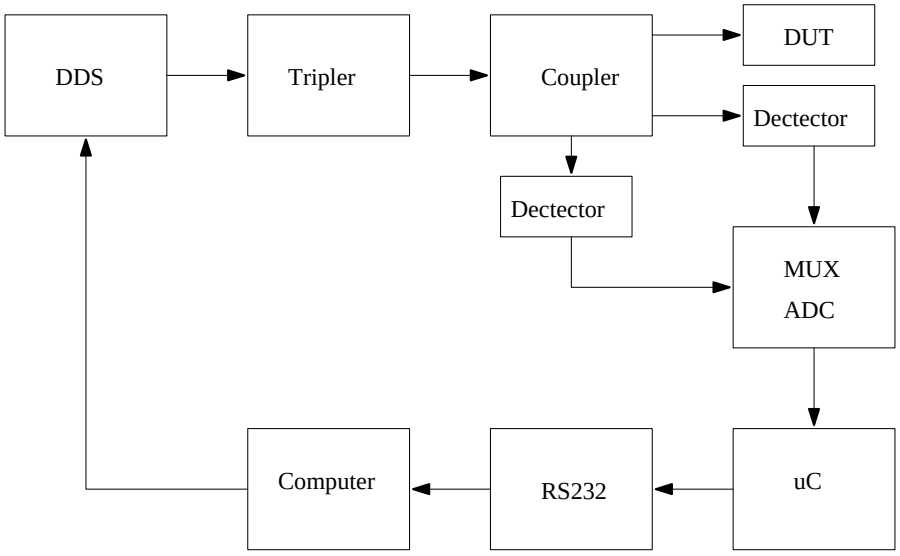



**Figure 1.1 Functional Block Diagram of Network Analyzer**

## 2. DIRECT DIGITAL SYNTHESIZER

DDS is the basic unit for the network analyzer. The AD9951 is a direct digital synthesizer (DDS) with 14-bit DAC operating up to 400 MSPS. The AD9951 uses advanced DDS technology, coupled with an internal high speed, high performance DAC to form a digitally programmable, complete high frequency synthesizer capable of generating a frequency-agile analog output sinusoidal waveform at up to 150 MHz. The AD9951 is designed to provide fast frequency hopping and fine tuning resolution (32-bit frequency tuning word). The frequency tuning and control words are loaded into the AD9951 via a serial I/O port.

### 2.1 Operation of DDS

The output frequency ($f_O$) of the DDS is a function of the frequency of the system clock (SYSCLK), the value of the frequency tuning word (*FTW*), and the capacity of the accumulator ($2^{32}$, in this case). SYSCLK is the clock frequency obtained by multiplying basic clock frequency by using PLL block. The exact relationship is given below with $f_S$ defined as the frequency of SYSCLK. The value at the output of the phase accumulator is translated to an amplitude value via the COS(x) functional block and routed to the DAC to produce sinusoidal wave.

$$f_O = (FTW)(f_S)/2^{32} \quad with \quad 0 \le FTW \le 2^{31}$$

$$f_O = f_S \times \left(1 - \left(FTW/2^{32}\right)\right) \quad with \quad 2^{31} < FTW < 2^{32} - 1$$

AD9951 can be used in either differential or single ended mode for clock input. In the circuit differential mode is used. Connecting the external pin CLKMODESELECT to Logic High enables the on-chip crystal oscillator circuit. With the on-chip oscillator enabled, a 12 MHz external crystal is connected to the REFCLK and REFCLKB inputs to produce a low frequency reference clock. The PLL allows multiplication of the REFCLK frequency in the range of 4 to 20. Control of the PLL is accomplished by programming the 5-bit REFCLK multiplier portion of Control Function Register No.2 with bits 7:3.

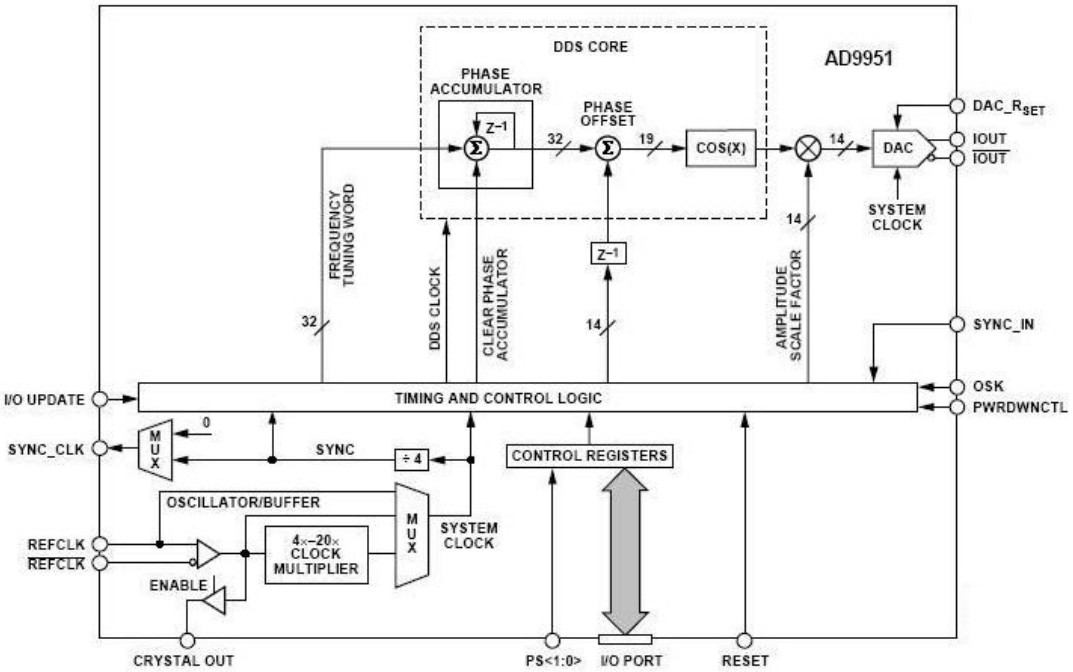



**Figure 2.1 Block Diagram of DDS**

The AD9951 has an integrated 14-bit current output DAC. Two complementary outputs provide a combined full-scale output current ($I_{OUT}$). The full-scale current is controlled by an external resistor (RSET) connected between the DAC_RSET pin and the DAC ground (AGND_DAC). The full scale current is proportional to the resistor values as follows

$$R_{SET} = 39.19 / I_{OUT}$$

In the circuit $R_{SET}$ value is taken as 3.9 k. with Iout 10 mA. The amplitude of the output voltage at $I_{OUT}$ is controlled by $R_{SET.}$ Only signal ended output from $I_{OUT\ has}$ been taken. Differential output using $I_{OUT,}$ $I_{OUTB}$ would provide better signal to noise ratio. The AD9951 serial port is a synchronous serial communications port. The interface allows read/write access to all registers that configure the AD9951. Using MSB first format, the AD9951's synchronous serial communication can be configured using serial I/O (SDIO), I/O update (IOUPDATA) and serial clock (SCLK).

Complete DDS circuit consists of a 160 MHz low pass filter, and Low noise amplifier (LNA). DDS works at 1.8V. The DAC in DDS requires 3.3 V. The circuit is separated in digital and analog part. Both the parts require different 1.8 V supplies as well as different grounds. 1.8 V is generated using TS72218. The two grounds are connected by a zero resistance away from AD9951 chip. The control of DDS is done using three lines SCLK, SDIO, IOUPDATE from microcontroller.

**2.2 Filter**

The output of DDS is taken single ended. To reduce the high frequency noise in the output of the DDS, an elliptic low pass sixth order filter of bandwidth 160 MHz has been incorporated. The filter characteristics are provided in Appendix A. The circuit diagram is shown in Figure 2.2.

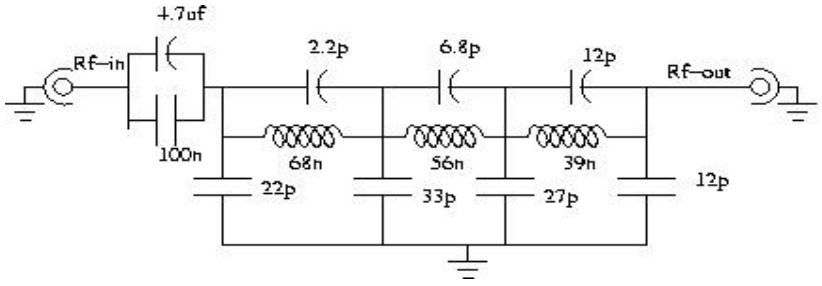



**Figure 2.2 Filter 160 MHz**

**2.3 Amplifier**

The output at $I_{OUT}$ is about 100 mV p-p. The cut off BAT15-04 is 0.224 V. Hence the required output is about 1 V p-p. To increase the output voltage to desired output voltage of 1V p-p, a low noise amplifier ERA3 by Mini-Circuits was used. The LNA works from DC up to few Ghz with a gain of 10dB. The circuit diagram is given in figure 2.3

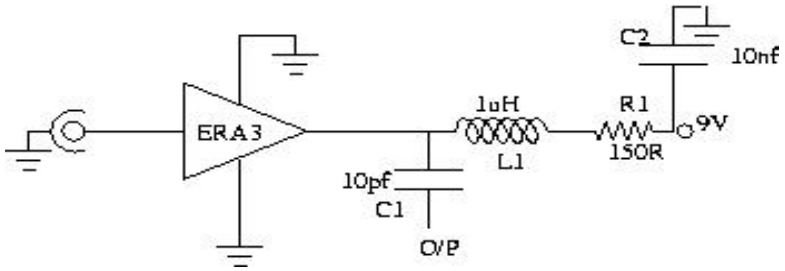



**Figure 2.3 ERA amplifier**

Complete circuit diagram of AD9951 in given in Appendix F.

## 3. FREQUENCY TRIPLER

It is necessary to multiply the frequency of low noise DDS output without significantly degrading the phase noise. Low noise frequency tripler constructed with schottky signal diodes generate odd-order harmonics with very low excess noise. The tripler circuit consists of four matched schottky diodes BAT-15-04 diodes by Infineon which has very high bandwidth limit. The tripler circuit works on the principle of converting sinusoidal signal to square pulses which are rich in odd harmonics. A filter now selects the desired tripled frequency. Four matched diodes D1, D2, D3 and D4 along with inductor forms the odd harmonic generator. Diode, D1, D3 rectify the input signal resulting in a DC current in L4. A square wave of current flows in D2, D4. The output network provides a low impedance to ground for the undesired frequencies and directs the desired harmonic to the output. The circuit diagram of the tripler is as shown in figure 3.1 which uses eighth order Butterworth filter of 120-210 MHz bandwidth. The output of filter is given to LNA BGA430 with 32 dB gain.

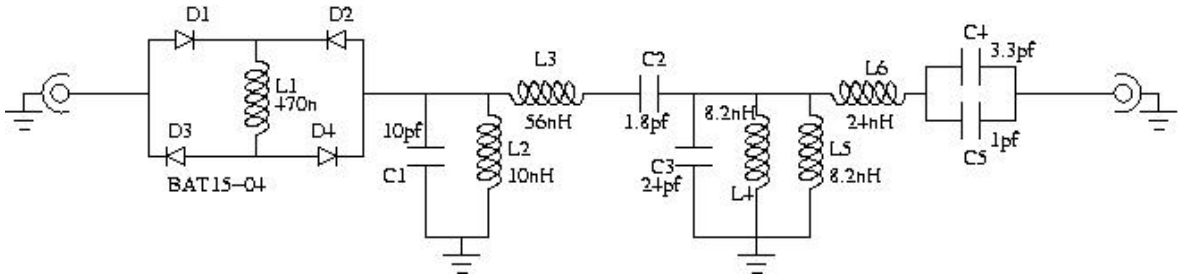



**Figure 3.1 Frequency Tripler**

### 3.1 BGA430 (Broad Band High Gain LNA)

The tripler circuit used completely passive circuit. The conversion gain of the tripler circuit is very low. Hence it needs to be amplified by a high value. The BGA430 is a broad band high gain amplifier based upon Silicon Bipolar Technology B6HF with 32dB gain. BGA430 has inbuilt circuit for matching with 50 ohms over a wide range of frequencies Hence no eternal matching circuit is required. Due to the high gain of the BGA430 RF blocking at the supply pin (VCC) has to be done very carefully. A broad-band low impedance RF path to GND has to be provided at VCC. If no appropriate RF blocking is used, RF can couple via the internal power lines to the input and the device might oscillate. Basic circuit of BGA430 is shown in Figure 3.2.

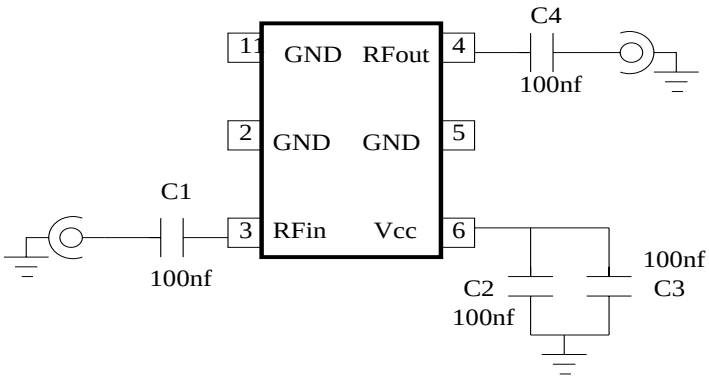
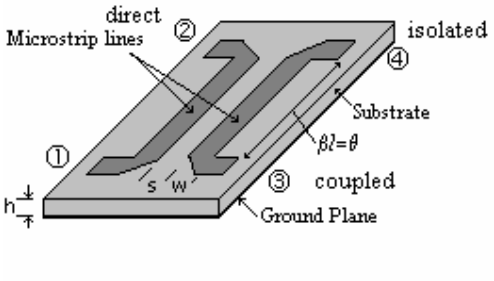



**Figure 3.2 BGA430**

## 4. DIRECTIONAL COUPLER

When two transmission lines are close together, because of the interaction of the electromagnetic fields of each line, power can be coupled between the lines. Those coupled lines are used to construct directional couplers. The directional coupler is a 4 port device. When the power is passes through a port then direct power is received in one port. The port beside the transmission port is called as coupled port. The forth port is called as isolated port.
In ideal directional coupler for our purpose of network analyzer a fraction of input power should be coupled and rest of the power should be received at direct port with matched conditions. No power should be received at isolated port.
1) Directivity is a measure of how well the coupler isolates two Opposite-traveling (forward and reverse) signals.
2) Transmission loss is the total loss in the main line of a directional coupler, and includes both insertion loss and coupling loss.
Thus Directivity should be as large as possible with minimum transmission loss. The basic diagram of directional coupler is as in Figure 4.1.




**4.1 Directional Coupler**

Directional coupler has been used for analyzing DUT. DUT is connected to direct port. The input power will be proportional to coupled port and the reflected power will be proportional to power at isolated port.
The reflection coefficient (γ), VSWR (Γ) are given by

$$\gamma' = (\text{Power at isolated port in dB}) - (\text{Power at coupled port in dB})$$

$$\gamma = 10^{\gamma'}$$

$$\Gamma = \frac{1+|\gamma|}{1-|\gamma|} \qquad (4.1)$$

The use of directional coupler in network analyzer is shown in Figure 4.2.

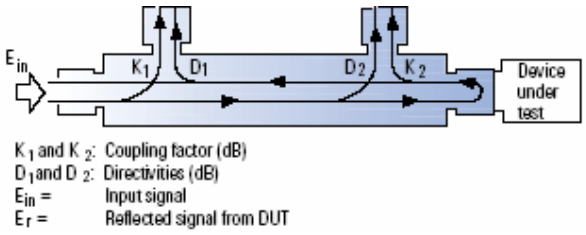



**Figure 4.2 Functioning of Directional coupler**

## 5. POWER DETECTOR

AD8313 is used as a power detector which is basically is a multistage demodulating logarithmic amplifier that can accurately convert an RF signal at its differential input to an equivalent decibel-scaled value at its dc output. The AD8313 works signal frequencies from 0.1 GHz to 2.5 GHz. The input dynamic range (decibel range of inputs over which AD8313 can be used is –65 dBm to 0 dBm (with 50 Ω matching at the input), It requires a

power supply of 2.7 V to 5.5 V and supply decoupling. The AD8313 uses a cascade of eight amplifiers, each having a nominal gain of 8 dB and a −3 dB bandwidth of 3.5 GHz. This produces a total midband gain of 64 dB. The current-mode outputs of these cells are summed to generate a piecewise linear approximation to the logarithmic function. They are converted to a low impedance voltage-mode output by a transresistance stage, the logarithmic intercept is positioned at nearly −100 dBm, and the output ranges from about 0.45 V dc at −73 dBm input to 1.75 V dc at 0 dBm input.

The power supply to each AD8313 $V_{POS}$ pin is decoupled by a 10 Ω resistor and a 0.1 μF capacitor. The two signal inputs are ac-coupled using 680 pF RF capacitors. A 53.6 Ω resistor across the differential signal inputs combines with the internal 900 Ω input impedance to give a broadband input impedance of 50.6 Ω. A basic circuit of power detection in RSSI (Received Signal Strength Indicator) mode is used in the circuit designing.

**5.1 Basic connections for RSSI (Received Signal Strength Indicator) mode**

The AD8313 connected in its basic measurement mode. A power supply between 2.7 V and 5.5 V is required. The power supply to each of the $V_{POS}$ pins should be decoupled with a 0.1 μF ceramic capacitor and a 10 Ω series resistor. The PWDN (power down) pin is shown as grounded. The input in this case is terminated with a simple 50 Ω broadband resistive match. If over-voltages are expected on the $V_{OUT}$ pin, a series resistor, $R_{PROT}$, is included. A 500 Ω resistor has been used to protect against over-voltage beyond to ±5 V.

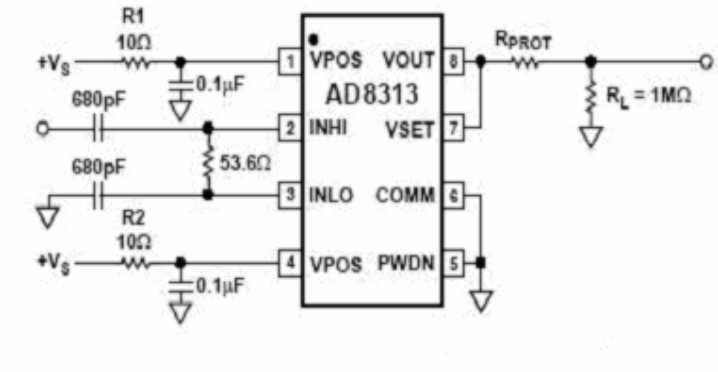



**Figure 5.1 AD8313 RSSI Mode**

## 6. DATA ACQUISITION

The output of the two power detectors are connected to two input pins of 8 bit analog to digital converter chip ADC0809 through two buffers. The clock to the ADC was provided through the microcontroller AT89C52. The micro-controller sends the select line input corresponding to the power detector, the ADC starts converting the analog o/p of the power detector to 8 bit digital data. By that time, the microcontroller waits for the EOC (End of Conversion) pin to be high. The o/p of the ADC was connected to one of the ports of the microcontroller. As soon as the EOC goes high, the microcontroller reads the o/p of the ADC.

**6.1 Analog to Digital Converter (ADC)**

The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. The circuit uses channel 0 and 1 for the two inputs. The input states for the address lines to select any channel are shown below. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

| ANALOG CHANNEL | SELECTED ADDRESS LINE | | |
|---|---|---|---|
| | C | B | A |
| IN0 | L | L | L |
| IN1 | L | L | H |

The DC values from detector circuit ranges between 0.5 V to 2 V. Hence to obtain maximum possible accuracy Vref(-) has been set to 0V and Vref(+) to 2 V using resistive divider circuit. Two buffers are used between actual analog data from power detector and ADC inputs. Pin P1.0 can be used as a clock to the ADC. By setting value of the T2CON.1 of microcontroller Pin P1.0 gives the square wave output same as the baud rate.

**6.2 Micro processing unit**

The task of the Micro-controller AD89C52 was to serially interact with computer and to control the functioning of the DDS and the ADC. The serial communication with the PC was setup at a baud rate of 9600bauds/sec. The crystal frequency provided to the microcontroller was 11.0592 MHz. Clock frequency generated was 921KHz. Timer2 was used as a baud rate generator for serial communication.

Timer2 Operating Modes

| RCLK +TCLK | CP/$\overline{RL2}$ | TR2 | MODE |
|---|---|---|---|
| 0 | 0 | 1 | 16-bit Auto-reload |
| 0 | 1 | 1 | 16-bit Capture |
| 1 | X | 1 | Baud Rate Generator |
| X | X | 0 | (Off) |

The formula for baud rate generation for Timer 2 is as follows:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{32 * [65536 - \text{RCAPH}, \text{RCAPL}]} \qquad (6.1)$$

if RCAPH = FFh

RCAPL = DCh

Baudrate = 9600 baud/sec

As soon as the circuit is switched on, the microcontroller sends the initialization bytes to the DDS. These comprise of two control words namely CFR1 and CFR2. The microcontroller then starts interacting with the PC, and waits for the computer to send the frequency control word (5 bytes). As soon as the microcontroller gets the frequency control word from the PC, it transmits them to the DDS. This transmission of freq. control word to the DDS takes place serially and synchronously. Bit by bit data is transmitted from pins of Port1. After every control word, the microcontroller sends an IOUPDATE to the DDS. The DDS then generates the corresponding frequency signal, which goes into the tripler, then the coupler and the power detector, the output of which finally goes into the ADC.

The microcontroller provided the clock to the ADC. This was accomplished by using the Output Enable feature of Timer2, which gives the clock at P1.0. The microcontroller provides the ADC with a start pulse, which triggers the conversion in the ADC, and waits for the EOC to get high. As the ADC gets high, it saves the ADC o/p byte in a register. It then changes the select line input of the ADC to start conversion of the output of the other power detector into digital data, and again waits for the ADC. As soon as the EOC gets high, microcontroller reads the o/p of the ADC and transmits both the bytes serially to the PC.

**6.3 Data Processing**

The two bytes received by the computer corresponds to the DC voltages at the two power detectors which, in turn, represent the reflected and transmitted power for the given load (DUT). To generate power values in dB from the voltages, the power voltage line equation of the AD8313 power detector is used. The calibration mismatch in the two power detectors is also considered while calculating individual power values. Using equation 4.1 the reflection coefficient and VSWR are calculated for a series of frequencies. The obtained VSWR values are then interpolated using the software to obtain a continuous VSWR vs. frequency graph. Short Circuit and Open Circuit Loads should ideally show an infinite VSWR for the complete range of frequencies. VSWR of a matched load comes out to be unity. Based on the ideal values the software calculates the mean square error magnitude for finite loads, the span of frequencies considered for error calculation is that for which the results for the short circuit and open circuit loads match with the theoretical values.

## 7. DESIGN CONSIDERATIONS

DDS: This is the basic functioning part of the circuit. DDS can produce a frequency up to 150 MHz for a crystal frequency of 20 MHz. But as it was not oscillating with DDS, a crystal of value 12 MHz has been used. The output of DDS starts getting spurious after 100 MHz. A 160 MHz sixth order elliptic low pass filter has been incorporated for this reason. The analog and digital grounds should be separate. The analog and digital supplies should be given by different voltage regulators.

Amplification of voltage from DDS should be appropriate. It should be greater than twice the barrier voltage 0.224V of the schottkey diodes (BAT15-04) used in the tripler circuit. The value of amplification should not exceed a threshold as it will lead to the saturation of the LNA BGA430 used in the tripler producing spurious even harmonics.

Tripler: The diodes used (BAT15-04) have a frequency cut off of few GHz. The main purpose was to convert a sine wave to square wave with odd harmonics. A necessary condition for this is that the diodes should be matched. Hence an anti-parallel pair of diodes was used. The operating range of the complete device is decided by the bandwidth of the tripler circuit which, in turn, depends on the operating frequency. As the fifth harmonic also plays role in conversion gain and the performance of the tripler, it is the deciding frequency of bandwidth. If f is the center frequency of the filter used in tripler then the bandwidth is equal to f/2. DDS produces a second harmonic, which is about 15 dB less than fundamental. This produces an effect on tripler output. The output of the tripler should be near 0 dBm to operate the power detectors in the linear range.

Coupler: The coupler was made using 200 MHz as the center frequency. The length of the coupler depends on the frequency of operation. Figure 7.1 provides a statistical description of the coupler. The length of the directional coupler is given by $L=\lambda_{eff}/4$. The simulations are performed on I3ED software.

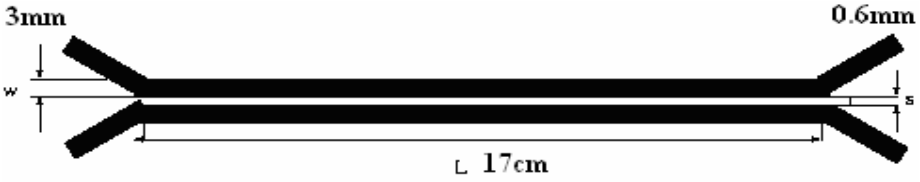



**Figure 7.1 Construction of Directional Coupler**

Power detector: A log amplifier is used as a power detector. A true RMS power detector is not a necessity of the application. A proper impedance matching network was implemented at the input of power detector. It will reduce the effective power entering in the detector and the external Power-Voltage of the detector. Even slight mismatch between the component values of the two detectors leads to large mismatch in their output.

Calibration: This is an important part of the project. The output of power detector should ideally give 0.5V when no input is given. However, when the DDS is off, the noisy input forces the output of the power detector up to 0.8 mV. Hence corresponding considerations must be taken while calculating the power from the voltage. The cable loss is about 1 to 2 dB per cable. Hence it should also be taken into account while calculating power. .

PCB design: A substrate of 4.4 glass epoxy 0.8 mm substrate is used for RF circuits. For proper impedance matching the micro strip lines should have characteristic impedance if 50 ohms. According to the following formula for the characteristic impedance $Z_o$ of the transmission line to be 50 ohms the line width of PCB needs to be 1.5mm.

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98\,H}{0.8W + T}\right)$$

$$0.1 < \frac{W}{H} < 3.0 \qquad 1 < \varepsilon_r < 15$$

## 8. PROJECT STATUS

The range of frequencies over which the network analyzer can work depends on the frequency generator, bandwidth of the coupler, power detector. The circuit is able to generate up to 210 MHz with high accuracy and resolution. The circuit is able to calculate VSWR of various loads within the frequency range of 114 MHz-210 MHz. The accuracy of the result varies with load characteristics. Finer results are obtained while testing a load which has a low VSWR. The calibration of the circuit has been done using a matched load and short circuit load. The calculated VSWR although not very accurate, gives a trend of the load characteristics over the range of frequencies.
The mismatching of two power detectors has been equalized by using software interpolations. The ADC currently being used provides 8 bit digital output. The accuracy can be increased by using higher bit ADC. The frequency of operation can be significantly increased by cascading another frequency tripler. An attempt was made to generate till 600 MHz using this method, but because of grounding problem, second harmonic distortion of the previous circuit takes place and the generated frequency is not pure.
Following modifications can be made in order to further improve the performance:-
1) High speed AVR microcontrollers (ATMEGA128) with inbuilt 10 bit ADC can be used.
2) Frequency generator circuit can be modified with the use of PLL and VCO, in which the clock of the PLL is provided by DDS circuit. This will greatly remove the harmonic distortions in the output of generator.
3) A standalone interface / display can be interoperated with the circuit.
4) There is a scope for modification at the software end, i.e. to plot the VSWR v/s Frequency graph on a smith chart.

## 9. CONCLUSION

Project involved design and development of a prototype of network analyzer over the range of frequencies from 120-210 MHz. Power detection, at various ports of a directional coupler, facilitates calculation of reflected power. The prototype is able to calculate reflection coefficient, VSWR of the load (DUT) for the aforesaid range of frequencies. The software script developed on the computer provides with the output plot of VSWR vs. frequency. The design is based on Direct Digital Synthesizer and tripler as generating unit, microcontroller control unit, ADC as data acquisition, and computer for data processing. A coupler is used for measuring the amount of power reflected back by the load. The whole process is automated and is working successfully.

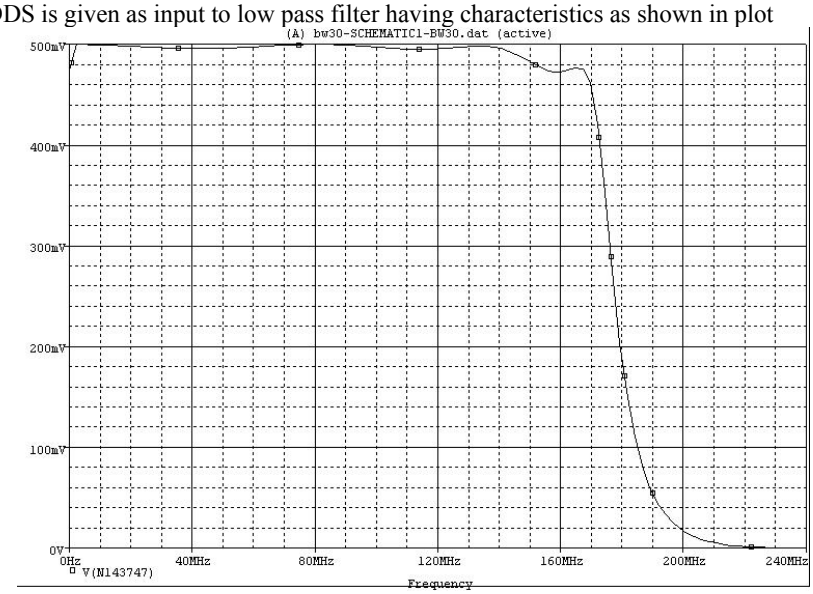
## 10. REFRENCES:

[1] Edward C. Jordon, “Electromagnetic waves and radiating system", second edition, 2003
[2] Pozar, David M. Microwave Engineering Second Edition, Wiley, New York 1998
[3] http://www.emclab.umr.edu/pcbtlc/microstrip.html for calculation of line width, by University of Moussi Rolla.
[4] www.dl5mgd.de/dds/AD9951 by Guilono for basic working of DDS AD9951.
[5] http://www.techlib.com/electronics/2diomult.html for diode tripler circuits by Charles Wenzel

## 11. APPENDIX

### A. 160 MHz low pass filter

Output from DDS is given as input to low pass filter having characteristics as shown in plot




**11.1 Frequency response of 160 MHz low pass filter**

### B. Frequency Tripler

Output from odd harmonic generator circuit consisting of diodes is given to band pass filter whose characteristics are shown in figure 11.2

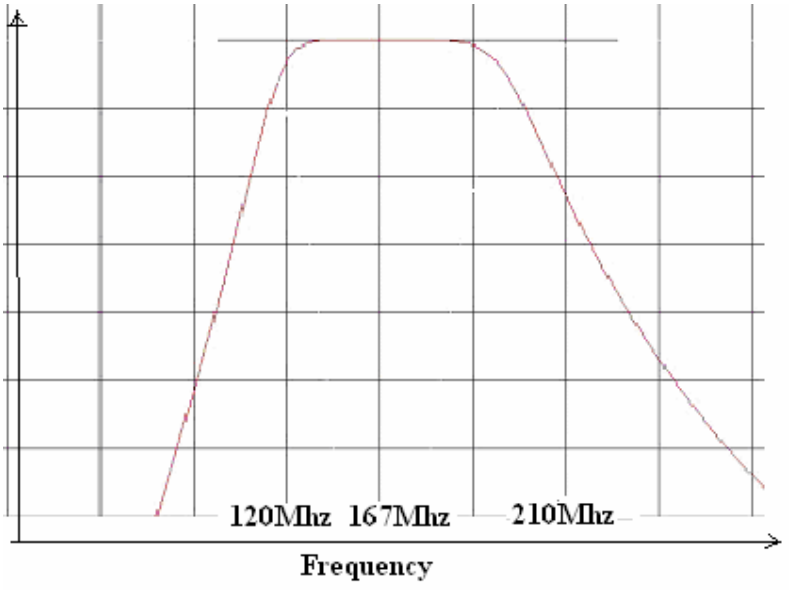



**Figure 11.2 Frequency response of 167Mhz centered band pass filter Observation Table**

**Table 11.1 Tripler Output**

| Input Frequency( MHz) | Output Frequency (MHz) | Output Amplitude(dBm) |
|---|---|---|
| 42 | 126 | -2.1 |
| 45 | 135 | -2.3 |
| 50 | 150 | -3.0 |
| 55 | 165 | -2.5 |
| 60 | 180 | -2.8 |
| 65 | 195 | -2.4 |
| 70 | 210 | -2.7 |

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**C. Power Detector**

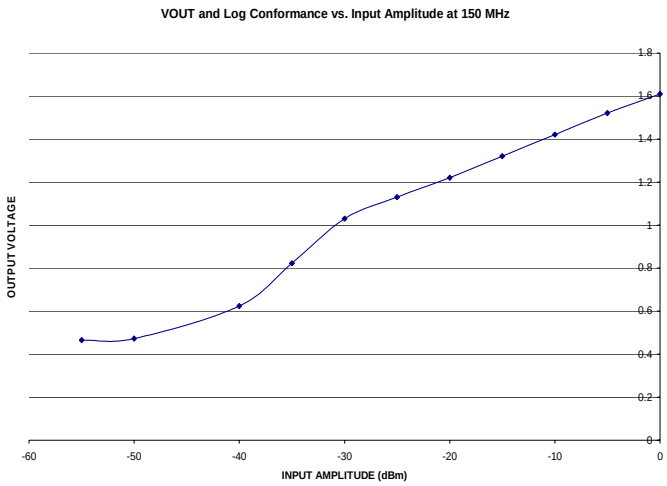
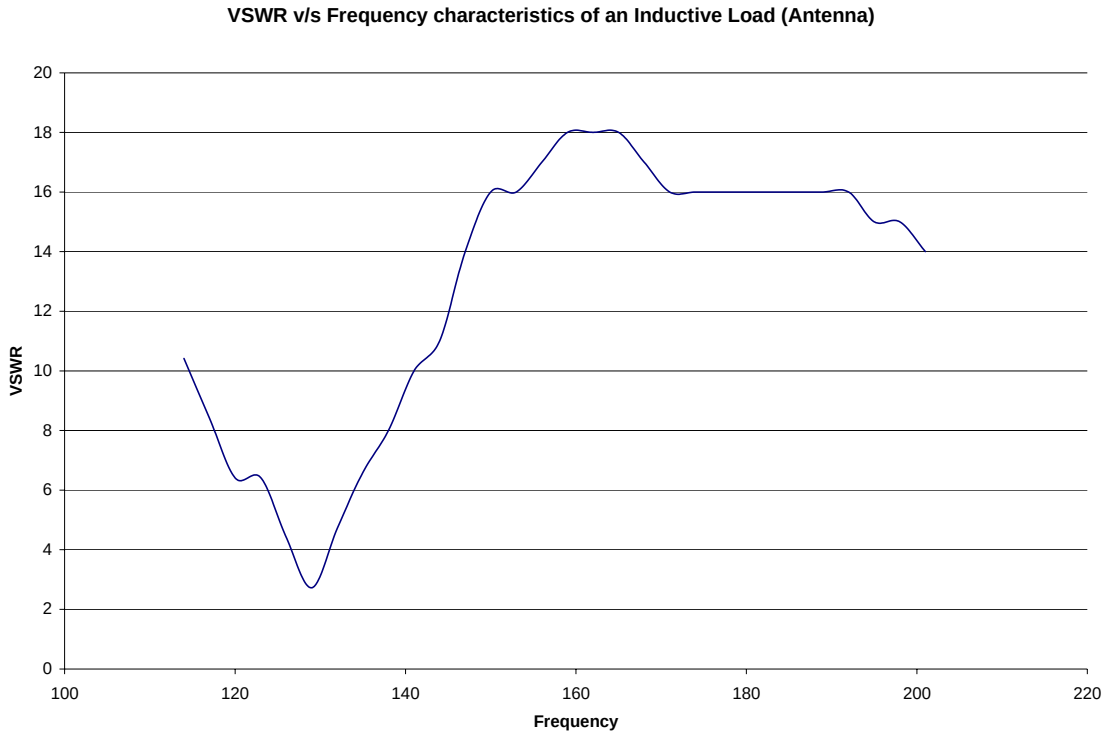


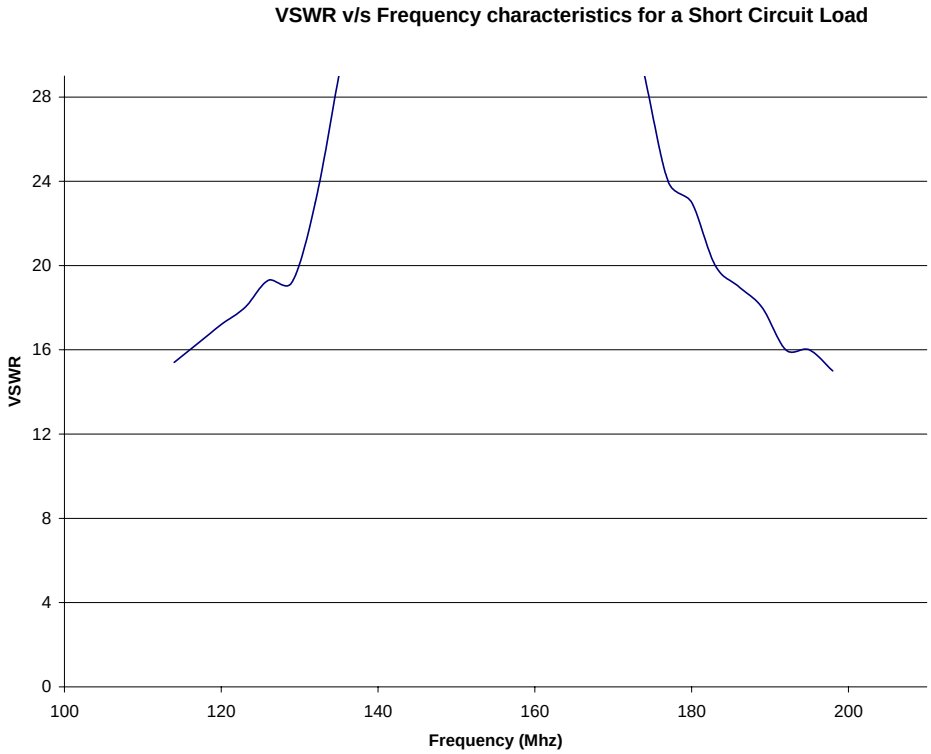

**Figure 11.3 Power Voltage line of power detector**

**Table 11.2 Power detector output**

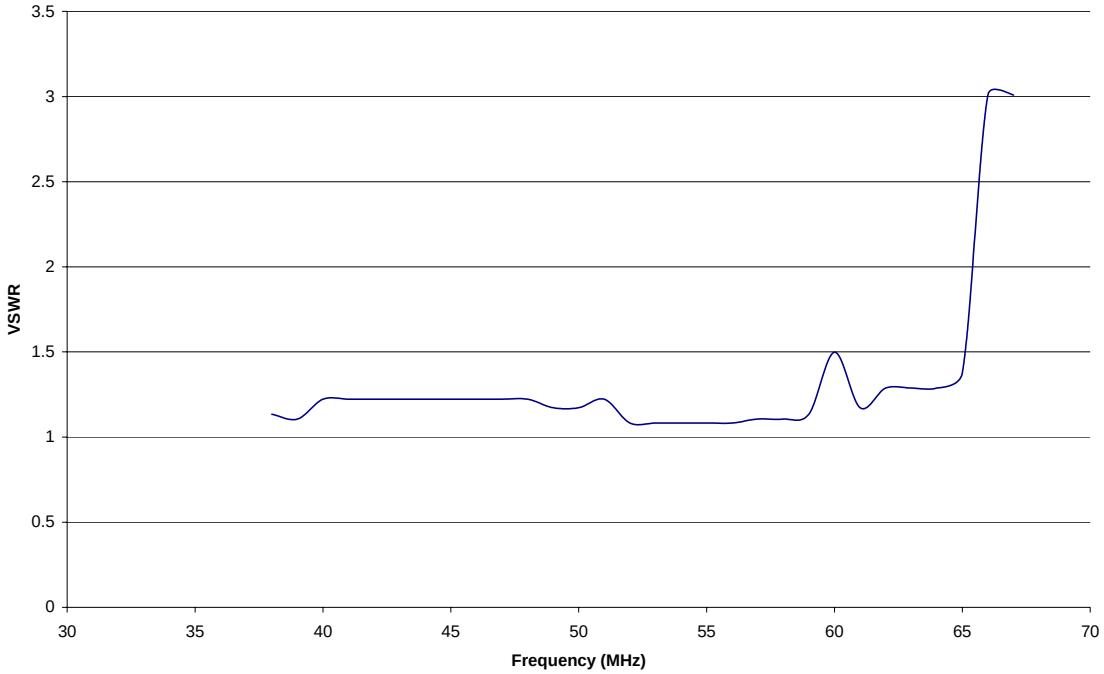
| INPUT FREQUENCY (MHz) | INPUT AMPLITUDE( dBm) | OUTPUT(Volt) |
|---|---|---|
| 150 | 0 | 1.61 |
| 150 | -5 | 1.52 |
| 150 | -10 | 1.42 |
| 150 | -15 | 1.32 |
| 150 | -20 | 1.22 |
| 150 | -25 | 1.13 |
| 150 | -30 | 1.03 |
| 150 | -35 | .823 |
| 150 | -40 | .624 |
| 150 | -50 | .472 |
| 150 | -55 | .465 |

**D. Graphs for various loads**

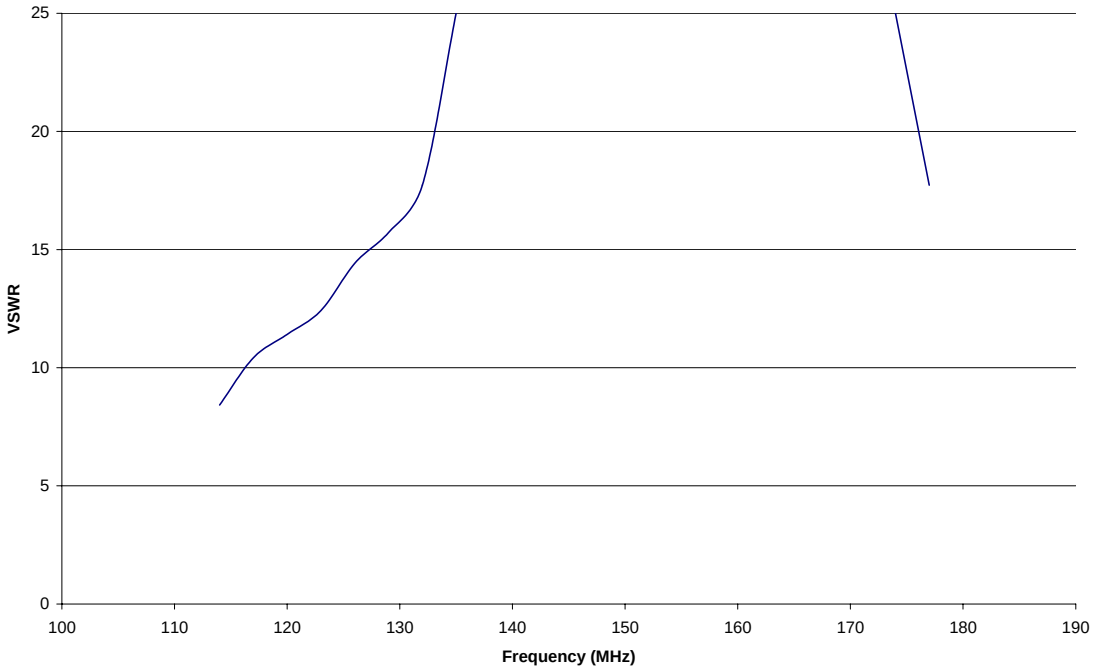


**VSWR v/s Frequency characteristics for a Matched Load**




**VSWR v/s Frequency characteristics for an Open Circuit Load**



**E. Coupler response**

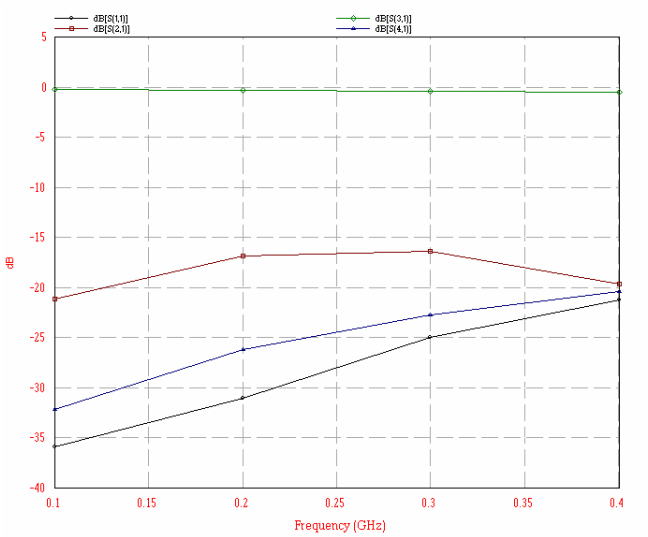



**Figure 11.4 Coupler response**

**F. AD9951 Circuit diagram**

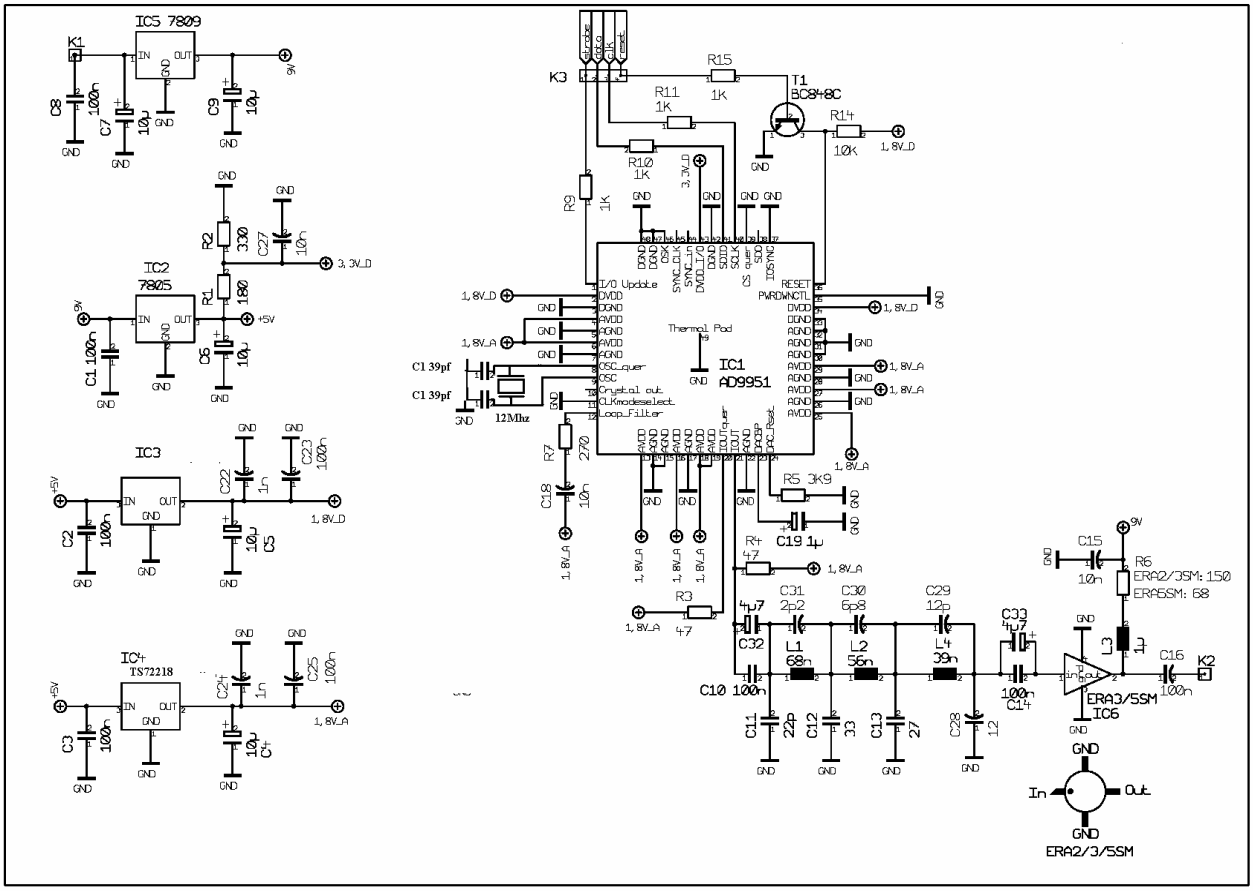



**Figure 11.5 AD9951 circuit**

**G. Control Unit**

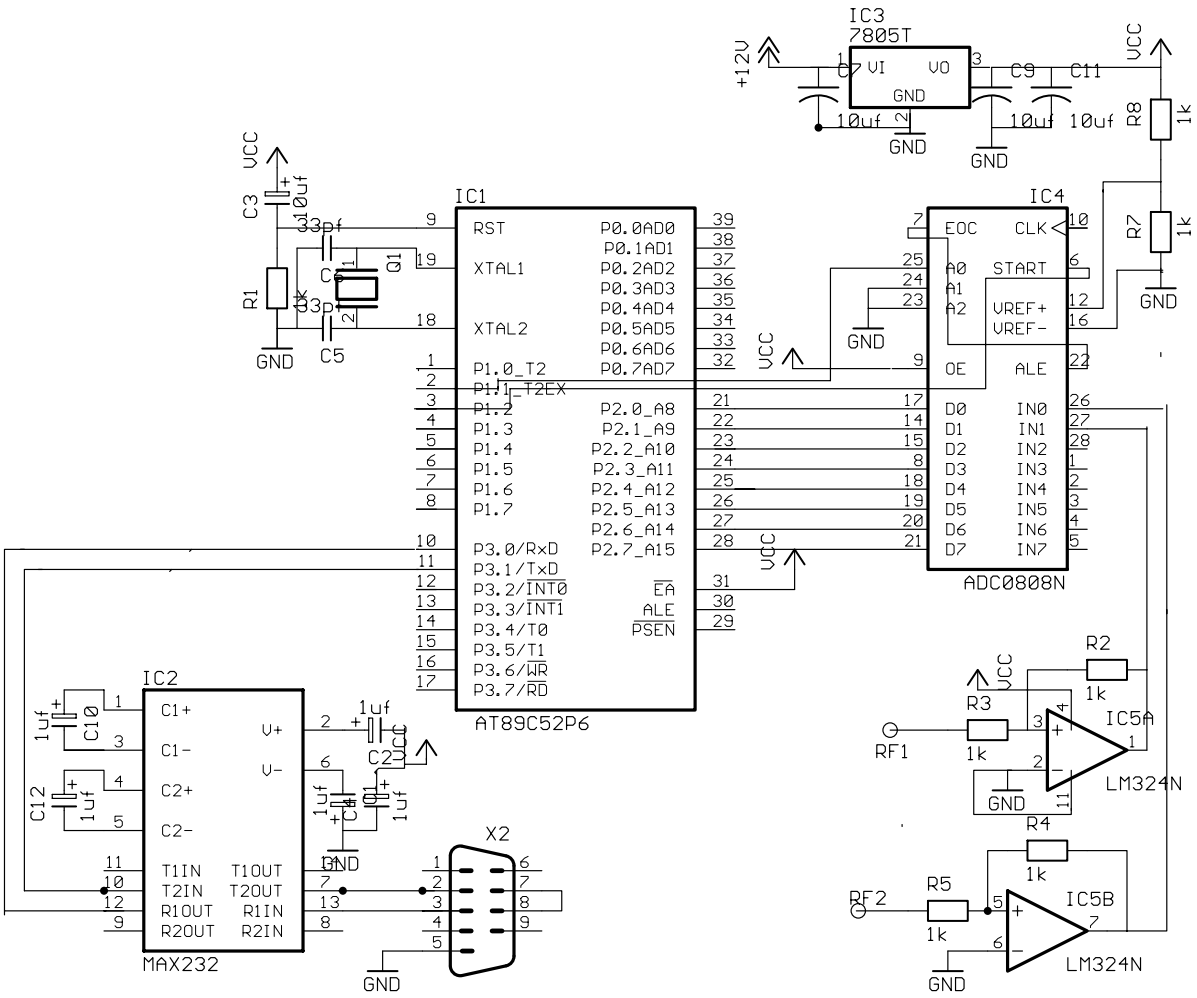



**Figure 11.6 Data acquisition Unit**

**H. Photographs of circuit**

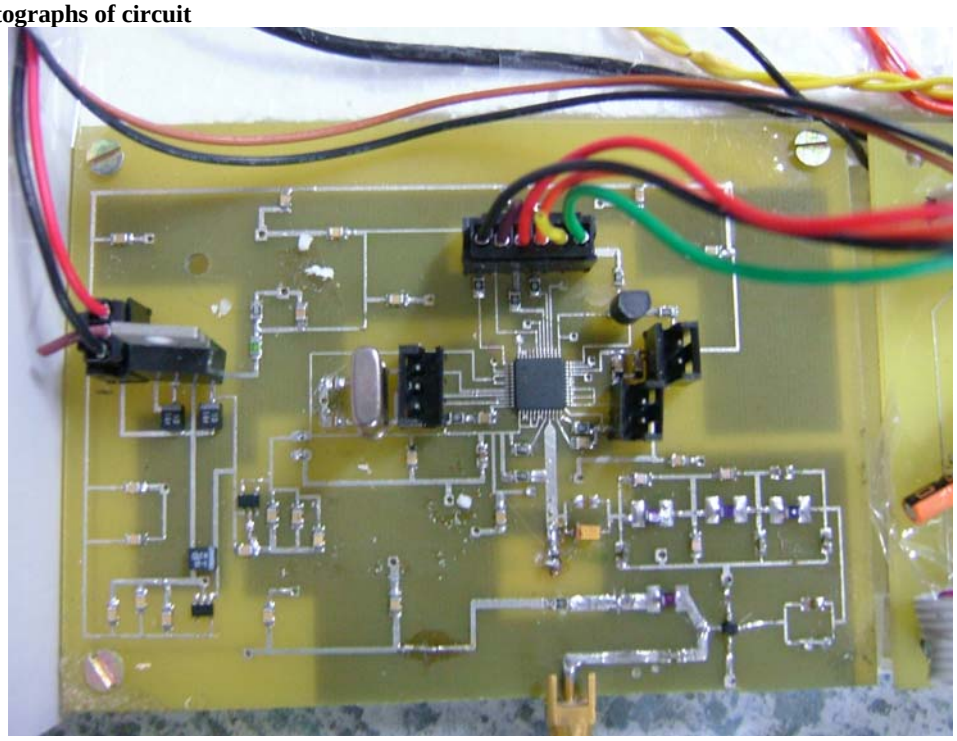


**Figure 11.7 AD9951 1**

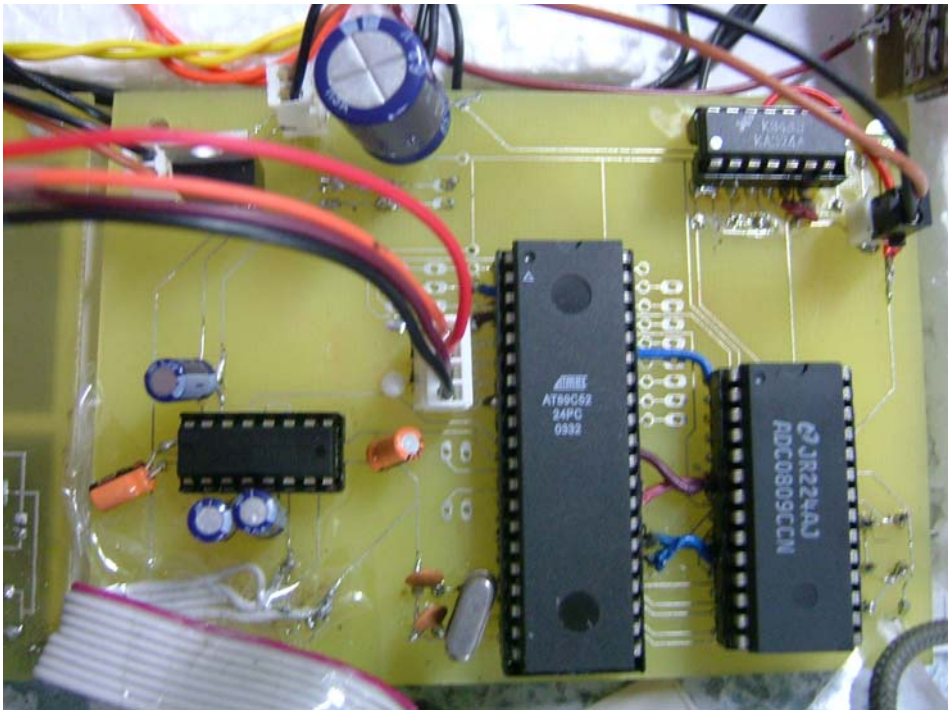



**Figure 11.8 Microcontroller with ADC**

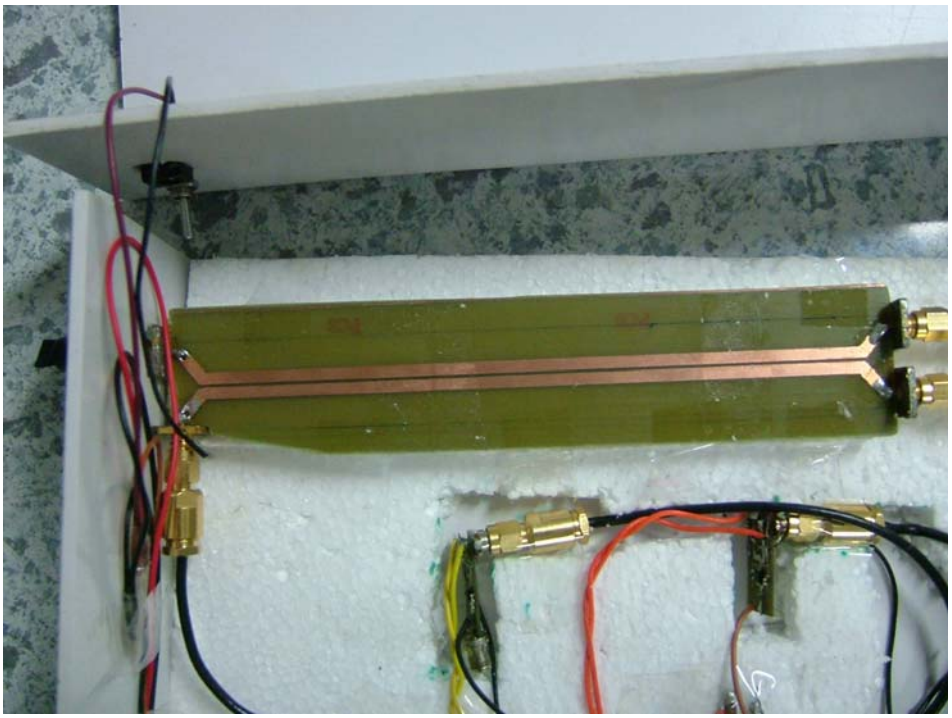


**Figure 11.9 Directional Coupler**

**Figure 11.10 Complete Unit**