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Measurement system for plotting C-V curve of an EIS capacitor

Group No: D 11

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Abstract

The project entails designing a measurement system which plots *C-V characteristics* of an *EIS (Electrolyte-Insulator-Semiconductor)* capacitor. The design utilizes the powerful lock-in amplifier method. The lock-in amplifier is a phase sensitive rectifier which compares the phase of the incoming signal with the reference signal for rectification. This system performs test on the given capacitor and transfers the results to a computer for further analysis and results. It can be further developed as a stand alone system for conducting experiments in characterization laboratories in place of the apparatus in use now at a much lower cost.

Contents

1. Introduction

The EIS (Electrolyte-Insulator-Semiconductor) capacitor is a MEMS device which finds its usage mostly in measurement of pH of electrolytic system. When pH change occurs there is change in the dielectric constant of the electrolytic medium which causes the capacitance of the device to change. This capacitance change can be observed by plotting the HFCV curve for the device. The subject of interest is the change in the flatband voltage of the device which occurs due to pH change.

The current system used in the microelectronic characterization laboratories utilizes many different components, thus making their interfacing difficult. Also since these instruments are multipurpose the cost of the total system is very high. There is a need for a simple cost effective system to obtain the HFCV curve.

This project aims to make a measurement system which plots the HFCV characteristics of an EIS capacitor. The design is based on the powerful technique of Lock-In amplification. The Lock-In amplifier is a phase sensitive rectifier which compares the phase of the incoming signal with the reference signal for rectification. The HFCV test

is performed on the given device and the information obtained is sent to a computer system for further analysis and results. The system transfers the information via parallel port. Currently the system is designed to check device performance on four frequencies.

2. Algorithms

We wish to implement two algorithms for characterizing the behaviour of EIS capacitor. The algorithms are:

2.1. C-V Plotting Method

The measurement of the capacitance of the EIS capacitor is carried out by biasing at a predetermined voltage and then applying a small signal voltage across the capacitor. The out of phase component of the output contains information about the capacitance. The measurement of the capacitance is done using the Lock-In Amplifier.The phase sensitive detector is the prime component of the lock in amplifier. It comprises of an opamp allpass phase shift network, comparator, an optional inverter and analog switch. The phase sensitive detector is used to rectify the incoming signal by comparing it with a reference signal. This reference signal is the same as the input to the DUT. The reference signal is input to the phase shift network. This network produces a phase shift in the output as compared to the input. The output of the phase shifter is fed to a comparator to yield a square pulse to control the analog switch. An optional inverter is a circuit which can be used as both as an inverter and follower depending upon the connection at the positive input terminal. If the positive terminal is grounded then it becomes an inverter else it behaves as a voltage follower. The grounding of the V+ terminal is controlled by the analog switch which is controlled by the output of the comparator. The phase shifter circuit is used to control the phase of the reference signal to bring it in-phase with the input signal of the optional inverter. In this condition we get the maximum dc output.The output of the optional inverter is a rectified version of the input signal. This signal is then passed through a LPF to obtain a constant DC. This dc voltage is directly proportional to the capacitance of the DUT.

2.1.1 Measurement System

This section explains the working of the capacitance meter board. The capacitance of the EIS capacitor is measured by extracting its C-V characteristics. An EIS capacitor behaves like a MOS capacitor in its C-V characteristics. There are two kinds of measurements possible, Low frequency C-V plot and High frequency C-V plot.

2.1.1.1 Measurement Techniques

The measurement of the capacitance of the EIS capacitor is carried out by biasing at a predetermined voltage and then applying a small signal voltage across the capacitor. The out of phase component of the output contains information about the capacitance. The measurement of the capacitance is done using the Lock-In Amplifier. The biasing is generally carried out by a DC ramp voltage which biases the device from accumulation to strong inversion. The ramp rate is kept low since a very high ramp rate can drive the device into a condition called 'Deep Depletion'. The measurement techniques are classified in two categories according to the frequency of the small signal. The various conditions are mentioned below followed by a description of the Lock-In amplifier.

2.1.1.1.1 Low Frequency Technique

The low frequency technique utilizes a very low frequency signal (0.1Hz – 10Hz). To explain the measurement technique we first assume that the DC biasing is such that the device starts from accumulation and goes towards inversion. The ramp rate is also sufficiently low.
The measured capacitance is a series combination of oxide capacitance Cox and the semiconductor capacitance Cs. In Accumulation majority carriers of the semiconductor respond to the incoming signal. Therefore the measured

capacitance is nearly equal to Cox. But as we move towards inversion the semiconductor charge decreases and so does the Cs. Therefore the series combination decreases. As we pass flat-band condition into inversion, the number of carriers on the surface increases again. Therefore the capacitance increases and after V_t the capacitance becomes nearly equal to Cox again. In strong inversion there are minority carriers on the surface, but since the input frequency is very small they can respond to the incoming small signal. The LFCV plot is shown if Figure 2.1.

2.1.1.1.2 High Frequency Technique

The basic structure of measurement does not change from LFCV technique. The frequency of the input signal is increased beyond 100Hz to obtain the HFCV plot. The HFCV plot in accumulation is identical to that of LFCV plot since majority carriers are involved. But as threshold is crossed the semiconductor capacitance Cs goes to CsminHF. Therefore the capacitance in inversion is the series combination of Cox and CsminHF. Refer Figure 2.1 for HFCV plot.

2.1.1.1.3 Deep Depletion

This condition arises when the ramp rate is extremely high and the carriers cannot respond to the changes in DC bias. The effect is seen only in inversion region and it causes the capacitance values to drop. The deep depletion curve is shown in Figure 2.1.

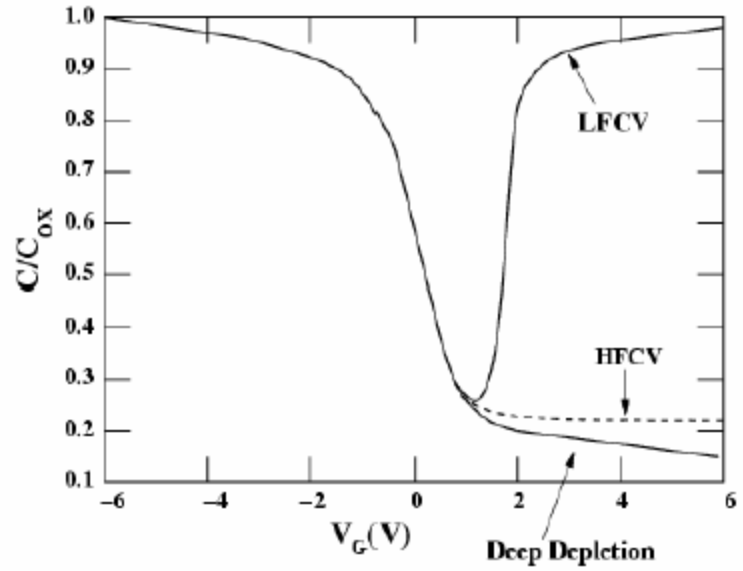

Figure 2.1 C-V plot of EIS Capacitor.

2.1.1.2 Lock-In Amplifier

The capacitance measurement is carried out by using a Lock-In Amplifier. The measurement system comprises of various subsystems which are explained in this section. There are various techniques adopted for measuring the capacitance. A lock-in amplifier uses the reference signal to detect the input signal from the output. If the reference signal is the same as given to DUT, there exists a high phase correlation in the signal output from DUT and the reference signal. This phase correlation can be utilized to extract the input signal from the output even in presence of large noise. Lock-in Amplifier is also called Phase Synchronous Detectors. A detailed description of the lock-in amplifier is given in the following sections with each block explained. A block diagram of the Lock-in amplifier is shown in Figure 2.2.

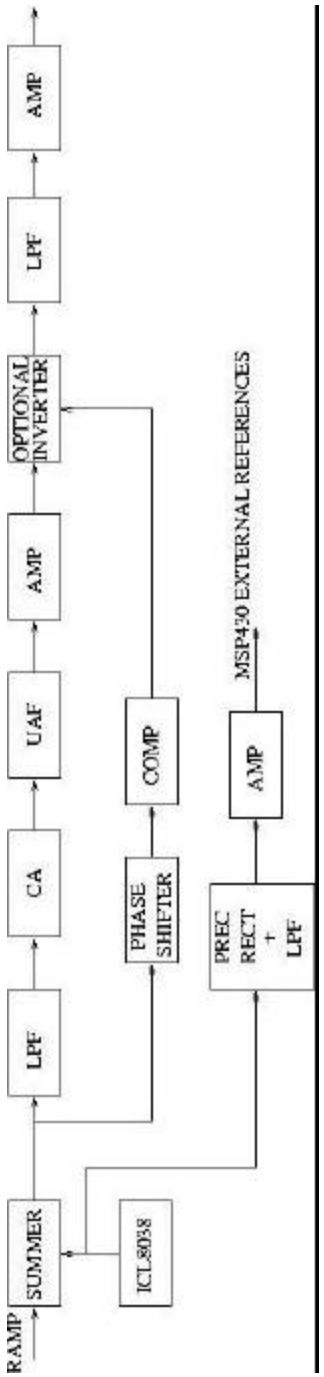

Figure 2.2 Block Diagram of Lock-In amplifier

2.1.1.2.1 Oscillator

A stable oscillator is a very important component of a lock in amplifier. The output of the oscillator should have a low total harmonic distortion. The oscillator used in this project is made from Intersil ICL8038 precision waveform generator. ICL8038 is a good waveform generator IC. It has a low THD, less than 1%. Also the output is stable with time. Although the output changes significantly if the supply voltage to the IC changes. Since a regulated supply is used in the project the supply voltages do not change significantly to alter the output of ICL8038. The

output of ICL038 was passed through an attenuator followed by a LPF of cutoff frequency slightly higher than the desired frequency. This removes any higher harmonics from the signal and we achieve a clean signal free from harmonic distortions. ICL8038 is powered by a ± 5 V supply. The resistances Ra and Rb control the duty cycle and frequency of the signal generated. If Ra = Rb then 50% duty cycle is obtained.

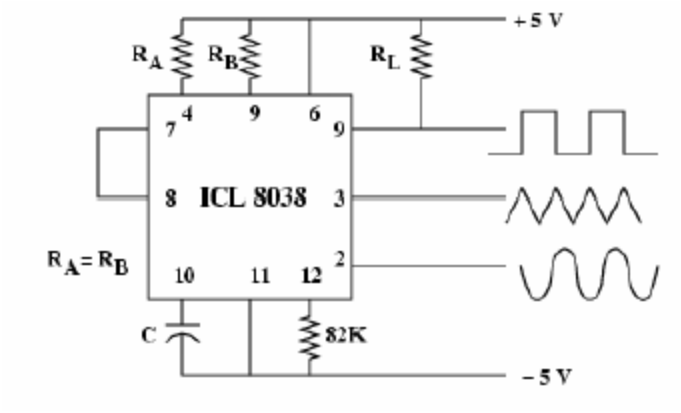

Figure 2.3 ICL8038 oscillator circuit

2.1.1.2.2 Charge Amplifier

Charge amplifier belongs to the class of negative feedback opamp circuits. Charge amplifier amplifies only the ac signals and blocks the dc. Thus it is used as a preamplifier stage in many circuits which utilize small signal superimposed with a dc. The EIS capacitor comes in the feedback path of the charge amplifier. So the charge amplifier is in principle used to measure the capacitance of the EIS capacitor. This project has the same input conditions and thus we use a charge amplifier stage for preamplification of the incoming signal. Figure 2.4 shows a simple charge amplifier. The gain of the charge amplifier is given by (3) when $R >> X_f$, the impedance of the feedback capacitor. The opamp is powered by a ± 5 V supply.

$$\frac{v_o}{v_i} = -\frac{C_x}{C_f} \tag{2.1}$$

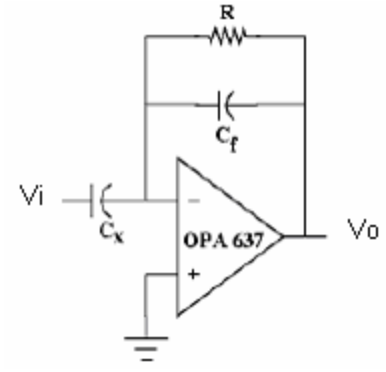

Figure 2.4 Charge Amplifier.

2.1.1.2.3 High-Q Bandpass Filter

The state variable filter topology uses two integrators and an inverting amplifier to obtain HP, BP and LP outputs simultaneously from one circuit. This project uses the state variable IC UAF42 available from burr-brown in a 14-pin

dip package. The chip has inbuilt precision resistors and capacitors. The gain and the frequency of operation can be selected by using only a few external resistors.The state variable filter is used in the project as a high Q band-pass filter to effectively eliminate all noise from the input signal. This noise can be picked up at the charge amplifier stage due to exposed leads. Thus BP filtering is necessary. The SVF was used in a non inverting pole-pair configuration. The circuit used is depicted is Figure 2.5. Resistances R1 and R2 are used to select frequency. The filter was used in a unity gain configuration at the center frequency.

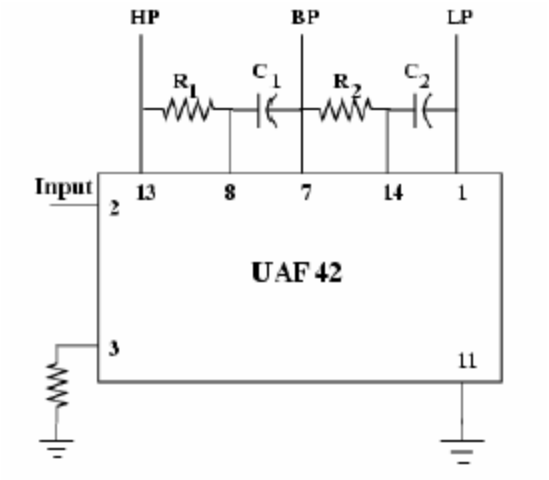

Figure 2.5 High-Q Bandpass Filter

2.1.1.2.4 Non-Inverting Amplifiers

The non-inverting amplifier is an opamp circuit which does not alter the phase of the signal while amplifying. The gain attained from the NI amplifier is given by:

$$\frac{v_o}{v_i} = (1 + \frac{R_f}{R_1}) \tag{2.2}$$

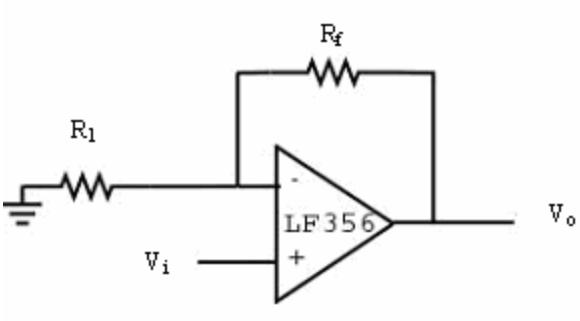

Figure 2.6 Non-Inverting Amplifier

2.1.1.2.5 Phase Sensitive Detector

The phase sensitive detector is the prime component of the lock in amplifier. It comprises of an opamp all-pass phase shift network, comparator, an optional inverter and analog switch. The phase sensitive detector is used to

rectify the incoming signal by comparing it with a reference signal. This reference signal is the same as the input to the DUT.

The reference signal is input to the phase shift network. This network produces a phase shift in the output as compared to the input. The output of the phase shifter is fed to a comparator to yield a square pulse to control the analog switch. An optional inverter is a circuit which can be used as both as an inverter and follower depending upon the connection at the positive input terminal. If the positive terminal is grounded then it becomes an inverter else it behaves as a voltage follower. The grounding of the V+ terminal is controlled by the analog switch CD4066 which is controlled by the output of the comparator.

The phase shifter circuit is used to control the phase of the reference signal to bring it in-phase with the input signal of the optional inverter. In this condition we get the maximum dc output. Figure 2.7 explains the circuit of the phase sensitive detector. The output of the optional inverter is a rectified version of the input signal. This signal is then passed through a LPF (f_o ~ 1-2 Hz) to obtain a constant DC. This dc voltage is directly proportional to the capacitance of the DUT. All the opamps are powered by a ± 5 V supply.

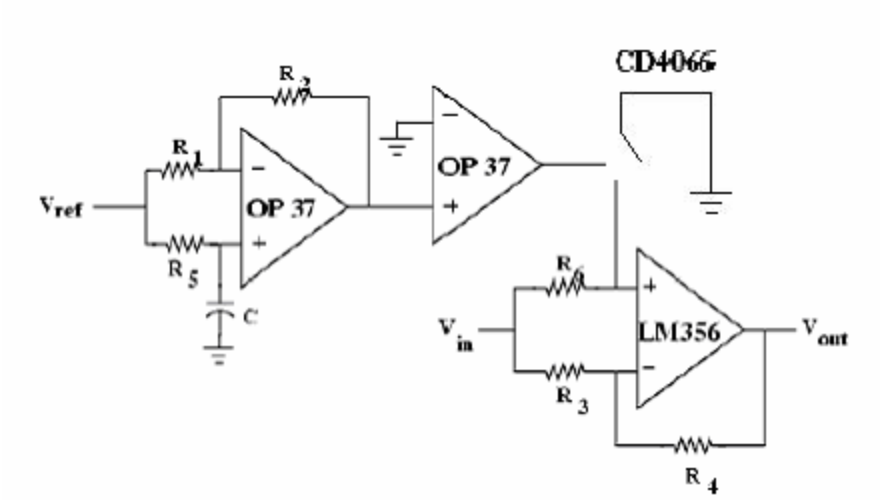

Figure 2.7 Phase Sensitive Detector

2.2. ConCap Method

It's a modified C(V) measurement technique which uses a feedback circuit to maintain the measured capacitance of the EIS capacitor at a constant capacitance value. The measurement set-up consists in principle of a lock-in amplifier for the capacitance measurement and two electronic circuits which drive the bias voltage of the EIS system. The voltage ramp generator is used to measure normal C(V) characteristics in the low (LF) and high (HF) frequency domain. The control circuit adjusts the bias voltage according to the preset capacitance value Csp. This set point Csp is chosen as a defined fraction of Cmax, normally about 0.7xCmax -depending on the shape of the high frequency C(V) curve. In the ConCap method, the system equilibrates from a starting voltage to a bias voltage V_{RB} corresponding to Csp. Any further change in the threshold voltage of the EIS system is now monitored as the change in V_{RB} under the assumption that the C(V) curve keeps its shape during the experiment. This can be checked by comparison with a final measurement.

3. Digital Controller

The MSP430 microcontroller we are using has inbuilt ADC and DAC. Its low power consumption makes it attractive for a battery operated system like ours. It has a JTAG interface and an inbuilt UART to transfer data to the PC through a serial cable. MAX3222 chip is used for serial data communication. It operates at 3.3 V and is thus voltage compatible with the microcontroller. MSP430 microcontroller has 5 digital I/O and one analog/digital port

implemented, P1 - P6. Each port has eight I/O pins. Every I/O pin is individually configurable for input or output direction, and each I/O line can be individually read or written to.

Ports P1 and P2 have interrupt capability. Each interrupt for the P1 and P2 I/O lines can be individually enabled and configured to provide an interrupt on a rising edge or falling edge of an input signal. All P1 I/O lines source a single interrupt vector, and all P2 I/O lines source a different, single interrupt vector.

3.1 Digital I/O Operation

The digital I/O is configured with user software. The setup and operation of the digital I/O is discussed in the following sections.

3.1.1 Input Register PxIN

Each bit in each PxIN register reflects the value of the input signal at the corresponding I/O pin when the pin is configured as I/O function.

Bit = 0: The input is low
Bit = 1: The input is high

3.1.2 Output Registers PxOUT

Each bit in each PxOUT register is the value to be output on the corresponding I/O pin when the pin is configured as I/O function and output direction.

Bit = 0: The output is low
Bit = 1: The output is high

3.1.3 Direction Registers PxDIR

Each bit in each PxDIR register selects the direction of the corresponding I/O pin, regardless of the selected function for the pin. PxDIR bits for I/O pins that are selected for other module functions must be set as required by the other function.

Bit = 0: The port pin is switched to input direction
Bit = 1: The port pin is switched to output direction

3.1.4 Function Select Registers PxSEL

Port pins are often multiplexed with other peripheral module functions. Each PxSEL bit is used to select the pin function – I/O port or peripheral module function.

Bit = 0: I/O Function is selected for the pin
Bit = 1: Peripheral module function is selected for the pin

Setting PxSELx = 1 does not automatically set the pin direction. Other peripheral module functions may require the PxDIRx bits to be configured according to the direction needed for the module function.

When a port pin is selected as an input to a peripheral, the input signal to the peripheral is a latched representation of the signal at the device pin. While PxSELx=1, the internal input signal follows the signal at the pin. However, if the PxSELx=0, the input to the peripheral maintains the value of the input signal at the device pin before the PxSELx bit was reset.

3.1.5 Configuring Unused Port Pins

Unused I/O pins should be configured as I/O function, output direction, and left unconnected on the PC board, to reduce power consumption. The value of the PxOUT bit is don't care, since the pin is unconnected.

The MSP board is shown in Figure 3.1. It has the following ports:

1) JTAG port (for programming)
2) Analog port
3) LCD port
4) Control Signal port (for selecting MUX outputs on analog board)
5) MAX 3222 serial port.

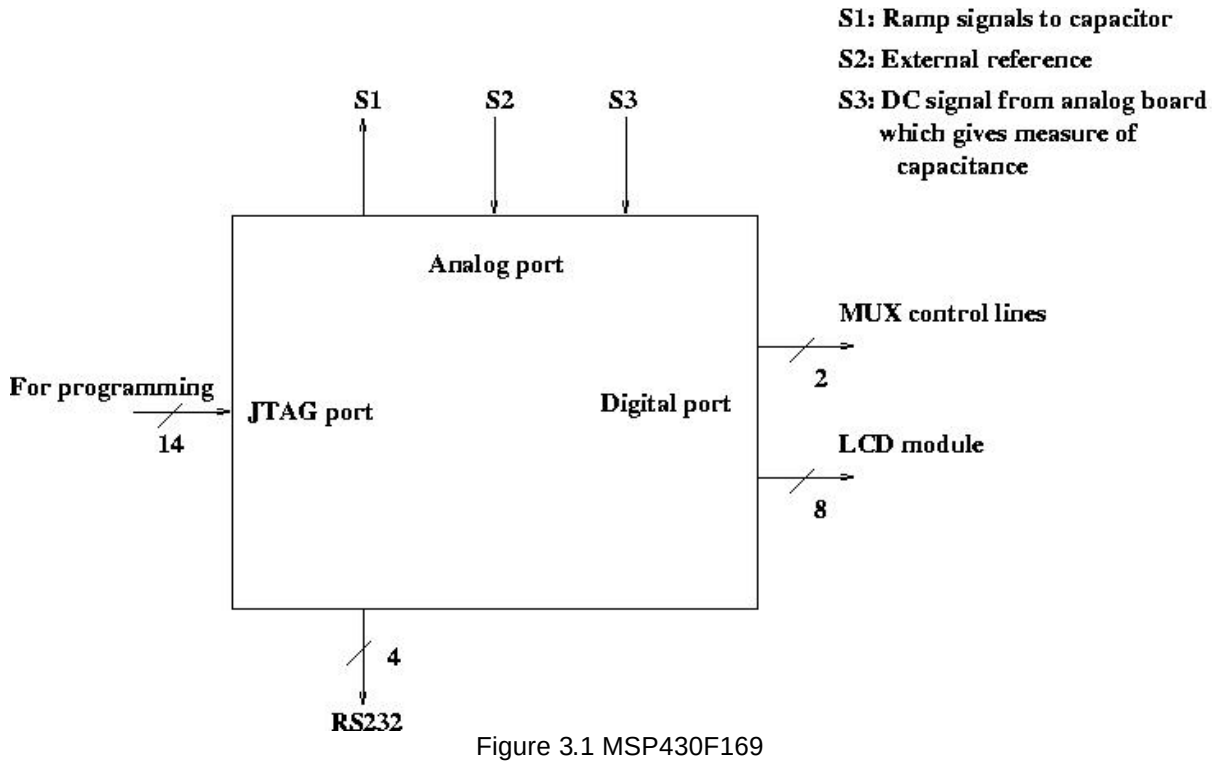

Figure 3.1 MSP430F169

4. JTAG interface

The JTAG connector is 2x7 pin with 0,1" step and TI recommended JTAG layout. The PIN.1 is marked with square pad on bottom and arrow on top. The purpose of the JTAG connector is to provide programming interface to the microcontroller.

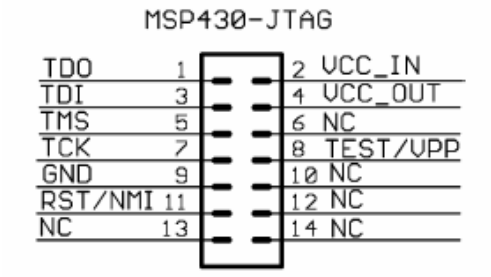

Figure 4.1 JTAG connector

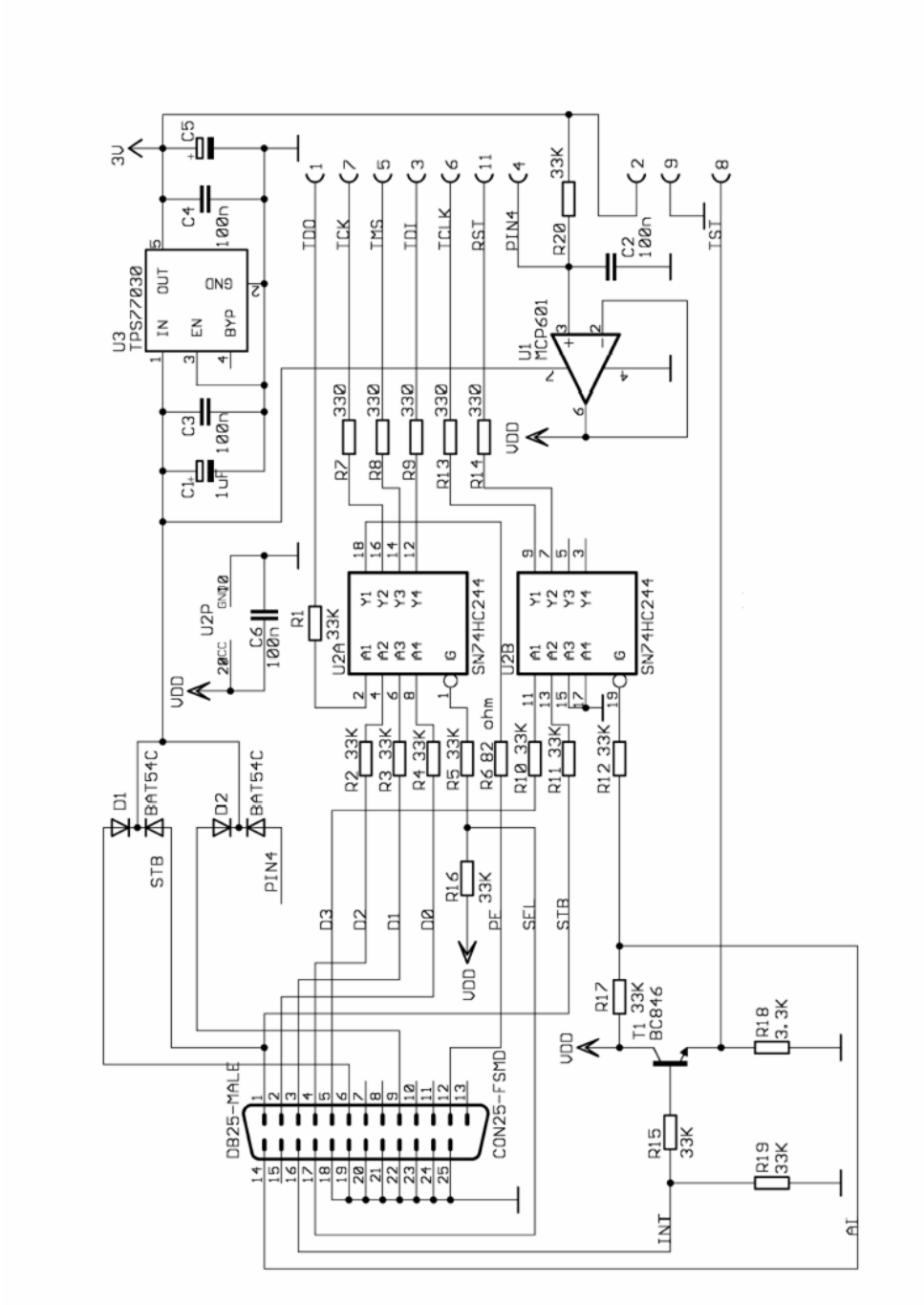

Fig 4.2 JTAG PCB layout

4.1 Target microcontroller voltage

MSP430-JTAG has build-in target board voltage follower and the JTAG voltage levels follow MSP430 target board voltage, so target may be powered with voltage between 2.7 and 3.6 V (if the target voltage is under 2.7V Flash memory can't be programmed)

5. USART Peripheral Interface, SPI Mode

The universal synchronous/asynchronous receive/transmit (USART) peripheral interface supports two serial modes with one hardware module.

In synchronous mode, the USART connects the MSP430 to an external system via three or four pins: SIMO, SOMI, UCLK, and STE. SPI mode is selected when the SYNC bit is set and the I2C bit is cleared.

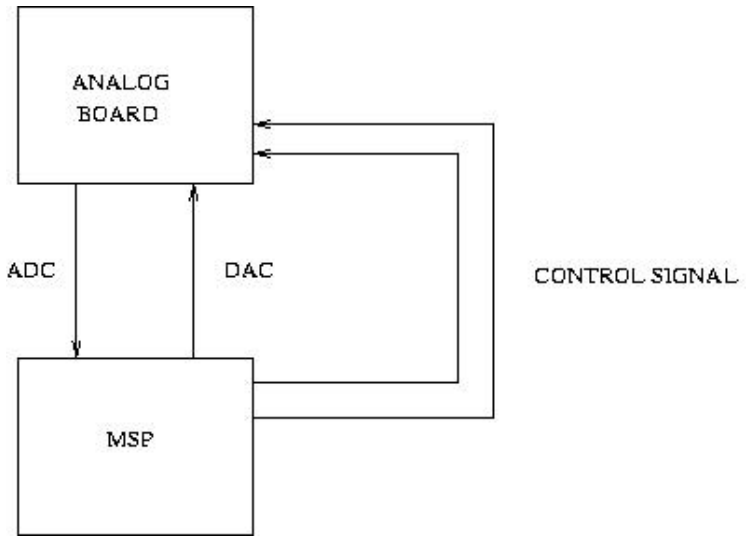

Figure 5.1 Data communication between the MSP and Analog boards

In the Figure 5.1 we communication between the MSP board and Analog board is shown. There are three signals:

1) DAC signal goes to the ramp generating circuit on the analog board. This circuit provides bias voltage to the EIS capacitor.
2) The output of the analog board is stored on the MSP bord through the ADC signal. In the C-V method this is transferred to the serial port. In the Concap method also, this is transferred to the serial port but its also fed back to converge the Vbias to mid-gap voltage.
3) The Control Signal is meant for frequency selection in UAF42, frequency generator, all pass filter and the low pass filter.

5.1 USART Operation: SPI Mode

In SPI mode, serial data is transmitted and received by multiple devices using a shared clock provided by the master. An additional pin, STE, is provided as to enable a device to receive and transmit data and is controlled by the master. Three or four signals are used for SPI data exchange:

1) SIMO: Slave in, master out
Master mode: SIMO is the data output line.
Slave mode: SIMO is the data input line.

2) SOMI: Slave out, master in
Master mode: SOMI is the data input line.
Slave mode: SOMI is the data output line.

3) UCLK: USART SPI clock
Master mode: UCLK is an output.
Slave mode: UCLK is an input.

4) STE: Slave transmit enable. Used in 4-pin mode to allow multiple masters on a single bus. Not used in 3-pin mode.

4-Pin master mode:

When STE is high, SIMO and UCLK operate normally.
When STE is low, SIMO and UCLK are set to the input direction.

4-pin slave mode:

When STE is high, RX/TX operation of the slave is disabled and SOMI is forced to the input direction.
When STE is low, RX/TX operation of the slave is enabled and SOMI operates normally.

5.1.1 USART Initialization and Reset

The USART is reset by a PUC or by the SWRST bit. After a PUC, the SWRST bit is automatically set, keeping the USART in a reset condition. When set, the SWRST bit resets the URXIEx, UTXIEx, URXIFGx, OE, and FE bits and sets the UTXIFGx flag. The USPIEx bit is not altered by SWRST. Clearing SWRST releases the USART for operation.

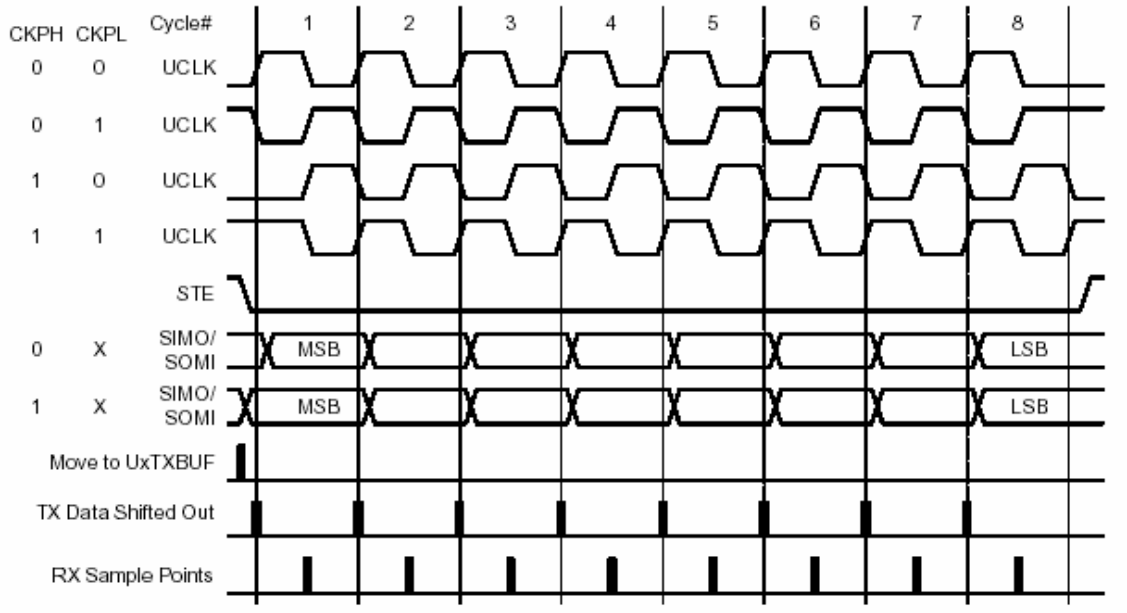

Figure 5.2 USART SPI Timing

6. ADC12

The ADC12 module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

6.1 ADC12 Operation

The ADC12 module is configured with user software.

6.1.1 12-Bit ADC Core

The ADC core converts an analog input to its 12-bit digital representation and stores the result in conversion memory. The core uses two programmable/selectable voltage levels (V_{R+} and V_{R-}) to define the upper and lower limits of the conversion. The digital output (N_{ADC}) is full scale (0FFFh) when the input signal is equal to or higher than V_{R+}, and zero when the input signal is equal to or lowers V_{R-}. The input channel and the reference voltage levels (V_{R+} and V_{R-}) are defined in the conversion-control memory. The conversion formula for the ADC result N_{ADC} is:

$$N_{ADC} = 4095(V_{in} - V_{R-})/(V_{R+} - V_{R-}) \quad (6.1)$$

The ADC12 core is configured by two control registers, ADC12CTL0 and ADC12CTL1. The core is enabled with the ADC12ON bit. The ADC12 can be turned off when not in use to save power. With few exceptions the ADC12 control bits can only be modified when ENC = 0. ENC must be set to 1 before any conversion can take place.

6.1.1.1 Conversion Clock Selection

The ADC12CLK is used both as the conversion clock and to generate the sampling period when the pulse sampling mode is selected. The ADC12 source clock is selected using the ADC12SSELx bits and can be divided from 1-8 using the ADC12DIVx bits. Possible ADC12CLK sources are SMCLK, MCLK, ACLK, and an internal oscillator ADC12OSC.

6.1.2 ADC12 Inputs and Multiplexer

The eight external and four internal analog signals are selected as the channel for conversion by the analog input multiplexer. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching as shown in Figure 6.1. The input multiplexer is also a T-switch to minimize the coupling between channels. Channels that are not selected are isolated from the A/D and the intermediate node is connected to analog ground (A_{VSS}) so that the stray capacitance is grounded to help eliminate crosstalk. The ADC12 uses the charge redistribution method. When the inputs are internally switched, the switching action may cause transients on the input signal. These transients decay and settle before causing errant conversion.

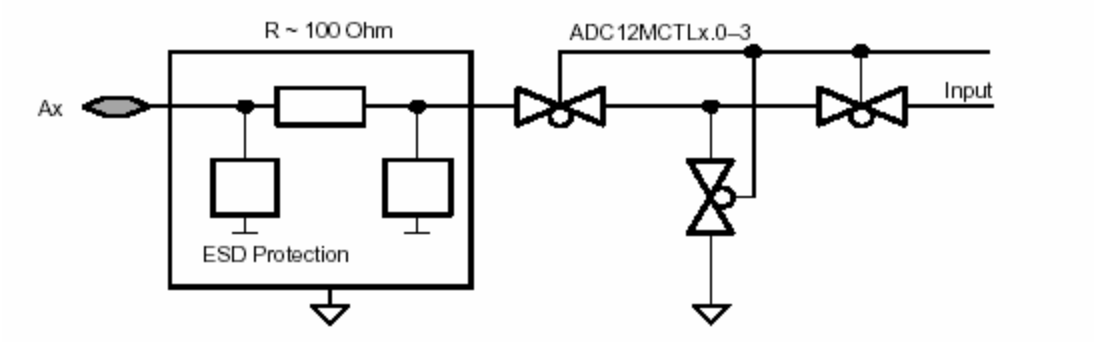

Figure 6.1 Analog Multiplexer

6.1.2.1 Analog Port Selection

The ADC12 inputs are multiplexed with the port P6 pins, which are digital CMOS gates. When analog signals are applied to digital CMOS gates, parasitic current can flow from V_{CC} to GND. This parasitic current occurs if the input voltage is near the transition level of the gate. Disabling the port pin buffer eliminates the parasitic current flow and therefore reduces overall current consumption. The P6SELx bits provide the ability to disable the port pin input and output buffers.

6.1.3 Voltage Reference Generator

The ADC12 module contains a built-in voltage reference with two selectable voltage levels, 1.5 V and 2.5 V. Either of these reference voltages may be used internally and externally on pin V_{REF+}. Setting REFON=1 enables the internal reference. When REF2_5V = 1, the internal reference is 2.5 V, the reference is 1.5 V when REF2_5V = 0. The reference can be turned off to save power when not in use. For proper operation the internal voltage reference generator must be supplied with storage capacitance across V_{REF+} and A_{VSS}. The recommended storage capacitance is a parallel combination of 10 µF and 0.1µF capacitors. From turn-on, a maximum of 17 ms must be allowed for the voltage reference generator to bias the recommended storage capacitors. If the internal reference generator is not used for the conversion, the storage capacitors are not required.

External references may be supplied for V_{R+} and V_{R-} through pins Ve_{REF+} and V_{REF-}/Ve_{REF-} respectively.

6.1.4 Sample and Conversion Timing

An analog-to-digital conversion is initiated with a rising edge of the sample input signal SHI. The source for SHI is selected with the SHSx bits and includes the following:

1. The ADC12SC bit
2. The Timer_A Output Unit 1
3. The Timer_B Output Unit 0
4. The Timer_B Output Unit 1

The polarity of the SHI signal source can be inverted with the ISSH bit. The SAMPCON signal controls the sample period and start of conversion. When SAMPCON is high, sampling is active. The high-to-low SAMPCON transition starts the analog-to-digital conversion, which requires 13 ADC12CLK cycles. Two different sample-timing methods are defined by control bit SHP, extended sample mode and pulse mode.

6.1.4.1 Extended Sample Mode

The extended sample mode is selected when SHP = 0. The SHI signal directly controls SAMPCON and defines the length of the sample period tsample. When SAMPCON is high, sampling is active. The high-to-low SAMPCON transition starts the conversion after synchronization with ADC12CLK. This is shown in Figure 6.2.

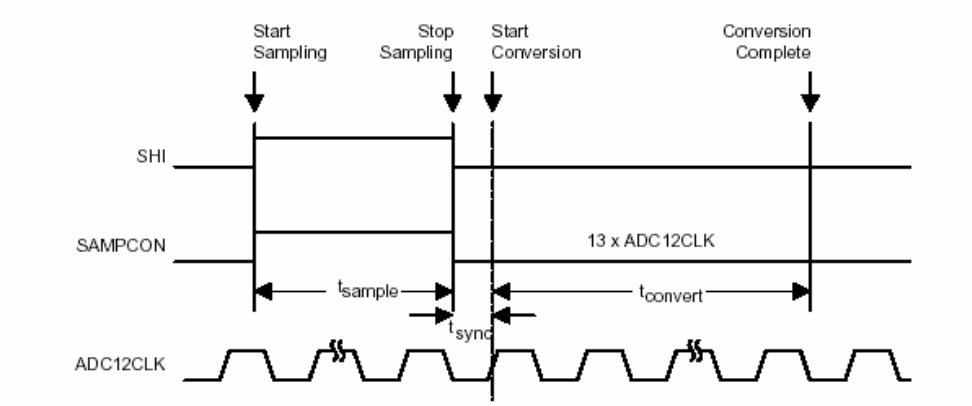

Figure 6.2 Extended Sample Mode

6.1.5 Conversion Memory

There are 16 ADC12MEMx conversion memory registers to store conversion results. Each ADC12MEMx is configured with an associated ADC12MCTLx control register. The SREFx bits define the voltage reference and the INCHx bits select the input channel. The EOS bit defines the end of sequence when a sequential conversion mode is used. A sequence rolls over from ADC12MEM15 to ADC12MEM0 when the EOS bit in ADC12MCTL15 is not set. The CSTARTADDx bits define the first ADC12MCTLx used for any conversion. If the conversion mode is single-channel or repeat-single-channel the CSTARTADDx points to the single ADC12MCTLx to be used. If the conversion mode selected is either sequence-of-channels or repeat-sequence-of-channels, CSTARTADDx points to the first ADC12MCTLx location to be used in a sequence. A pointer, not visible to software, is incremented automatically to the next ADC12MCTLx in a sequence when each conversion completes. The sequence continues until an EOS bit in ADC12MCTLx is processed - this is the last control byte processed. When conversion results are written to a selected ADC12MEMx, the corresponding flag in the ADC12IFGx register is set.

6.1.6 ADC12 Grounding and Noise Considerations

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.
Ground loops are formed when return current from the A/D flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small, unwanted offset voltages that can add to or subtract from the reference or input voltages of the A/D converter. The connections shown in Figure 6.3 help avoid this. In addition to grounding, ripple and noise spikes on the power supply lines due to digital switching or switching power supplies can corrupt the conversion result. A noise-free design using separate analog and digital ground planes with a single-point connection is recommended to achieve high accuracy.

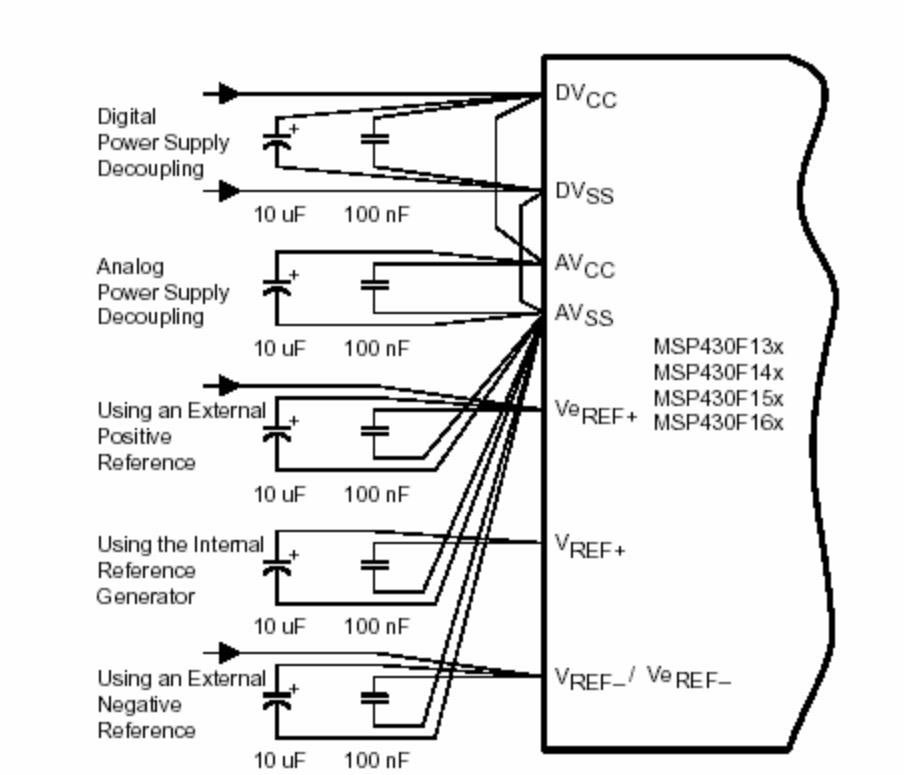

Figure 6.3 ADC12 Grounding and Noise Considerations

7. DAC12

The DAC12 module is a 12-bit, voltage output DAC. The DAC12 can be configured in 8- or 12-bit mode and may be used in conjunction with the DMA controller.

7.1 DAC12 Operation

The DAC12 module is configured with user software.

7.1.1 DAC12 Core

The DAC12 can be configured to operate in 8- or 12-bit mode using the DAC12RES bit. The full-scale output is programmable to be 1x or 3x the selected reference voltage via the DAC12IR bit. This feature allows the user to control the dynamic range of the DAC12. The DAC12DF bit allows the user to select between straight binary data and 2's compliment data for the DAC. When using straight binary data format, the formula for the output voltage is given in Table 7.1.

Resolution	DAC12RES	DAC12IR	Output Voltage Formula
12 bit	0	0	$Vout = Vref \times 3 \times \frac{DAC12\_xDAT}{4096}$
12 bit	0	1	$Vout = Vref \times \frac{DAC12\_xDAT}{4096}$
8 bit	1	0	$Vout = Vref \times 3 \times \frac{DAC12\_xDAT}{256}$
8 bit	1	1	$Vout = Vref \times \frac{DAC12\_xDAT}{256}$

Table 7.1 DAC12 Full-Scale Range (Vref = $Ve_{REF}+$ or $V_{REF}+$)

In 8-bit mode the maximum useable value for DAC12_xDAT is 0FFh and in 12-bit mode the maximum useable value for DAC12_xDAT is 0FFFh. Values greater than these may be written to the register, but all leading bits are ignored.

7.1.2 DAC12 Port Selection

The DAC12 outputs are multiplexed with the port P6 pins and ADC12 analog inputs.When DAC12AMPx > 0, the DAC12 function is automatically selected for the pin, regardless of the state of the associated P6SELx and P6DIRx bits.

7.1.2.1 DAC12 Reference

The reference for the DAC12 is configured to use either an external reference voltage or the internal 1.5-V/2.5-V reference from the ADC12 module with the DAC12SREFx bits. When DAC12SREFx = {0,1} the V_{REF+} signal is used as the reference and when DAC12SREFx = {2,3} the Ve_{REF+} signal is used as the reference. To use the ADC12 internal reference, it must be enabled and configured via the applicable ADC12 control bits. Once the ADC12 reference is configured, the reference voltage appears on the V_{REF+} signal.

8. Power Supply

We are using a single 6V battery operated power supply. We are using low dropout regulators for this purpose. We are using TPS7350 for generating + 5 V, TPS7333 for generating + 3.3 V and LT1054 for generating - 5 V.

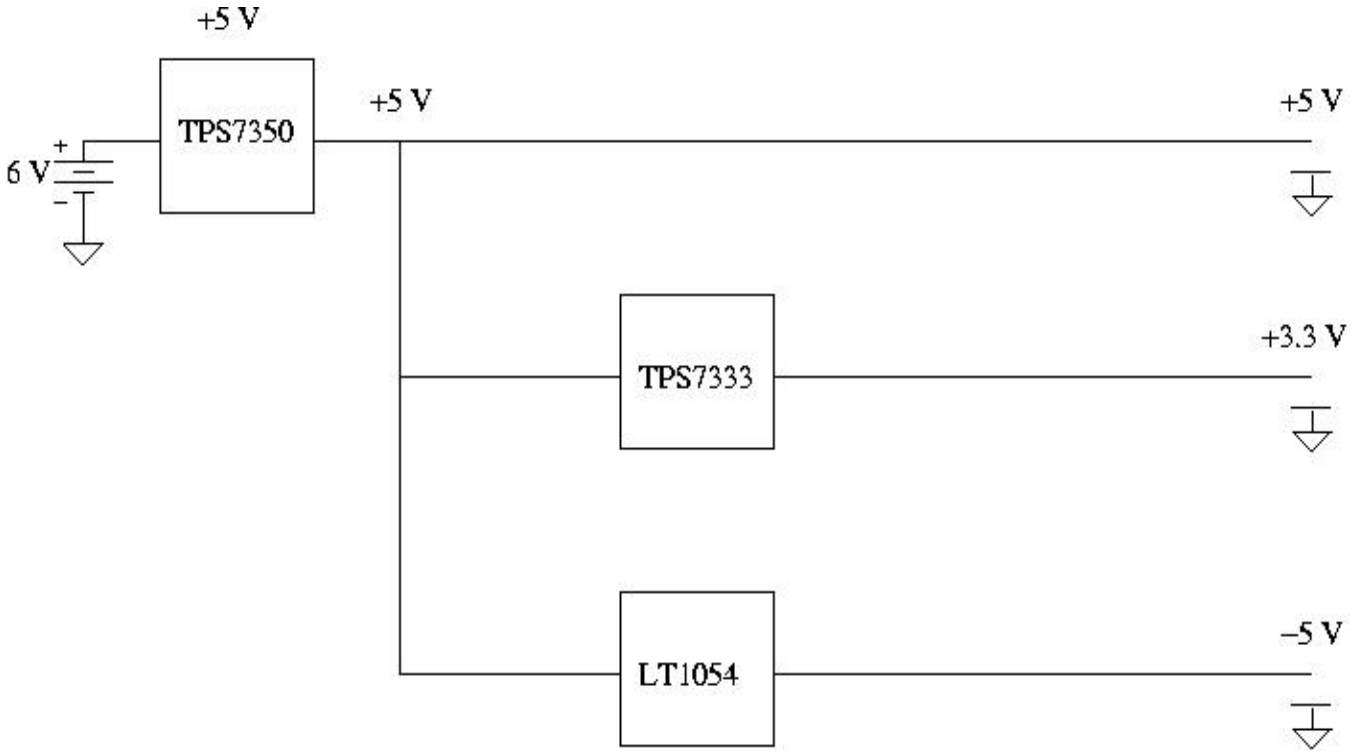

Figure 8.1 Power supply using 6V battery

References

1. Horowitz P, Hill W. *Art of Electronics,* Second Edition, Cambridge University Press, 1995.
2. Sedra A S, Smith K C, *Microelectronic Circuits,* Fourth Edition, Oxford University Press, 1999
3. Sydenham P H, *Handbook of Measurement Science,* Vol 1
4. Elson J, *PARAPIN: A Parallel Port Pin Programming Library for Linux*. University of Southern California, March 2000
5. *Analog Design Application Manual,* Analog Devices, *http://www.analog.com*
6. Datasheets from Intersil, Texas Instruments and National Semiconductors

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