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Wireless Network Camera

Group: D1
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Abstract

The report discusses the approach, design and implementation of a Wireless Network Camera (WNC). The project aims at developing a WNC which would be capturing the images in real time and transferring them to a PC over a wireless network using the 802.11g, WiFi protocol. The project comes out with a 2.5inch x 3inch network camera unit. The report explains how a raw image data is captured by a CMOS sensor, interfacing of the sensor with Blackfin DSP processor (BF533) where a real-time MPEG encoding can be done and after which the TCP/IP stack can be added to send the data over WLAN. The received images then can be viewed by any MPEG decoder.

1. Introduction

The project mainly aims to develop a board having a micron lense, a DSP based microprocessor (BF533), an SDRAM, a flash and a Wlan module. The report describes how these five modules have been interfaced faced with each other. The circuitry works with a 25MHz clock. The DSP processes take place at 600MHz. Thus for the tracks on the designed PCB which interface flash and processor, RAM and processor, sensor and processor special care have been taken. These are described in the section 5 of the report. The board designed is a 4 layer, 75mm x 63mm in size. Sample codes have been written to test the working of SDRAM, flash and the Micron sensor. These are described in section 6 of the report.

2. Block Diagram

Figure 1 shows the block diagram of the WNC.
The circuit comprises of mainly the following components:-

1. Blackfin (BF533) processor
2. SDRAM (256Mb)
3. Flash (8Mb)
4. Micron image sensor
5. Micron camera connector
6. Wlan module

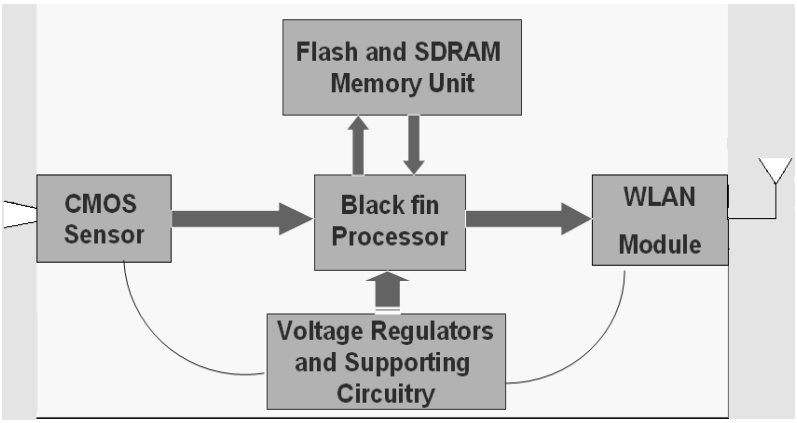

Figure 1: Block Diagram

3. Circuit Description

3.1. Camera sensor and connector (Micron circuitry): The micron camera sensor (MT9V111) is connected to the camera connector. The camera sensor captures the image and sends it to the parallel port interface of BF533. The camera sensor is given a clock of 25 MHz and supply of 2.8V. It captures the images at 640 x 480 resolutions and at 27-30 fps. It gives the digital data to the PPI of BF533.

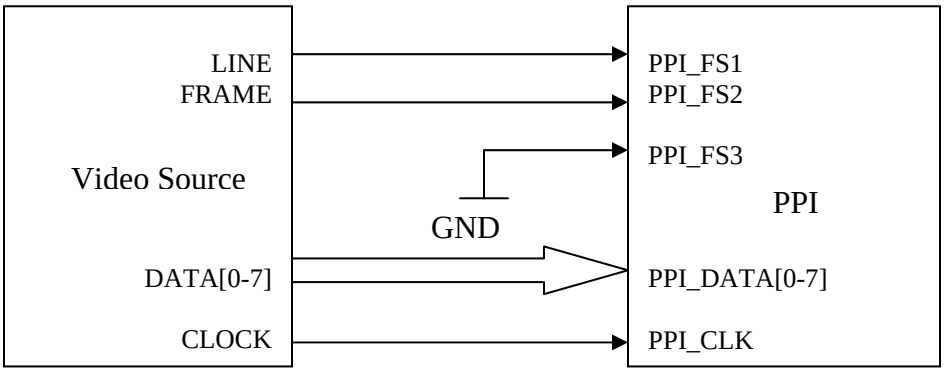

Figure 2: Interfacing Micron image sensor and BF533's PPI

The MT9V111 has a pixel array of 782 columns by 492 rows. The leftmost 26 columns and top eight rows are optically black and can be used to monitor the black level. The image data in progressive scan mode by BF533. The amount of vertical and horizontal blanking is programmed by the two wire interface SDA and SCL which are connected to BF so that they can be programmed by the processor itself.

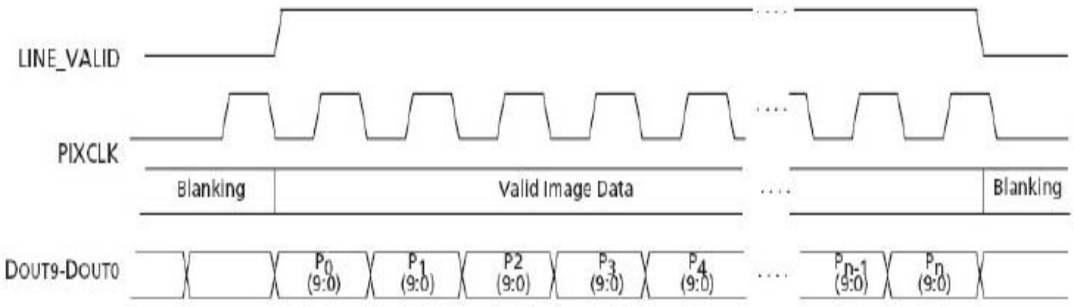

Figure 3: Output Data timing

The image data is an 8 bit datum which is interfaced to the PPI of BF. This datum is synchronized with the pixel clock which is also supplied to BF533. The LINE_VALID signal is high for the 8 bits of data and when it becomes low it indicates the valid line data. Similarly FRAME_VALID signal is high for the whole frame and when it becomes low it indicates the end o f the previous frame and beginning of a new frame.

These LINE_VALID and FRAME_VALID lines are input to the frame synchronization pins of BF533 in addition to the pixel clock.

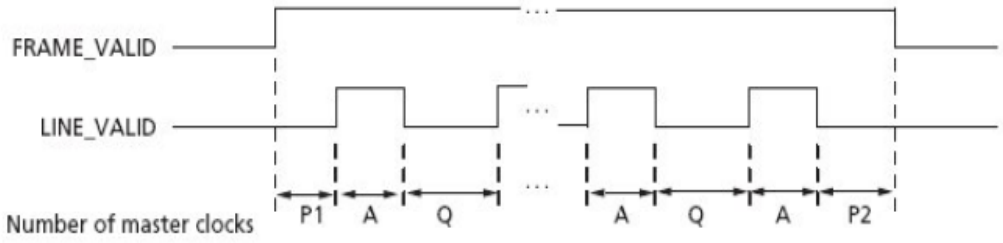

Figure 4: Frame Valid Timing

3.2. SDRAM: The processing of data takes place in the RAM of this circuitry. The 128MB SDRAM is quad bank DRAMs operating at 3.3V and are synchronous in nature. All signals are registered on positive edge of the clock. This clock is supplied by BF533. The SDRAM operates in word mode and hence each of the x16's 33,554,432 bit banks is organized into 4096 rows by 512 columns by 16 bits.

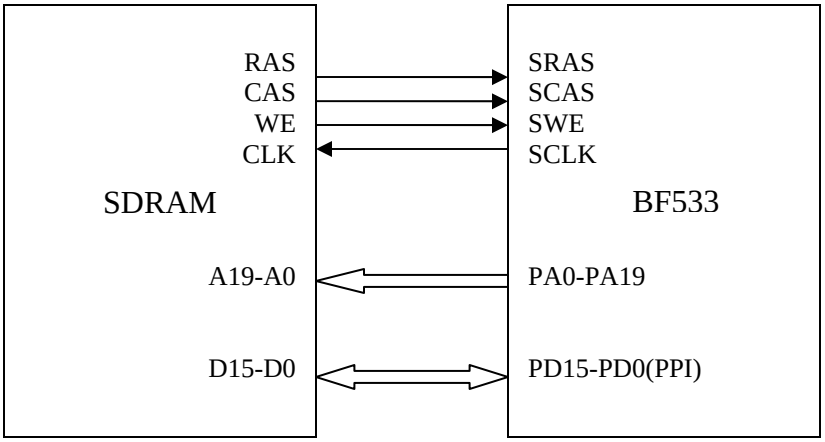

Figure 5: SDRAM interfaced with BF533

Read and write accesses to the SDRAM are burst oriented accesses; start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by READ or WRITE command. The RAS, CAS and WE lines of SDRAM are interfaced with SRAS, SCAS and AWE of BF533. The address lines of SDRAM are interfaced with PA1-PA19 lines on blackfin. The data lines are interfaced with PD0-PD15 data lines i.e. PPI data pins of BF533. The clock provided to RAM is through the SCLK pin of BF533.

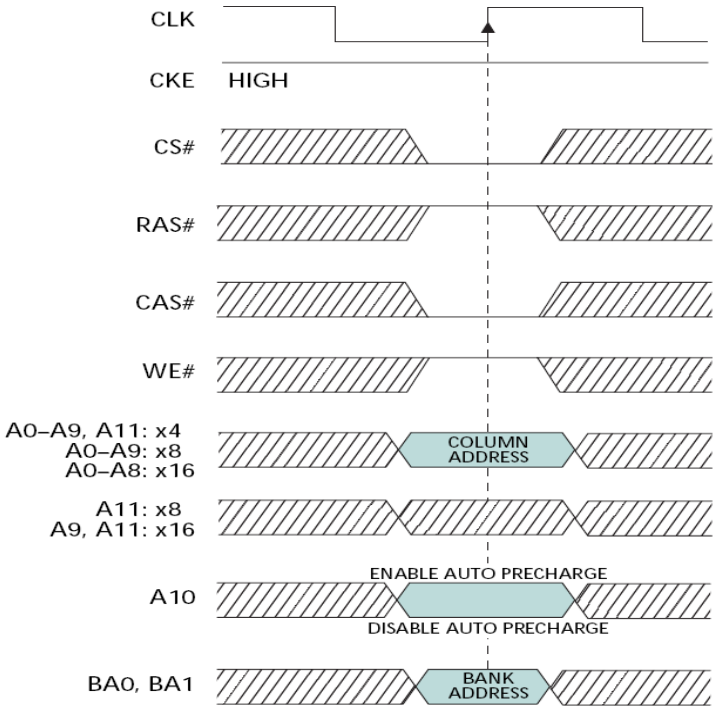

Figure 6: Timing of signals in SDRAM for READ command

The address bit registered coincident with the active command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0-A11 select the row).The address bits registered coincident with the read or write command are used to select the starting column location for the burst address.

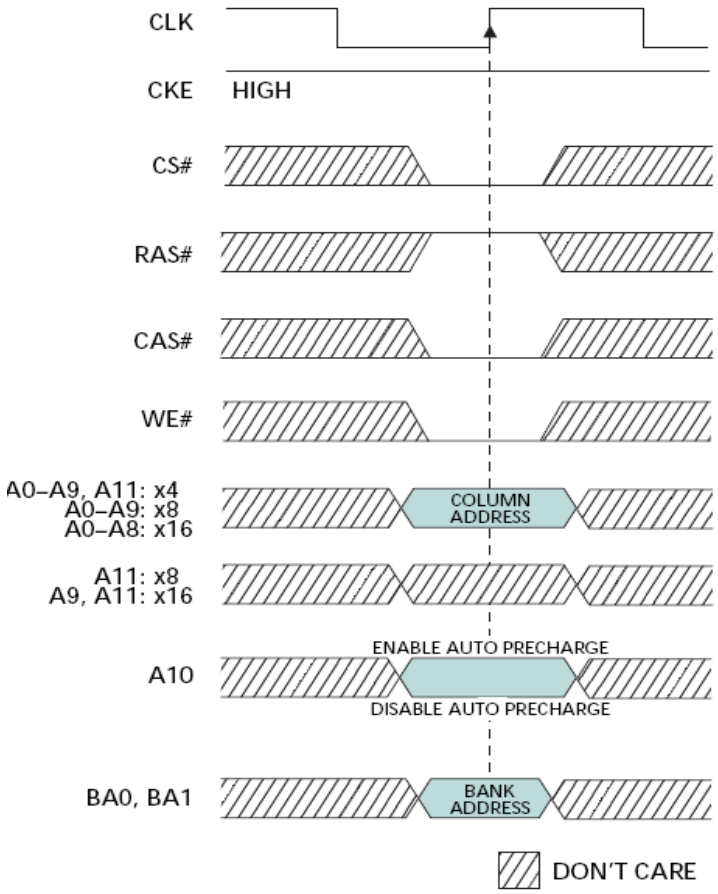

Figure 7: Timing of signals in SDRAM for WRITE command

The signals for the read and write commands corresponding to the clock and data are shown in figures 6 and 7 respectively.

3.3. Flash: Flash is used so that a dxe (executable for a DSP processor) can be loaded into it and the board can directly be booted by just supplying power to it. The flash in interfaced with the blackfin according to Figure 8.

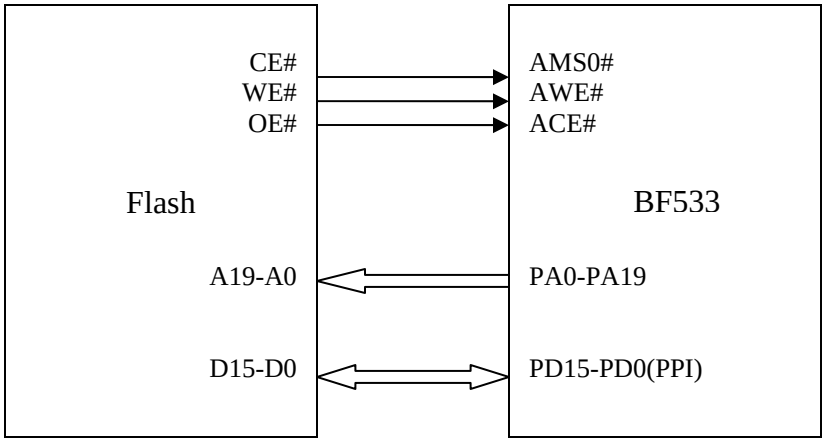

Figure 8: Interfacing Flash with BF533

Flash is asynchronous in nature. The BYTE# is used to indicate whether flash is used in word mode or byte mode. As of in our case it is used in word mode and is set high. The CE#, OE#, WE# signals are used to interface it with blackfin's AWE, AOE, AMSO pins which are used in reading and writing operations. The address pins of flash are interfaced with the same PA1-PA19 pins of blackfin as was in the case of sdram but which chip is selected is done with the help of chip select operation. Also the data pins of flash are connected with the PD0-PD15 pins i.e. the PPI of blackfin. The A19, A20 and A21 pins of flash are pulled high through 1Kohm resistor to avoid them being in tri state when the board would be reset.

3.4. WLAN Module: The image data after being captured by micron image sensor is sent to Blackfin processor. This is raw image data. To view the data on LAN TCP–IP stack needs to be added to the above data. Indeed the image data can also be encoded in a particular format in real time (this processing would take place by the utilization of RAM) so that the data can be compressed and TCP-IP stack is now added over this data and sent to WLAN module. The WALN module also contains an antenna and the data is transmitted using 802.11 g protocol at 2.4GHz. The image can now be viewed by any Wi-Fi enabled decoder in real time. The WLAN module makes use of Marvell chipset.

4. Schematic

The schematic is attached in the Appendix II at the end of the Report. Page 1 in the schematic contains Flash, SDRAM, Black fin, USI connector, micron connector and JTAG. Page 2 contains all the voltage regulators and the decoupling circuitry.

The schematic was completely designed in Orcad. After the completion of the schematic an *ascii* file was generated which was later made use of while making the layout.

5. PCB layout

After the completion of the schematic now comes the layouting part. We first fixed the size of the PCB to 2.5 inch X 3 inch and then the started the layouting procedure. We also figured out that in order to make a board of this dimension it will take at least 4 layers to successfully include all the components and routes

5.1 Making the footprints: All the footprints were designed by us. Mechanical details of all the components were studied from their respective datasheets and then after doing the required calculations footprints were made. All the footprints were checked many times.

5.2 Component Placement: Few things that we have taken care of while placing the components are:

- All the LED's and connectors are on the vertical edges of the board
- All the decoupling capacitors are on the bottom layer
- SDRAM is at the minimum possible distance from the Blackfin
- No passive components are between WLAN module and Blackfin
- Voltage regulators are placed one after the other such that the lower voltages follow the higher ones 5V->3.3V->2.8V->1.2V

5.3 Layer stack up: The layer stack up is as follows:

Layer 1	Top Layer
Layer 2	Power Layer
Layer 3	Ground Layer
Layer 4	Bottom Layer

Table 1: Layer Stack up

The PCB is a 50 Ohm impedance board and accordingly the following stacks up details have been used with 5 mil clearance and 5 mils track width.

>Layer 1: 18+25 microns copper
> Dielectric- 0.36mm
> CCL 0.8mm (including 35 micron copper each side)
> Dielectric-0.36mm
>Layer 4 18+25 microns copper
> Total nicle-1.6mm

5.4 Routing: While routing things that have been taken care of are:

- The entire routing is manual.
- Minimum track width and clearance of 5 mils is used.
- Vias of three different diameters 16 mils, 18 mils and 32 mils with respective drill sizes 8 mils, 8 mils and 16 mils have been made use of depending upon the use.
- First address lines routing is done from Blackfin to SDRAM and then from SDRAM they are taken to Flash.

- No routing was done in the Power and ground layers. Instead power planes were made below Blackfin, Voltage regulators and the Oscillator.
- Length matching of address lines was done.
- 8 test points have also been included.

The complete PCB layout and the photo plots obtained after releasing the gerber have been attached in Appendix III and IV respectively.

6. Software

The aim of software part of our EDL project was to test the individual components of our board which included SDRAM, Flash, and Micron Sensor and WLAN module.

6.1 PLL Settings: Firstly we installed VDSP++ on our EMP01 set up in our SPANN lab and changed the core and system clock of Blackfin dynamically through the PLL settings to make the processes faster. The core clock frequency was made 600 MHz whereas the system clock frequency was set to 120 MHz. For this we used a 25 MHz crystal oscillator which provided the clock in frequency.

6.2 SDRAM Test: Then, the wait states were loaded on Blackfin to configure it for carrying out tests on SDRAM, Flash etc. We performed the 55 & AA tests on SDRAM after initializing the control registers. In 55 tests we wrote a pattern 55 on all memory locations and then XORed it with ff to get AA on all memory locations through our code. Similarly we did the AA test but with initial pattern as AA instead of 55.These tests proved that all the memory locations of SDRAM are fine and the Blackfin processor could write and store values on them.

6.3 Flash Test: For Flash we did the flag settings and configured control registers to enable us to read write and erase data on flash memory. Firstly the flash memory was completely erased and then 16 bits data was written on flash with memory space extending from 0x0 to 0xffffff and then successfully read. This completed our flash test as we could successfully perform the erasing, writing and reading operations on it.

6.4 Micron Image Sensor Test: The test for Micron sensor involved capturing video and storing data in raw format on SDRAM and viewing it using the image view tool of VDSP++. Firstly, we configured SDRAM registers in sdram_wait.c. Then, we configured system to unmask PPI interrupts in the function PPI_DMA_Interrupt_Set. After this the DMA channel 0 was enabled for PPI. It was configured to dump captured data on SDRAM (starting address 0x0).The DMA is set as a 2D array with counts of X & Y as number of horizontal and vertical pixels with stride 2.Then finally PPI interface was enabled in the function PPI_Interface_Enable. Here input buffers on flag were enabled and control register of PPI is configured for 3 frame syncs.

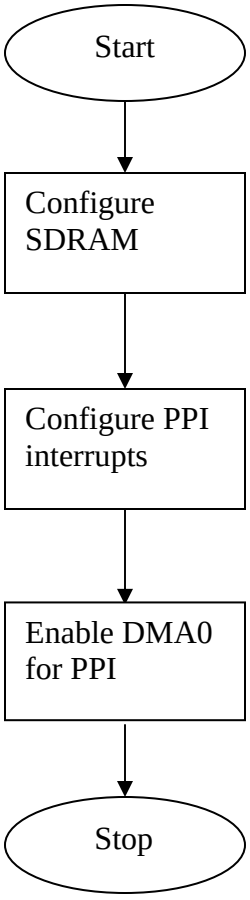

Figure 10: Program Flow Diagram for Micron Sensor

7. Conclusion

Circuit for the Wireless Network Camera is correctly designed and checked. A 4 layer PCB is also successfully made. We have also made diagnostics for SDRAM, Flash and the Micron Camera. All the codes are successfully tested on the board.

Video in real-time has been successfully transferred on WLAN. The delay in video can be improved making more efficient MPEG encoding and decoding algorithms.

7. Future Plans

The processor can be replaced with a more power full, dual core (BF561) processor. Also an RC remote can be interfaced with the UART of the processor which can switch the board on and off. After the camera is placed at a certain location remote can also be used to rotate it so that it can scan the surroundings over the entire range of elevation and azimuth of 0^{o}-360^{o}. The DC-jack footprint should be changed so has to have the jack horizontal rather than vertical. A fish eye lense having very high resolution can be interfaced with the processor instead of the present lense. In software, efficient codes can be written which can capture the images in real time and transfer them over a wireless network with minimal amount loss.

Acknowledgement

We would like to express our deep sense of gratitude to Professor C. P. Mammen, Professor P.C. Pandey, Professor U. B. Desai, Professor L.R Subramanian, Mr. Nalesh Shivnandan, Mr. Akshay Mishra, Mr. Vijay and Mr. Qutubuddin Saifee for their guidance and valuable suggestions throughout the course of the project.

References

[1] "Datasheet of ADSP BF533", Analog Devices, http://www.analog.com. Last accessed on 30th Oct. 2006

[2] "Micron MT9V111 CMOS sensor details", Micron, http://download.micron.com/pdf/datasheets/imaging/MT9V111.pdf. Last accessed on 30th Oct. 2006

[3] "Datasheet for Flash", Spansion, www.spansion.com/datasheets/25974b4.pdf. Last accessed on 30th Oct. 2006

[4] "Datasheet of SDRAM", Micron, http://www.micron.com/dram. Last Accessed on 30th Oct. 2006

[5] "Visual DSP Tutorial", Analog Devices, www.analog.com/UploadedFiles/Associated_Docs/4365032078788740_get_started_guide.pdf. Last accessed on 30th Oct. 2006

Appendix I
Bill of materials

S.No	Part	Description	Qty	Part No.	Reference
1.	10NF	CAP,10NF 50V 10% SMD 0402	28	C0402C103K5RAC	C1,C2,C3,C4,C5,C6,C7,C8,
					C15,C16,C17,C18,C19,C20,C21,
					C22,C23,C24,C25,C26,C30,
					C31,C32,C33,C34,C35C40,
					C41
2.	22UF10V	CAP,22UF 10V10% SMD 6032	6	T495C226K010AS	C10,C13,C14,C27,C38,C39
3.	100NF	CAP,100NF 50V 10% SMD 0402	1	C0402C104K5RAC	C12
4.	1UF	CAP,1UF 50V 10% SMD 0402	2	C0402C105K5RAC	C9,C11
5.	1UF16V	CAP,TANT 1uF16V 10%, SMD 6032	2	T491C105K016AS	C29,C28
6.	10UF16V	CAP,TANT 10uF16V 10%, SMD 6032	2	T491C106K016AS	C36,C37
7.	LED	Red Diffused, through hole LED [small 3mm]	3	P363-ND	DS1,DS2,DS3
8.	1N4148	Thru. Hole DIODE 1N4148DICT-ND DO-35	1	1N4148DICT-ND	D1
9.	SMB5817	SMD Diode, Max. Peak Reverse Voltage 20V, DO-214AA 1 Amp Schottky Rectifier — SMT	1	SMB5817MSCT-ND	D2
10.	DIGICAM_1	24 Pin connector for micron digital camera	1	XF2H-2415-1	J1
11.	DC JACK	RAPC742 PC mount, 1mm pin, Power Jack	1	RAPC742	J2
12.	JTAG_HEADER	Breakaway Headers Unshrouded Double Row, .100 X .100 Centers. Connector 14Pins (7X2)	1	103783-7	P1
13.	10KOHMS	RES, 10 KOHMS,5% SMD 0402	3	TNPW 0402 103 JT-1	R1,R2,R3
14.	0 OHMS	RES, 0 OHMS,5% SMD 0402	10	TNPW 0402 000 JT-1	R4,R5,R28,R29,R30,R31,R32,
					R33,R34,R35
15.	4K7OHMS	RES, 4.7 KOHMS,5% SMD 0402	15	TNPW 0402 472 JT-1	R9,R10,R11,R12,R13,R14,R15,R16,
					R17,R18,R19,R20,R21,R22,R24
16.	22 OHMS	RES, 22 OHMS,5% SMD 0402	3	TNPW 0402 220 JT-1	R37,R38,R39
17.	1KOHMS	RES, 1 KOHMS,5% SMD 0402	3	TNPW 0402 102 JT-1	R6,R7,R8

18.	470OHMS	RES, 470 OHMS,5% SMD 0402	3	TNPW 0402 471 JT-1	R25,R26,R27
19.	33 OHMS	RES, 33 OHMS,5% SMD 0402	1	TNPW 0402 330 JT-1	R23
20.	20KOHMS	RES,20 KOHMS,5% SMD 0402	1	TNPW 0402 203 JT-1	R36
21.	PRESS _SWITCH	PRESS SWITCH (4 pin small)	1	P1102S	SW1
22.	TPS	Surface mount test points	8		TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8
23.	ADSP21531/32/33	ADSP-21533, 160-LEAD METRIC PLASTIC BALL GRID ARRAY (MINI-BGA)	1	ADSP-BF33SKBC-600	U1
24.	AM29LV640MT	Am29LV640MT, 48 PINS TSOP 64 Megabit (2 M x 8-Bit/1 M x 16-Bit) 3.0 Volt-only, Mirror bit Flash Memory	1	AM29LV640MT-110REI	U3
25.	128MBSDRAM	MT48LC16M16A2TG-7E TSOP 54Pins 128Megabits SDRAM	1	MT48LC16M16A2TG-75D	U2
26.	P5K connector	Narrow Pitch(.5 mm) connectors P5 series 60 pin socket	1	AXK5F60345J	U4
27.	ADP3339_3.3	5V to3.3V 1.5A , Low Dropout regulator, SOT-223 package	1	ADP3339AKC3.5	U5
28.	ADP3339_285	3.3V to 2.85V 1.5A , Low Dropout regulator, SOT-223 package	1	ADP3339AKC-2.85	U6
29.	LM317	LM317 1.5A 3-Terminal Adjustable Regulator TO263 package	1	LM317S	U7
30.	OSC25MHZ_H	OSC 25 MHz, Ceramic SM TYPE, 3.3Volts	1	CSX750PBB25MB	Y1

Table 2: Bill of materials

Appendix II
Schematics

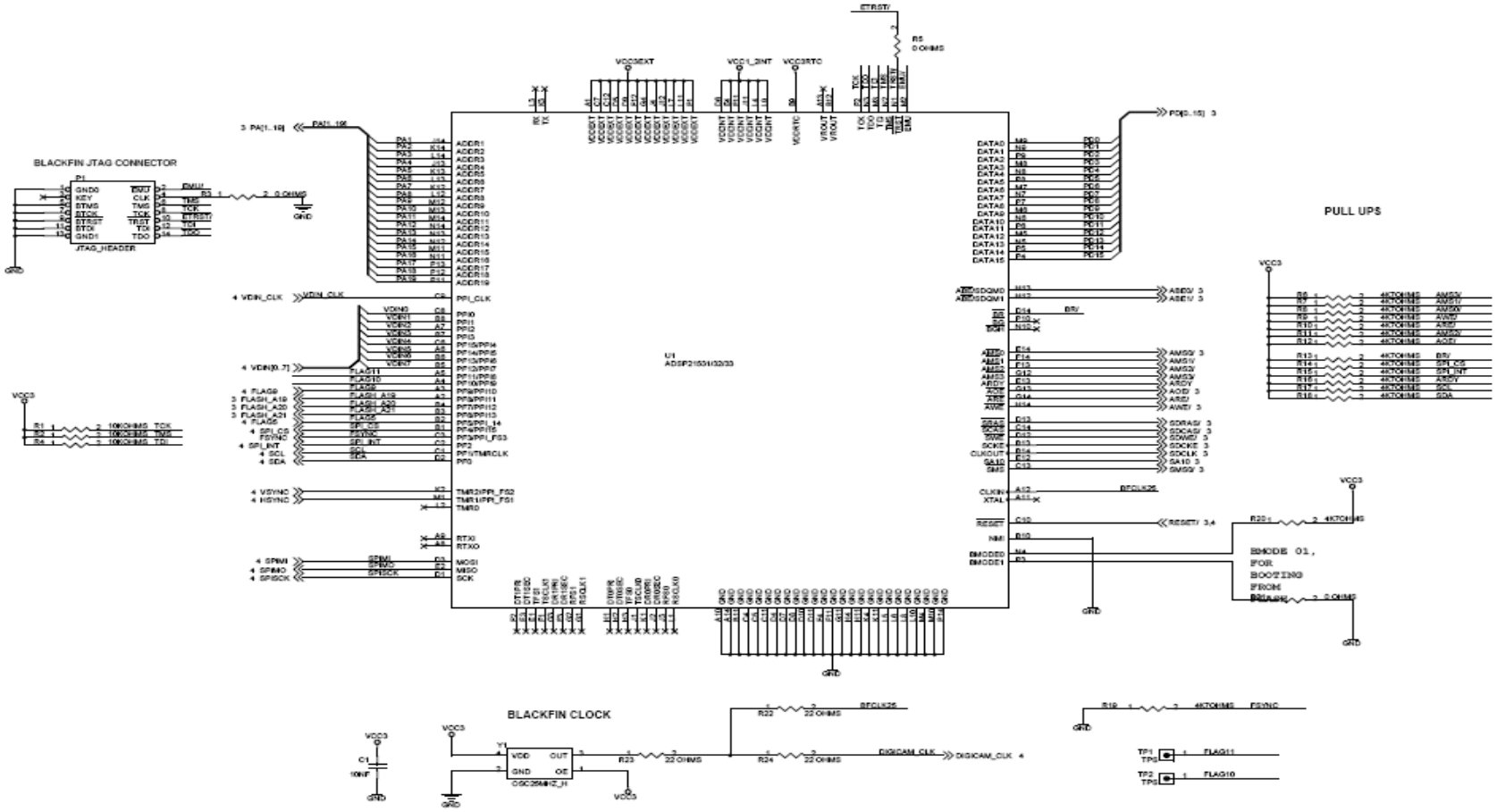

Figure 10: Schematic (Page1)

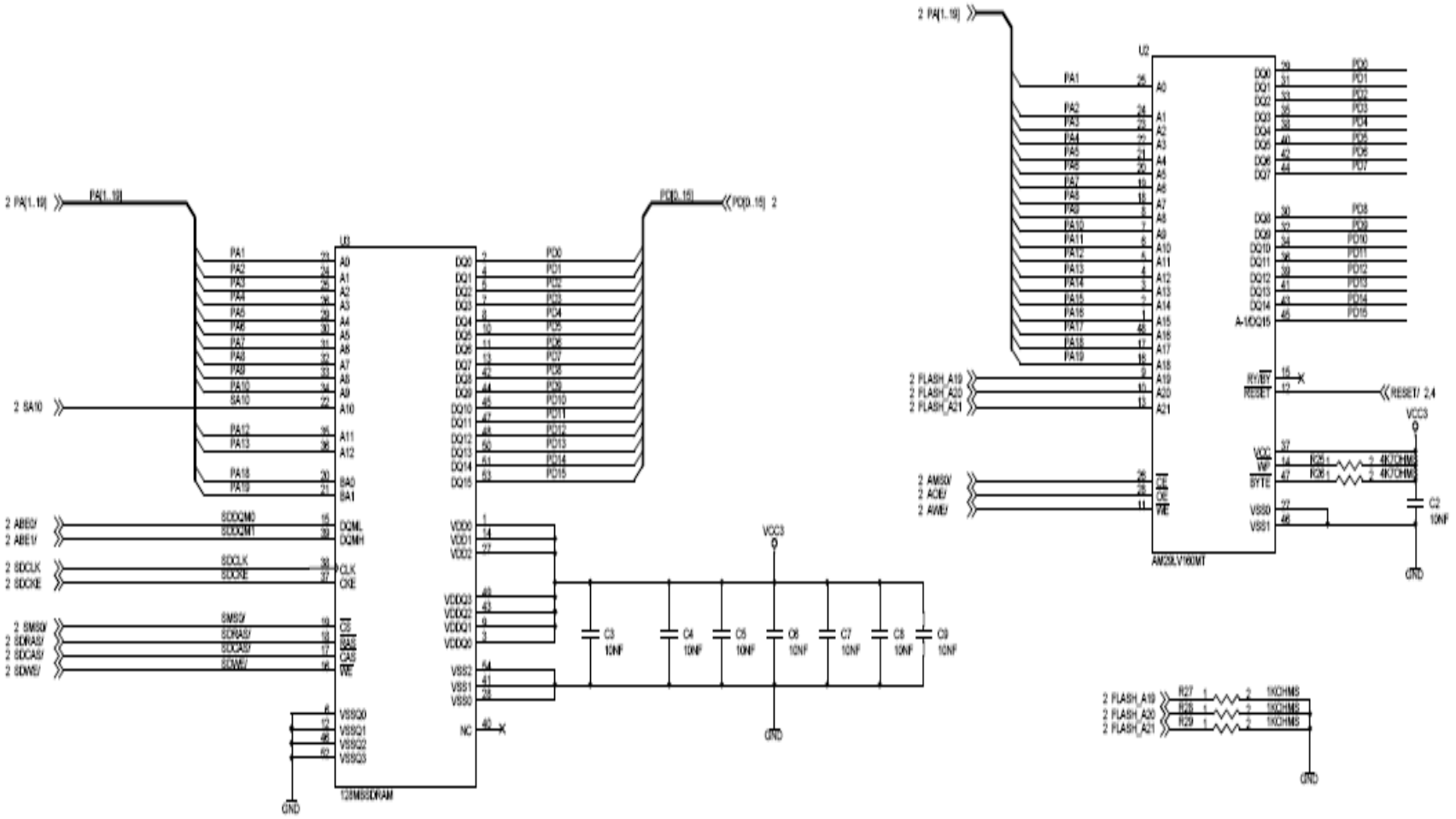

Figure 11: Schematic (Page2)

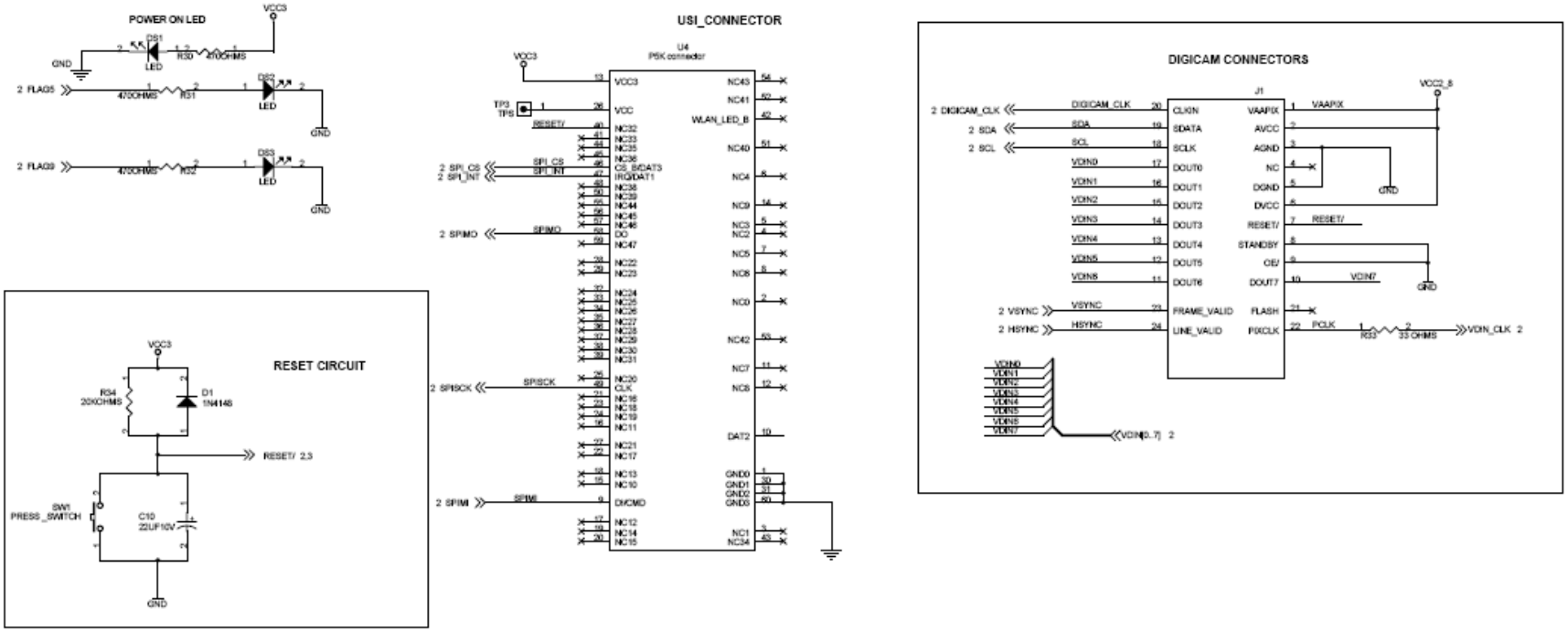

Figure 12: Schematic (Page3)

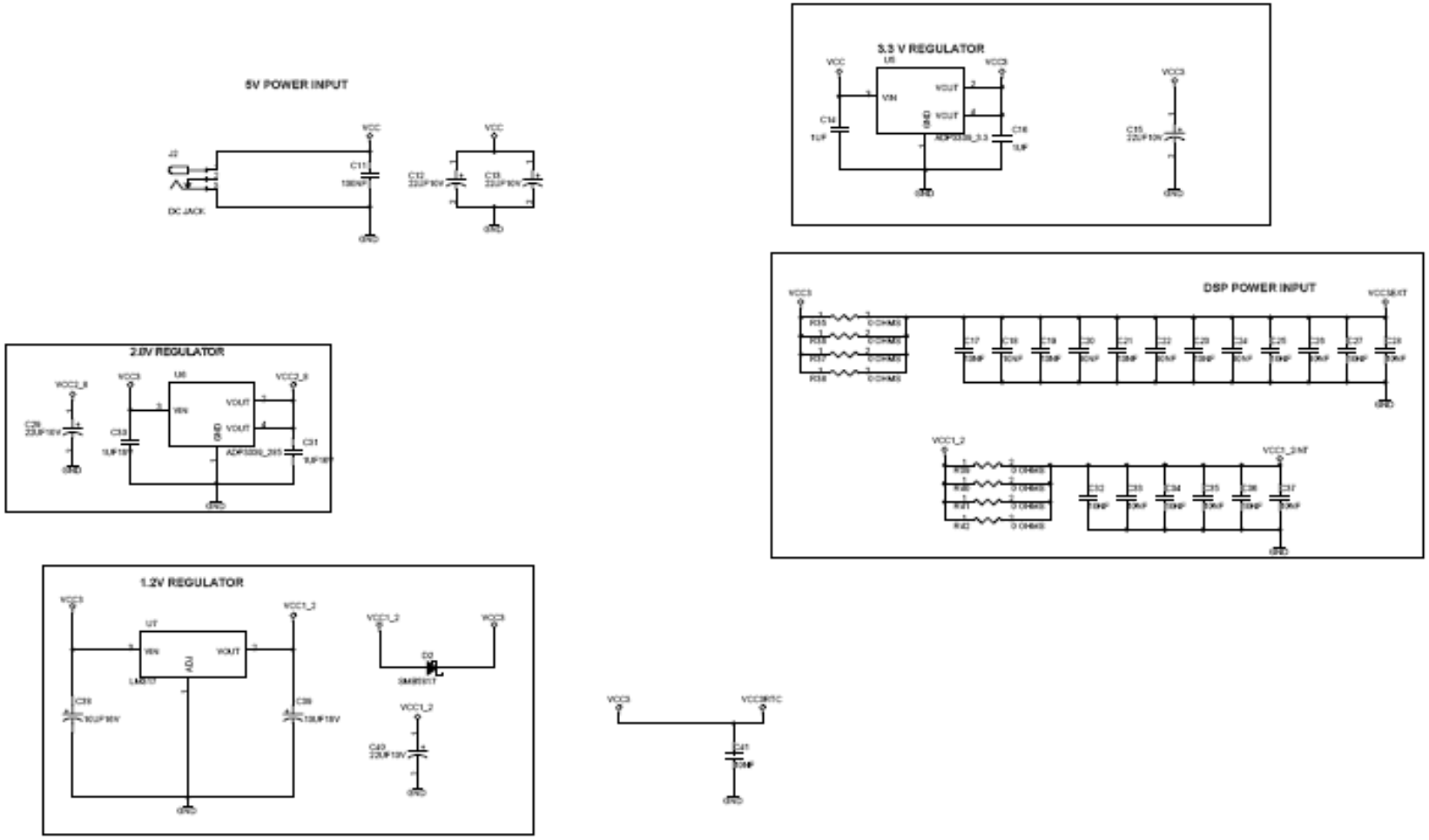

Figure 13: Schematic (Page 4)

Appendix III
PCB Layout with completed Routes

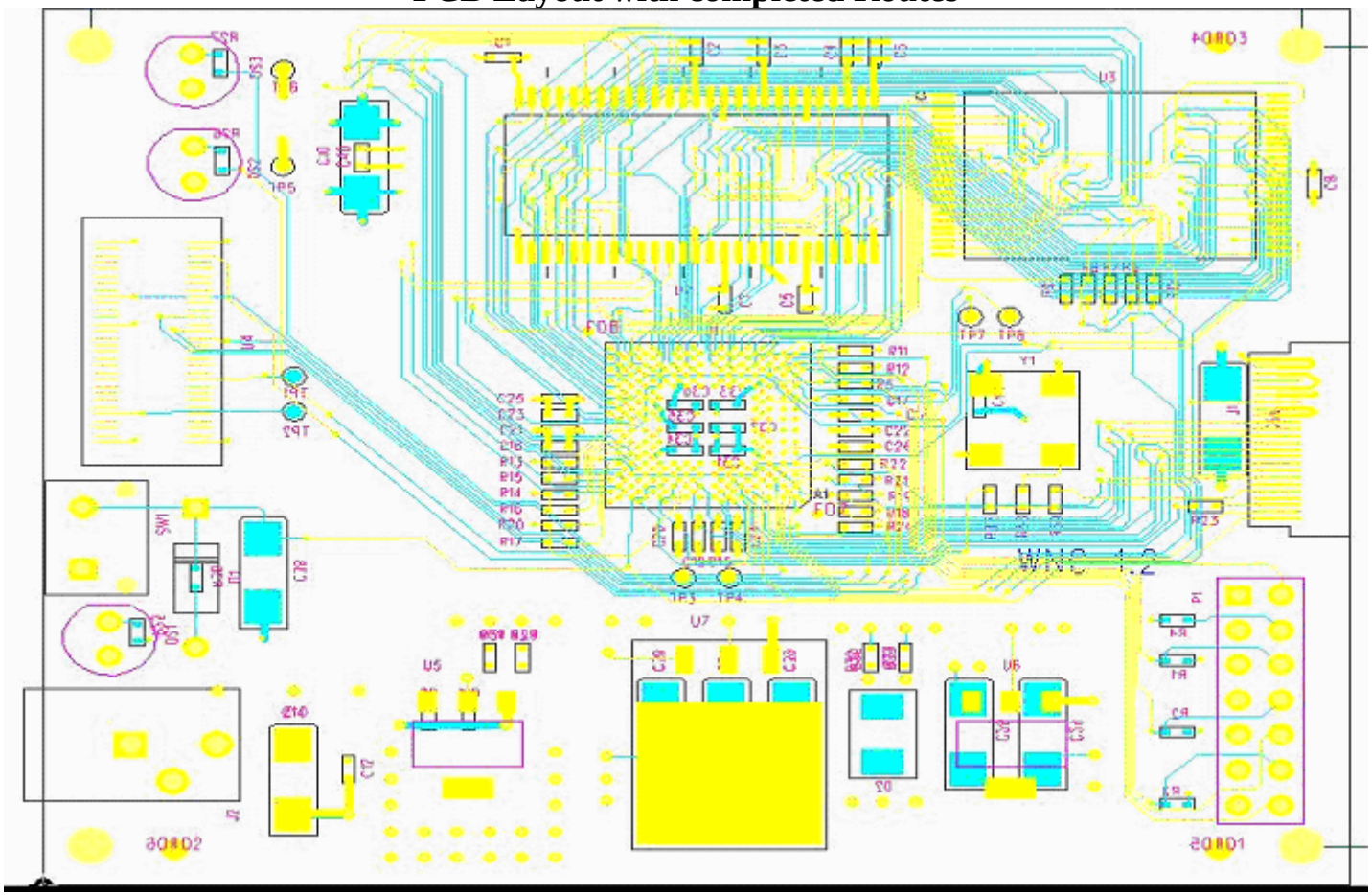

Figure 14: Complete PCB Layout (75mm x 63mm)

Appendix IV
Photo Plots

In the order:

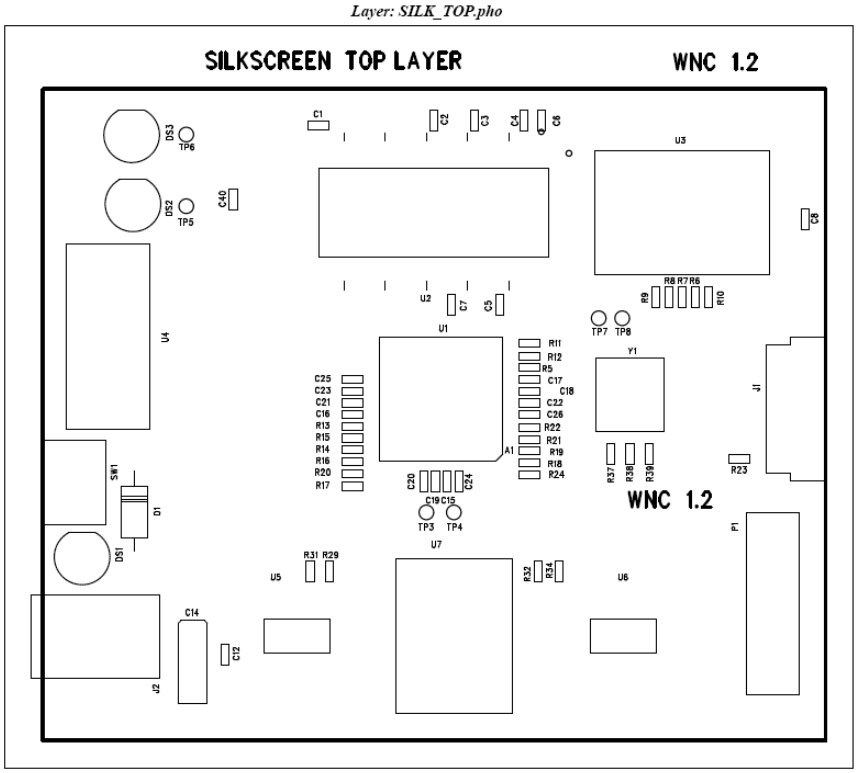

Figure 15

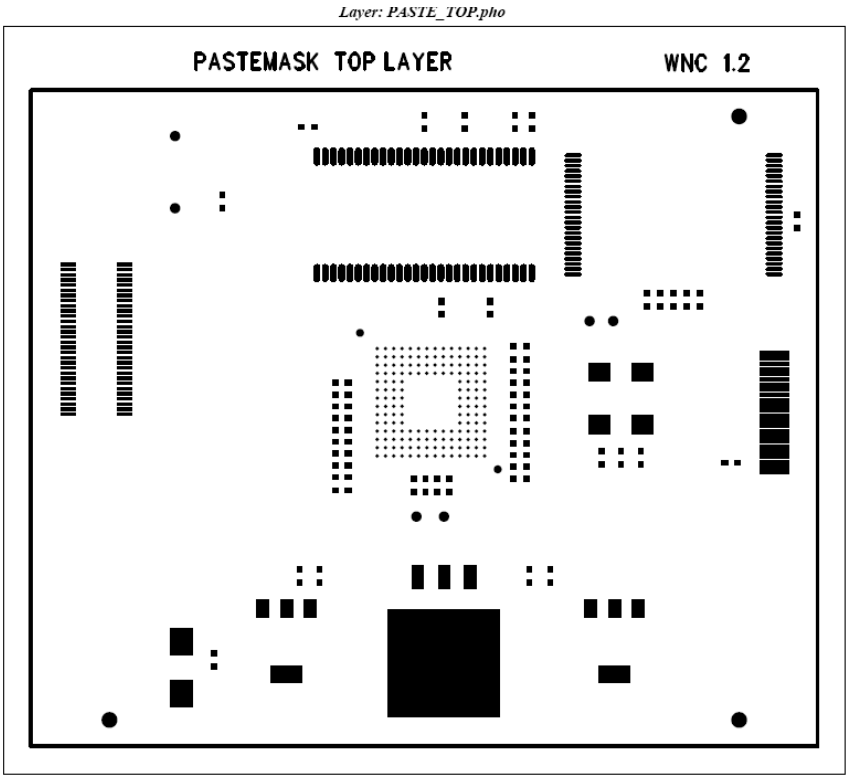

Figure 16

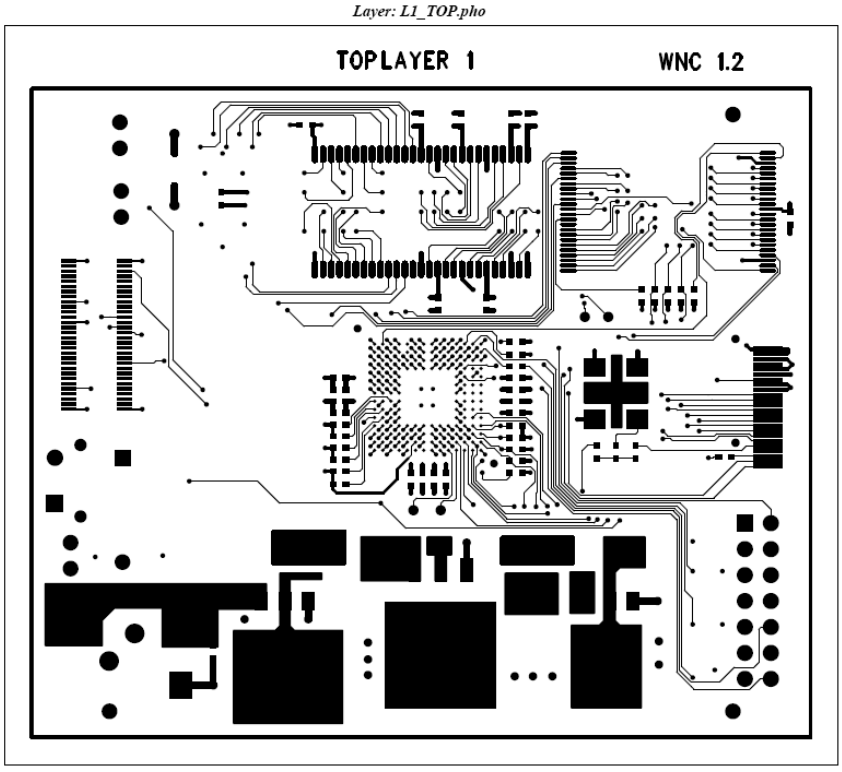

Figure 17

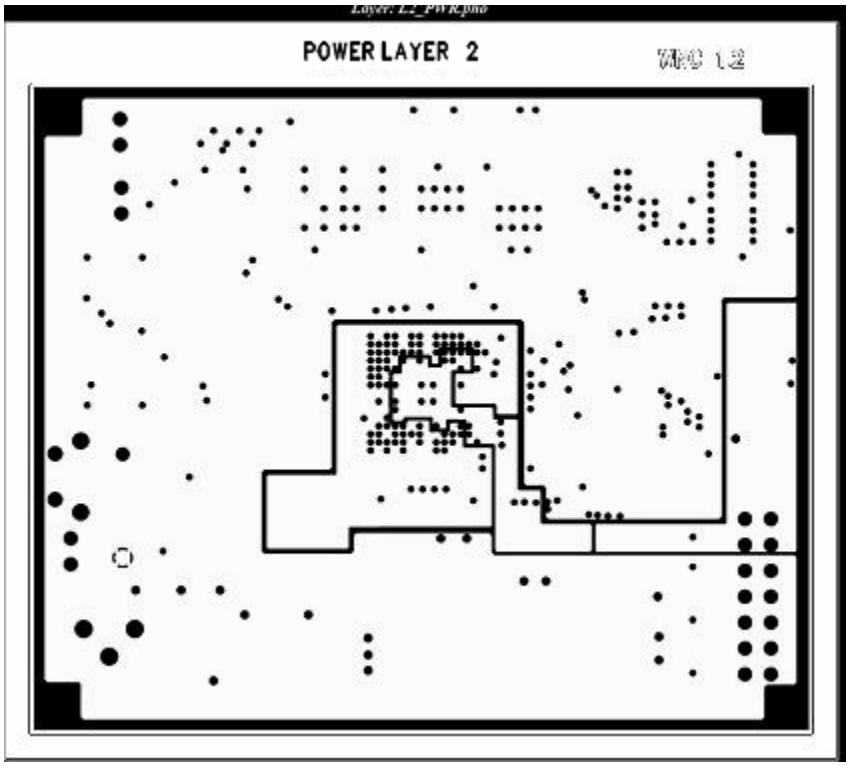

Figure 18

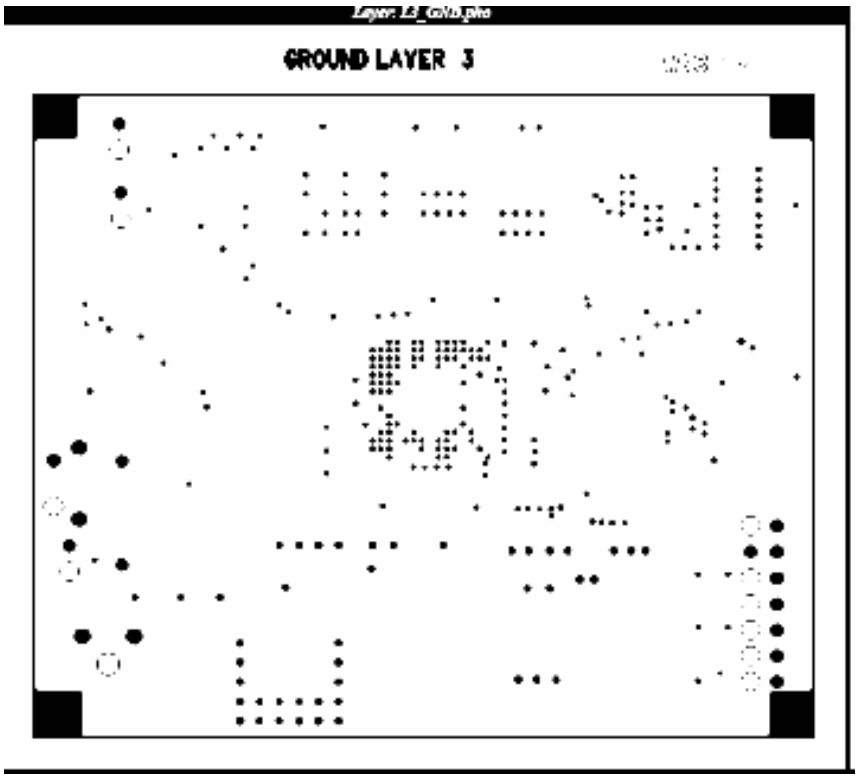

Figure 19

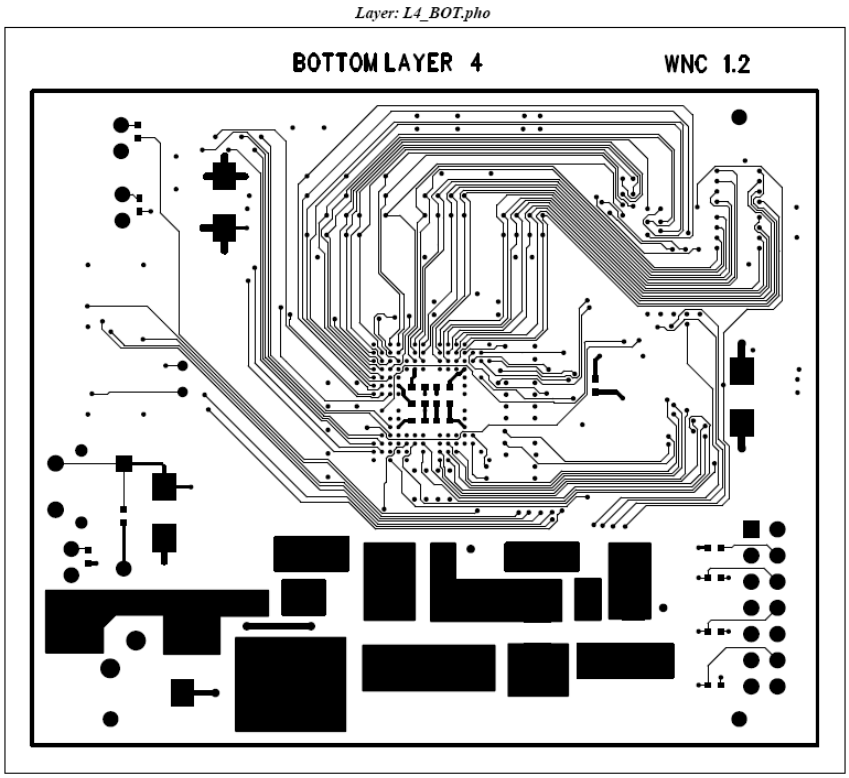

Figure 20

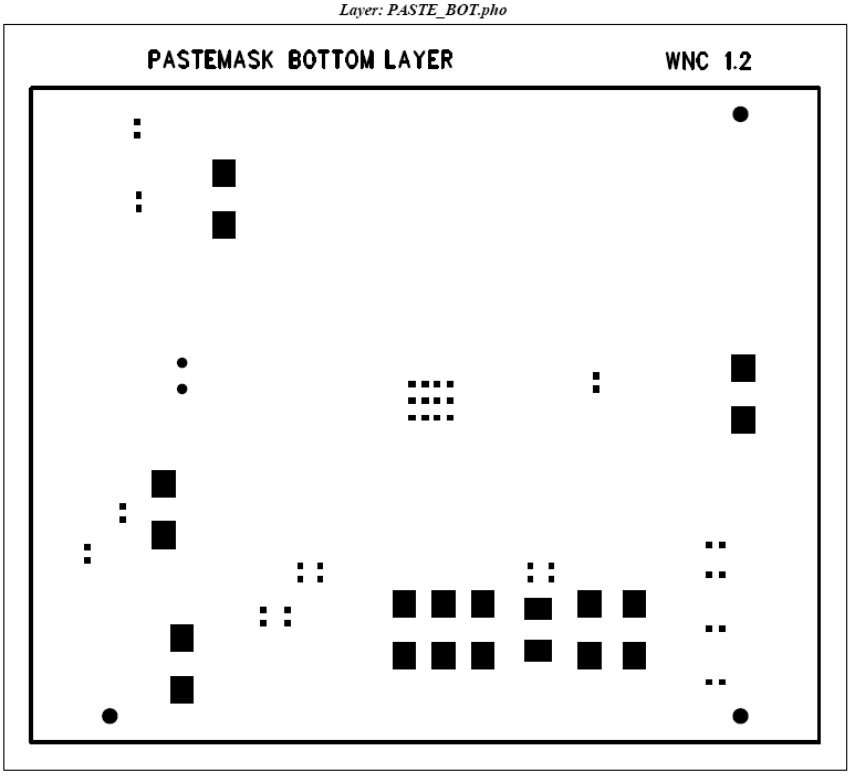

Figure 21

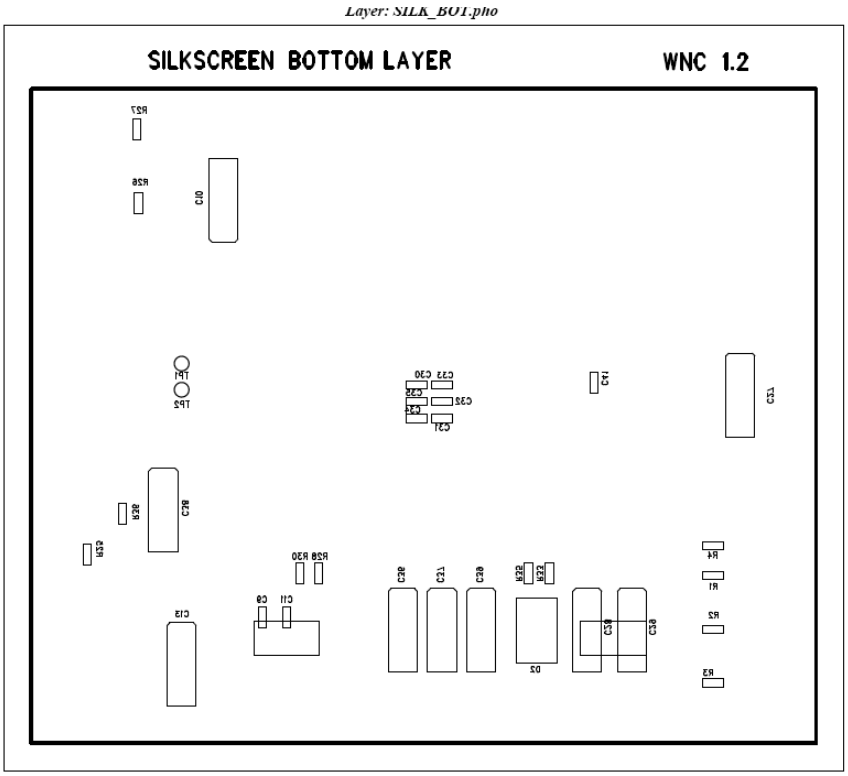

Figure 22

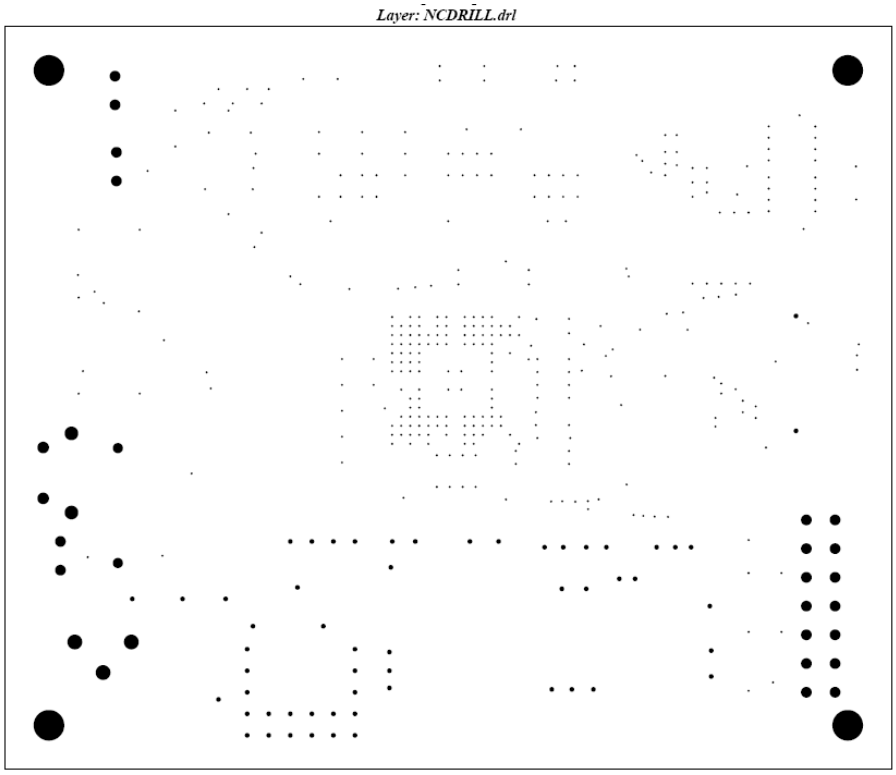

Figure 23

Appendix V
Assembled PCB

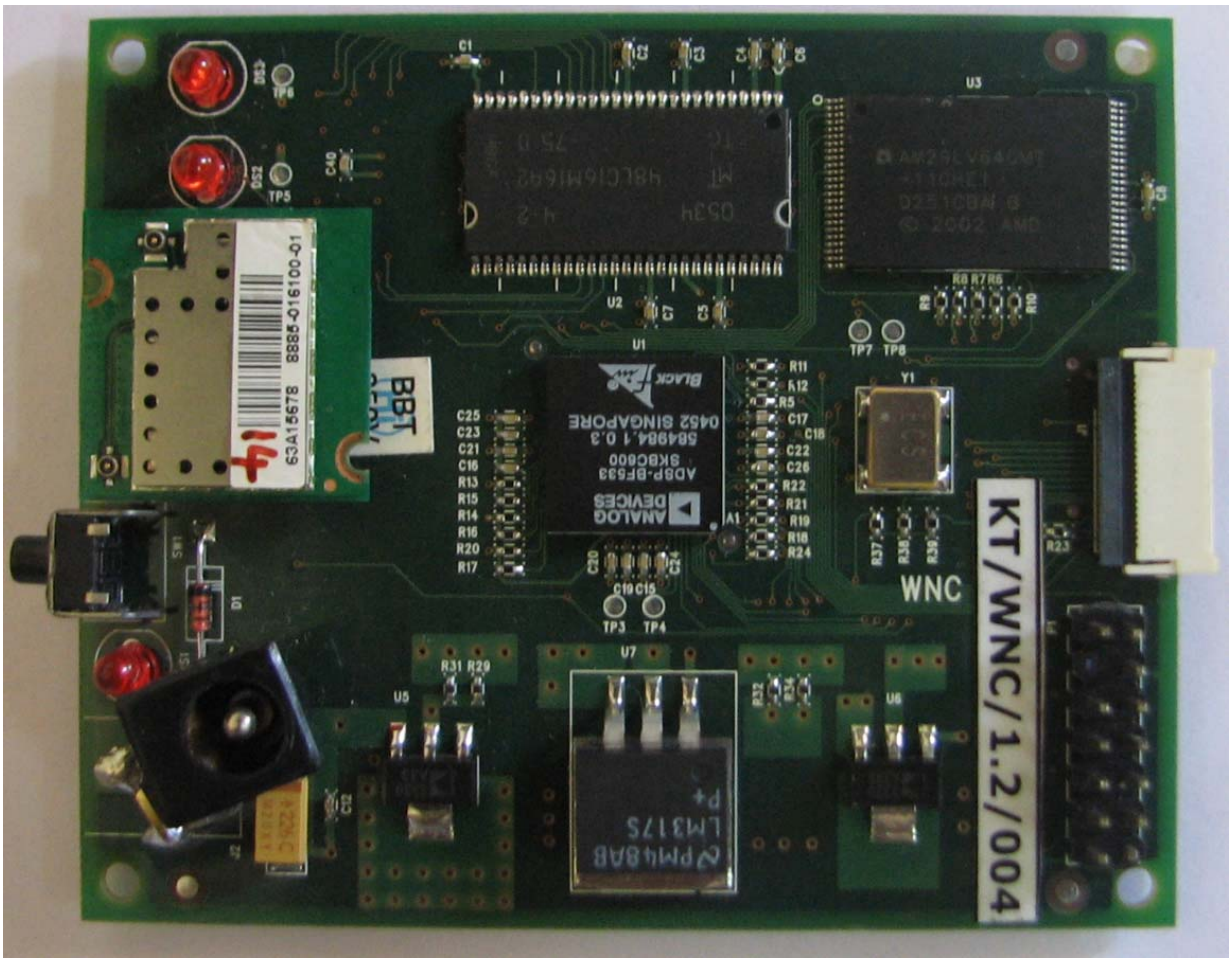

Figure 24: PCB after Fabrication and Assembly