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SMALL SIGNAL PHASE DETECTION AND CONDITIONING

Group No . D09

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ABSTRACT : The project aims at designing a device which can detect unwanted pulses generating from a high voltage system and determines it's basic parameters such as threshold voltage , peak value of the pulses and it's polarity . The pulses are generated at a very high frequency . We first design the circuit using normal operational – amplifier (LM 741) and check it by giving pulses from a frequency generator . The device helps us understand the nature of the unwanted pulses (noise) that is generated so that we can build our high voltage system for better efficiency .

1 . INTRODUCTION

Partial discharge is primary cause of the failure of high voltage systems . Partial discharge occurs when there is a gap in the dielectric between two electrodes in a high voltage device and which cannot be bridged . Partial discharge deteriorates the insulation and hence reduces the life of the system . In this project , we detect the pulses generated from the high voltage system due to partial discharge . The system superimposes these pulses on a 50 Hz AC signal and then later filters it out . The signal we get as our input is the filtered out signal . We design our device intially using normal operational amplifiers (LM 741) at very lower frequencies. The pulses which occur due to partial discharge have a very high frequency , of the order of 500 MHz . The width of these pulses is 60 – 100 nm and the amplitude is not more than 300 mV . Figure 1 shows the small signal pulses superimposed on the 50 Hz AC signal.

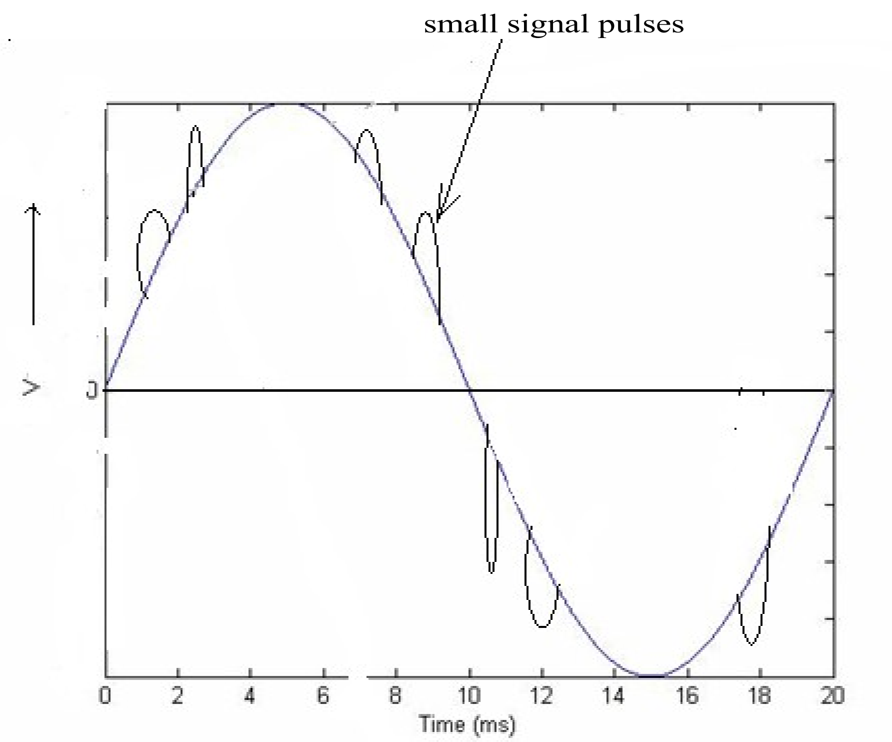

Fig 1 . Small signal pulses superimposed on sinusoidal 50 Hz AC supply voltage .

2 . BLOCK DIAGRAM :

The input signal we get from the high voltage system after filtering out the 50 Hz AC supply is amplified first using a pre – amplifier circuit . Then the output of pre – amplifier is given as an input to the absolute value detector circuit which inverts the polarity of the negative going pulses so that it’s output is always positive pulses . Then these pulses are used to determine the peak value by using the peak value detector circuit . We can also set the threshold voltage so as to allow pulses with some minimum amplitude to be sampled by the ADC . The pulses whose peak value is less than the threshold voltage are not considered for sampling i.e for those pulses whose magnitude is greater than the threshold voltage are only sampled . The sampling is done only at one point i.e the peak value .

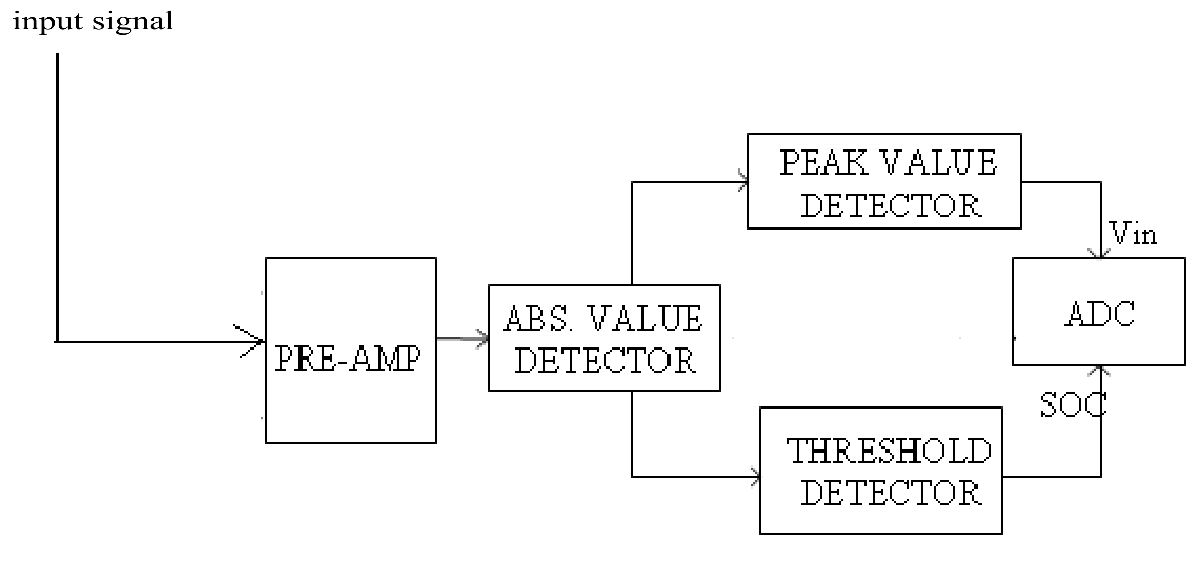

Fig 2 . Block Diagram of the proposed device

3. COMPONENTS :

a) LM 741 (for testing on bread – board)
b) THS 4302 (for pre – amplifier circuit)
c) AD 8000 (High speed operational amplifier)
d) ADC 12040 (High sampling rate ADC)
e) IN 4001 (Diode)
f) CL 1005 (Bipolar Junction Transistor)
g) pic18f4620 (Microcontroller)

4. CIRCUIT ANALYSIS :

<u>Pre – amplifier :</u>

The small signal pulses generated due to the partial discharge from the high voltage device have a very narrow width of the order of 60 – 100 nm and an amplitude of not more than 300 mV . These signals are passed through the pre – amplifier circuit . These pulses originate at a very high frequency of approximately 500 MHz . So , we should be using an amplifier which works at very high frequency . THS 4302 produced by Texas Instruments is an operational – amplifier which works effectively at a very frequency upto 1 GHz and has a very high slew – rate (5500 V / micro-s) . It also offers a very low noise (which is very essential in a high voltage system because a lot of noise generated by a high voltage system hence it becomes essential to use such devices which will generate less noise) and hence low signal distortion . It is a fixed gain amplifier with a gain of 5 V / V . Hence if the input pulses have an amplitude of 300 mV , the signal at the output will have an amplitude of 1.5 V . Figure 3 gives the pin – description of THS 4302 and Figure 4 gives the circuitry for pre – amplifier . The pre – amplifier is basically a non – inverting amplifier . The capacitors at the input is used to further filter out the DC components in the signal . We could have used another capacitor at the output of the pre – amplifier but the output signal thus received had a negative DC component .

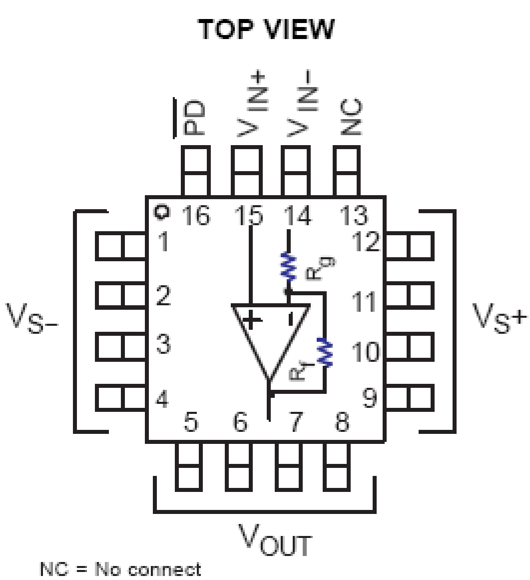

Fig . 3 . Pin description of THS 4302

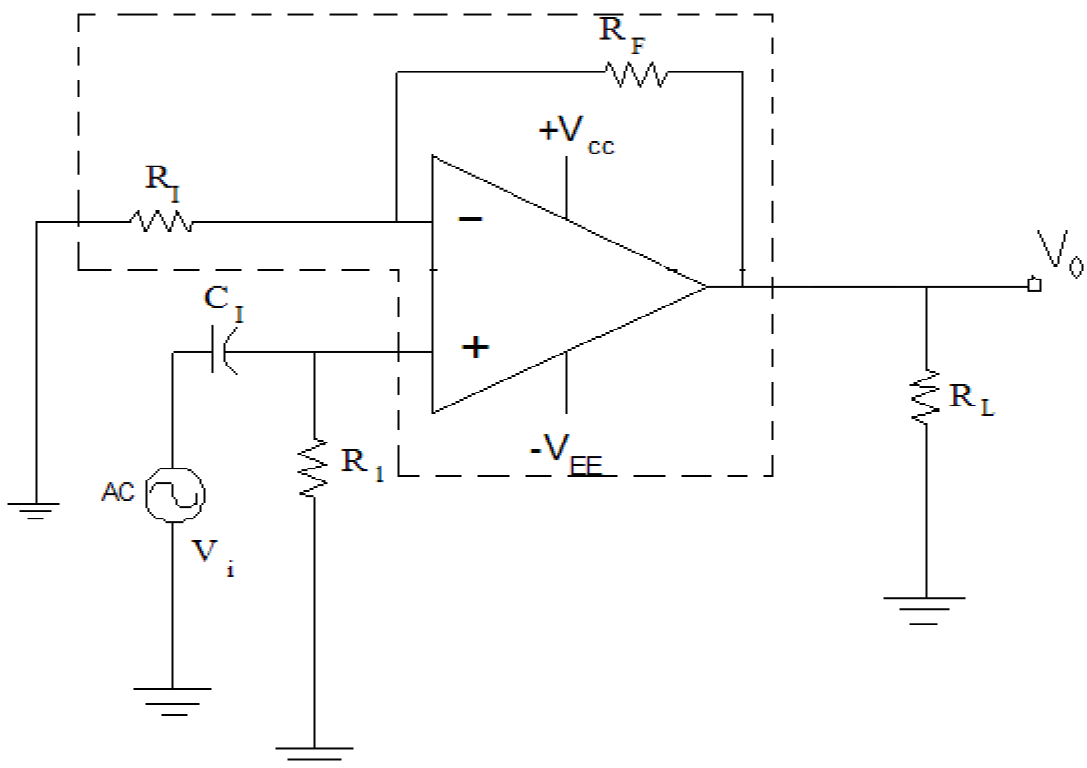

Fig 4 . Pre – amplifier circuit

The region under the dotted curve is the fixed gain amplifier THS 4302 in which R_F and R_I are fixed by the manufacturer such that $R_F / R_I = 5$. While testing on bread – board we are using LM 741 where in we decide the value of R_F and R_I so that we get a gain of 5 .

Absolute Value Detector :

The small signal PD pulses can either be positive or negative . The negative pulses are inverted by implementing this circuit as this circuit is made unipolar . We are using a precision rectifier for this purpose due to very low input voltage signals . This detector circuit should provide a unity gain . For this purpose the values of R1 and R4 must be equal to R2 and R5 respectively .Hence,the output is a unipolar signal (always positive) .We are using AD 8000 operational amplifier for the absolute value detector . AD 8000 is an ultra – high speed , high performance , current feedback amplifier . It has a very high slew – rate of 4100 V / micro – sec which is comparable to the THS 4302 operational – amplifier . The major difference between these two devices is that THS 4302 is a fixed gain amplifier and AD 8000 is not . Figure 5 gives us the pin – description of AD 8000 .

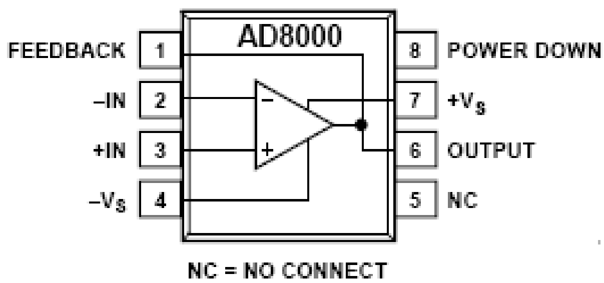

Fig 5. Pin description of AD 8000 .

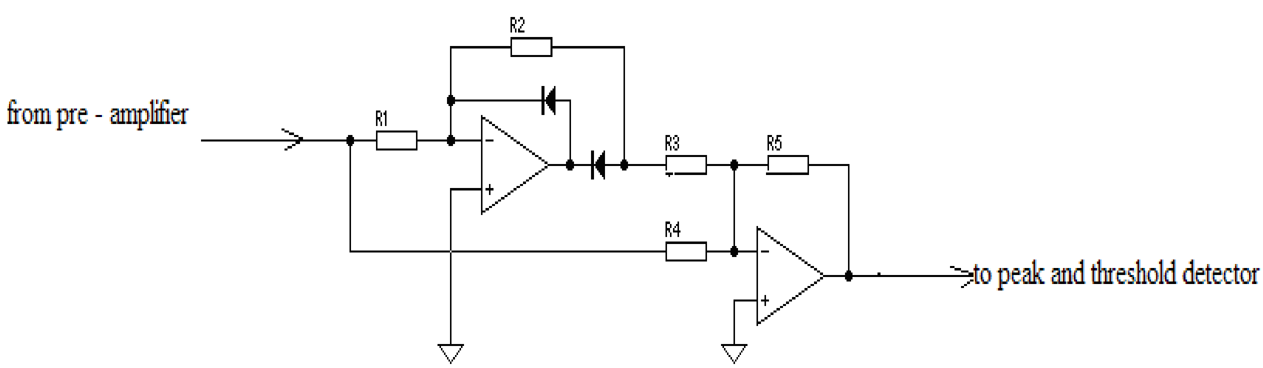

Fig 6. Absolute Value Detector .

If the input given to the absolute value detector is a sinusoidal AC wave then the output will be a unipolar DC as in figure 7 .

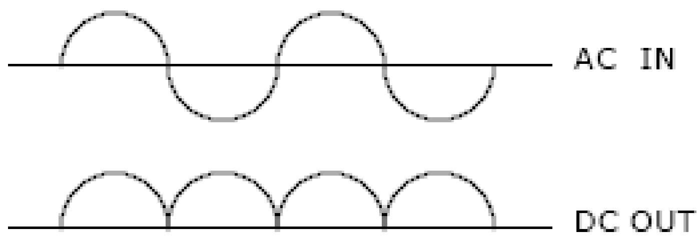

Fig 7 . Input / output characteristic of the absolute value detector

Threshold detector :

This circuit helps us to set a threshold voltage for the pulses coming in from the absolute value detector . If the pulses are above the noise – margin set by this circuit , we allow these pulses to go through to the ADC for sampling . For this purpose , we use a comparator i.e a pulse width modulator . The comparator output is high whenever the magnitude of the pulses appearing at it's non – inverting terminal is greater than the noise – margin that is set at it's inverting terminal . We can change this threshold voltage by varying the potentiometer . The output of this circuit is used to drive the ADC . The ADC is enabled only when the output of the comparator is high . Figure 8 shows the circuit diagram for the threshold detector .

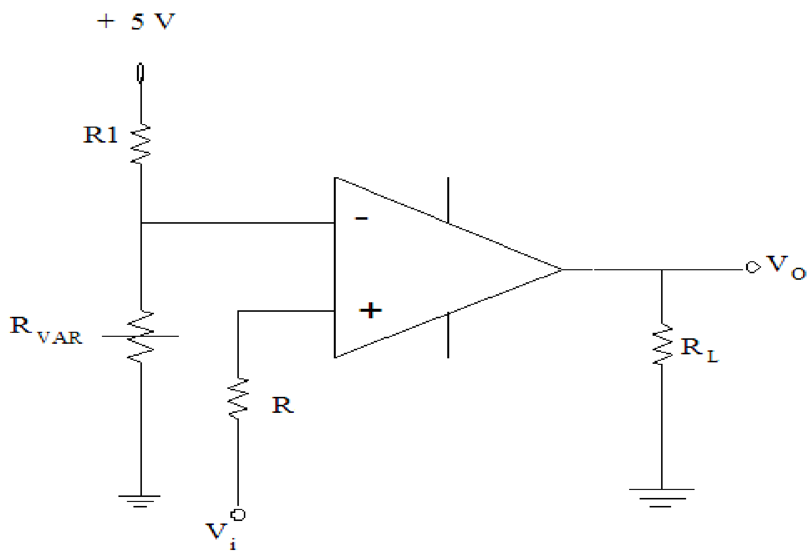

Figure 8 . Threshold value detector .

Figure 9 shows the input / output waveforms of the comparator . The threshold voltage is a constant DC voltage whose magnitude can be changed by varying the potentiometer .

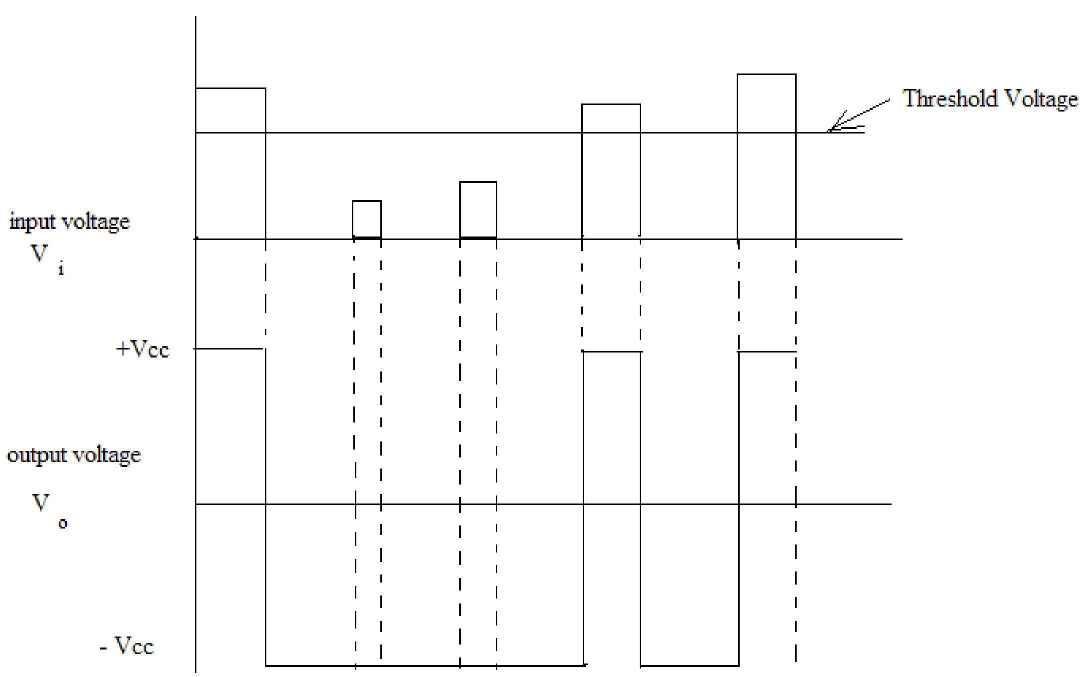

Fig 9. Input / output characteristics of the threshold detector.

Peak value detector :

The peak value detector traces the peak of the pulses and holds it for sometime for the Analog – to – digital converter . The peak is obtained by charging a capacitor through a diode so that ideally no return path is available for capacitor to discharge . Discharging is done using a bipolar junction transistor . The transistor is kept open initially for charging . When we need to discharge the capacitor , we connect the base to the supply voltage of 5 Volts (15 volts in the case of testing on bread – board with LM 741) . Figure 10 shows the circuit diagram of the peak value detector . Figure 11 shows the ideal behaviour of the peak value detector . The peak value detector holds the peak of the signal until the peak is sampled completely by the ADC . After sampling the peak completely , we discharge the capacitor . Here again , the gain of the peak - value detector should be unity . Hence , the values of R1 and R3 is the same as the values of R2 and R4 respectively . The RC circuit we have made using R5 and C1 should ideally have a large time constant so that a constant DC voltage is obtained at the output of the peak – value detector . The discharging is done manually when testing on the bread – board and by using a monoshot while implementing the circuit on PCB level . The signal obtained at the output of the peak – value detector circuit is given as an input to the ADC for sampling .

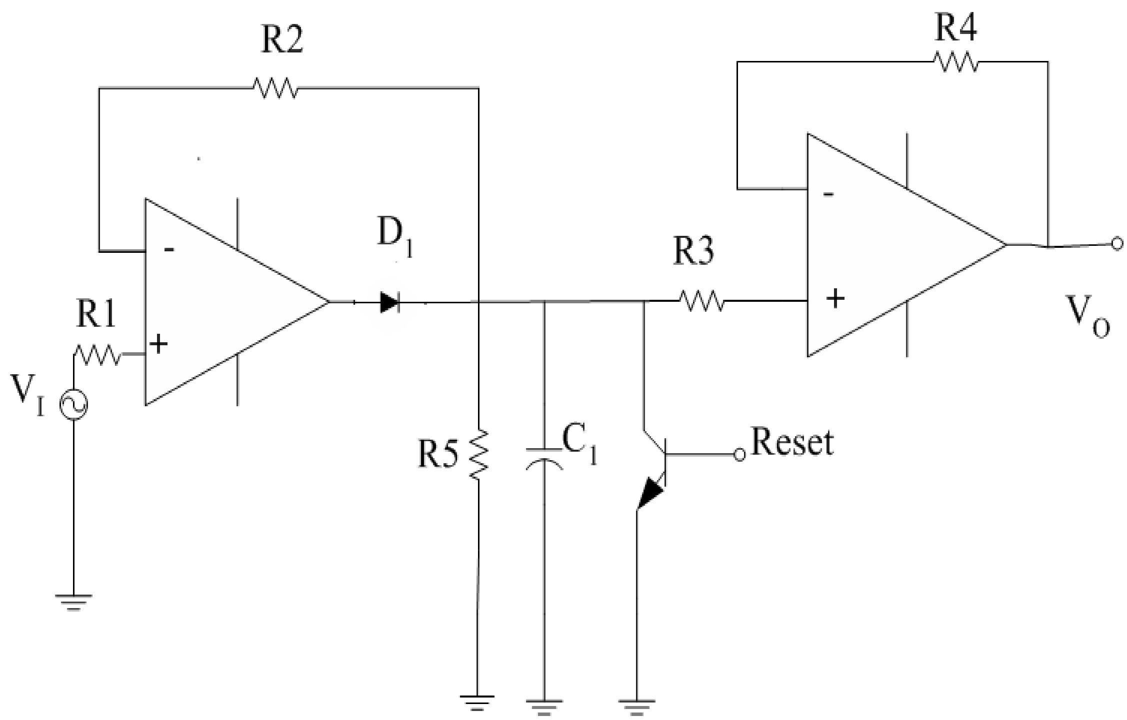

Figure 10 . Peak value detector circuit .

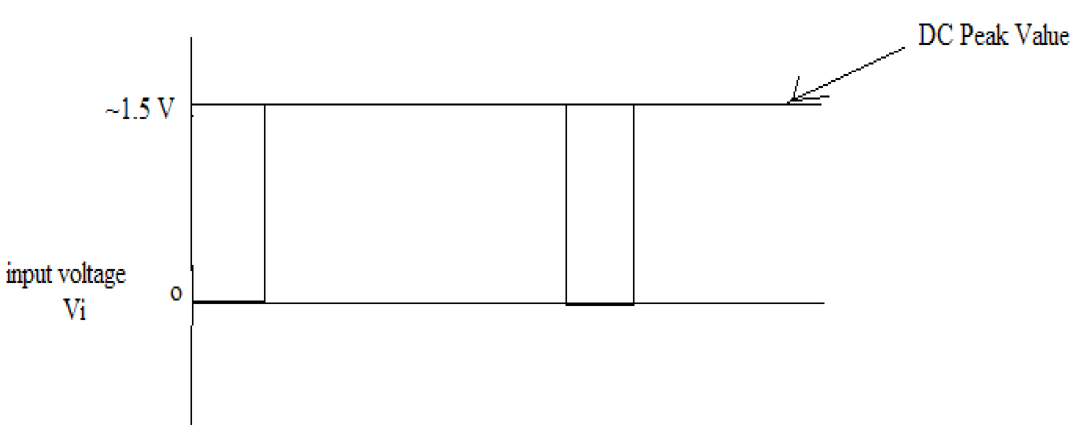

Fig 11 . Input / output behaviour of the peak value detector .

Analog – to – Digital converter (ADC) :

The ADC is used to digitise the peak of the small signal pulses . It is enabled when the output of the threshold value detector is high i.e when the magnitude of the pulses is greater than the noise – margin set by the threshold detector circuit . The input to the ADC is the peak value of the pulses which is sampled . The sampling rate of the ADC should be very high due to the high frequency of the pulses . The ADC we shall be using is ADC 12040 manufactured by National Semiconductors having a sampling rate of 40 MSPS (Mega Samples Per Second) . ADC 12040 is a 32 pin 12 – bit Analog – to – digital converter . We give a reference voltage to the ADC and then the output we obtain is in the digital form depending upon the reference voltage . Hence , we get 2^12 = 4096 different digital levels . The information obtained by the ADC is then transferred for further applications . Figure 12 shows the pin description of ADC 12040 .

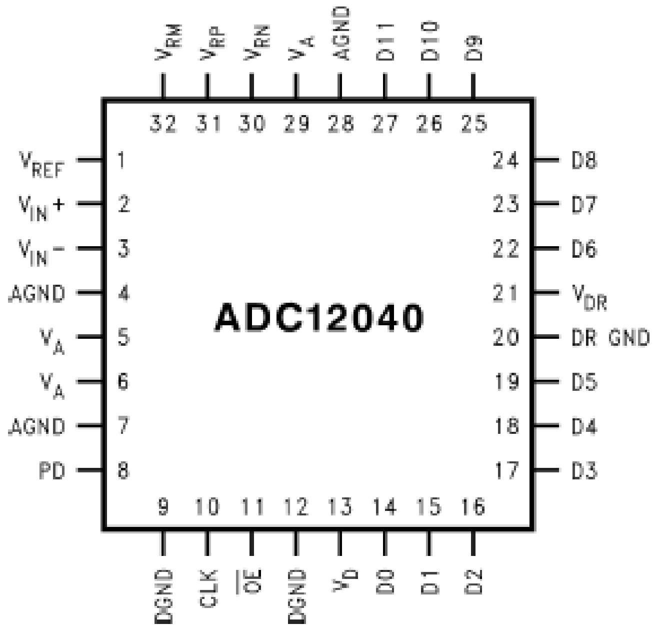

Fig 12 . Pin description of ADC 12040

Testing on bread – board :

We have used general purpose operational – amplifier LM 741 for testing on the bread board . The input signal to the pre – amplifier circuit is given by a frequency generator . The frequency of the input signal in this case should not be more than 3-4 MHz as the slew rate of LM 741 is very low . The magnitude of the input voltage is set at nearly 300 mV so that after amplification at the pre – amplifier level, the magnitude is nearly 1.5 V . Figure 13 shows the pin description of LM 741 in a dual-in-line package .

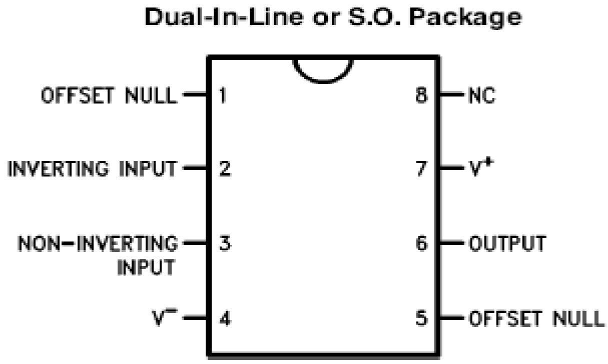

Fig 13 . Pin description of LM 741 .

5. SCHEMATIC :

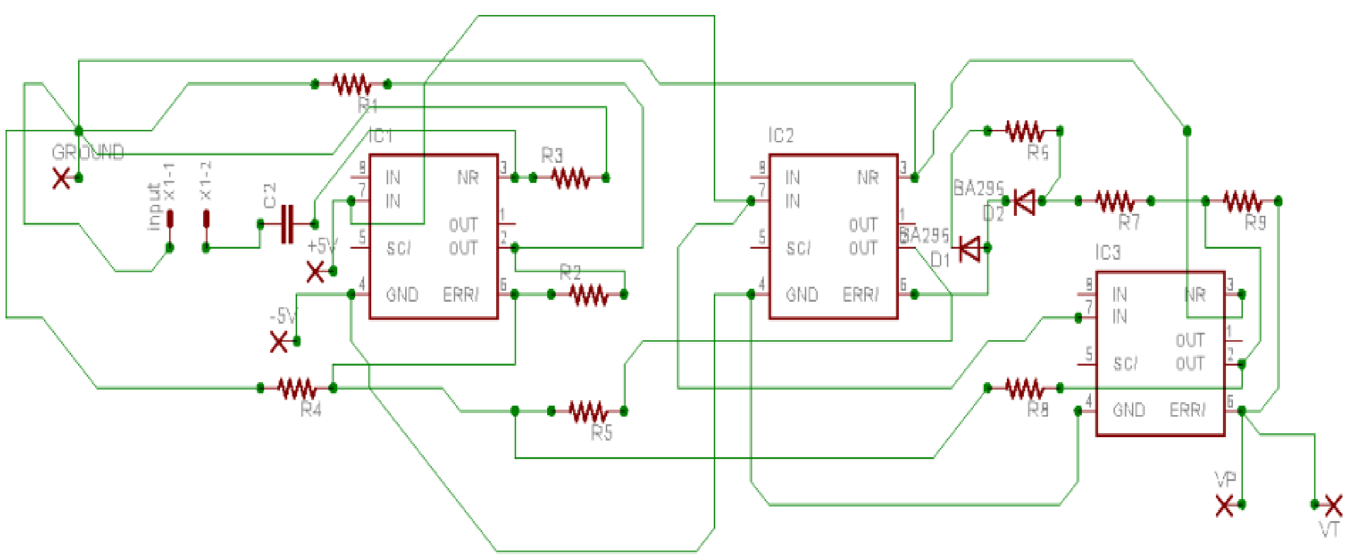

Fig 14 . Schematic for pre-amplifier and absolute value detector .

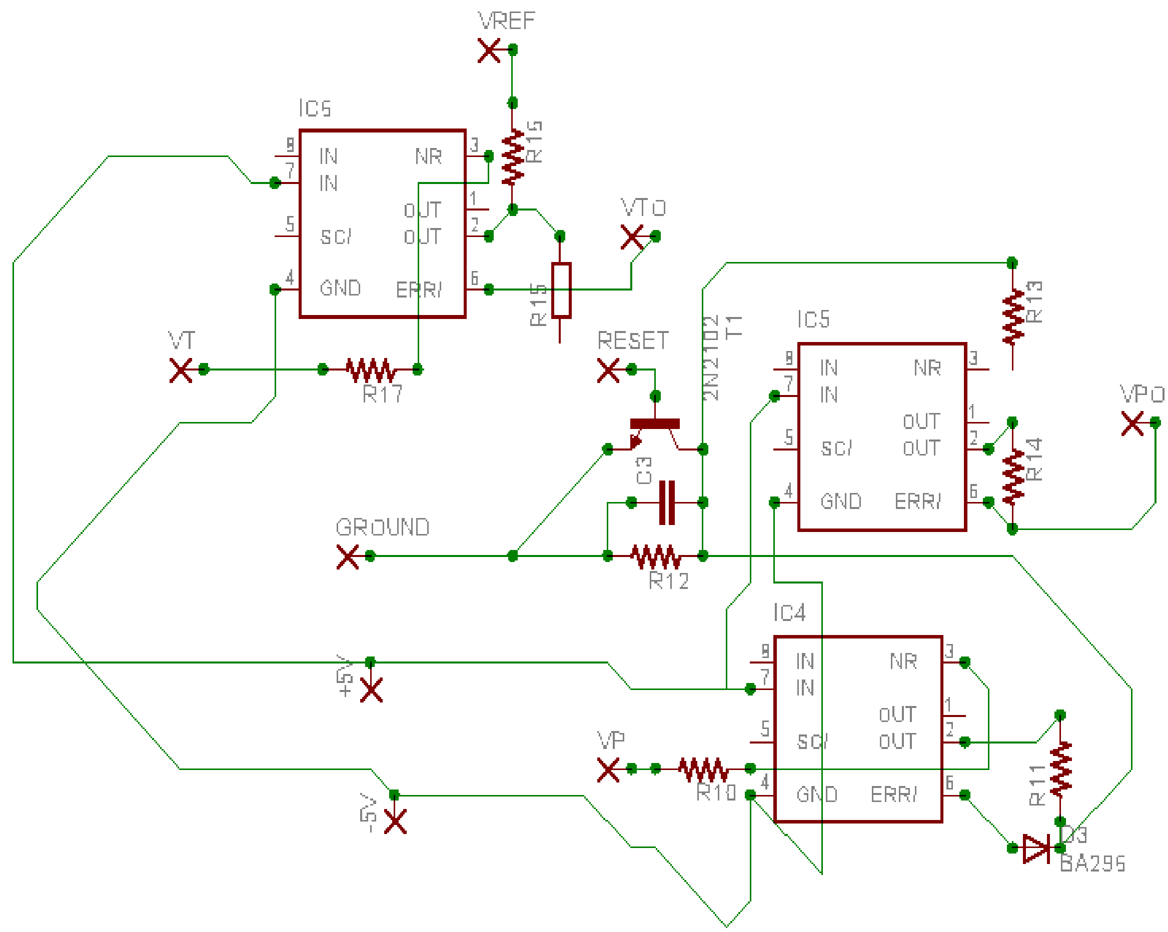

Fig 15. Schematic for peak value and threshold ciruit .

6. PCB WORK :

Two separate PCBs is made , one consisting of pre – amplifier and the absolute value detector circuits and the other consisting of peak value and threshold value detector circuits . Figure 16 and figure 17 shows these two different PCBs respectively .

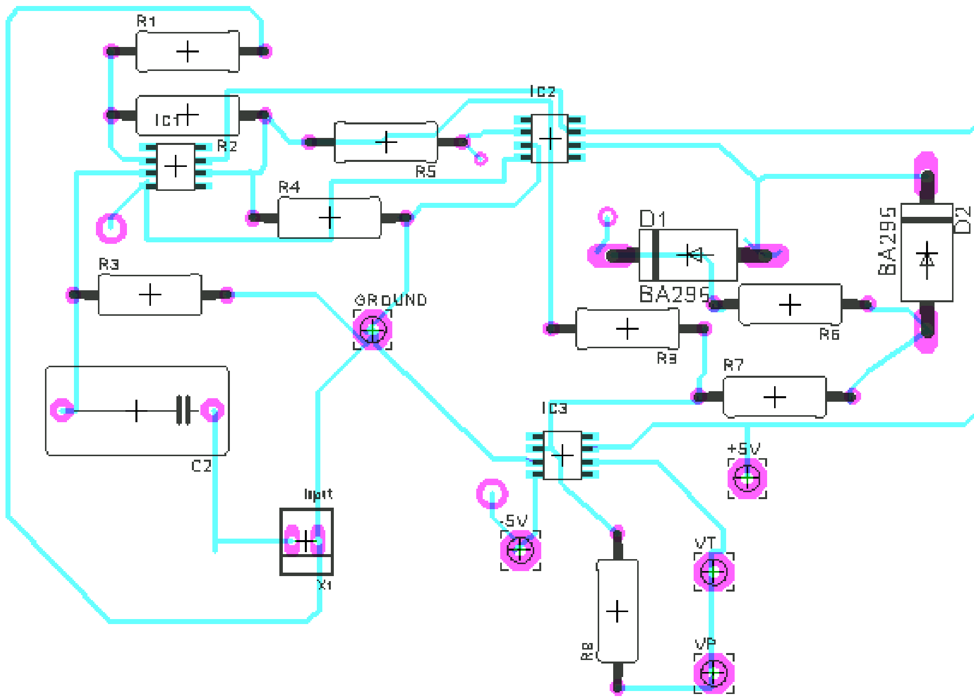

Fig 16. PCB for peak – value and absolute value detector circuits.

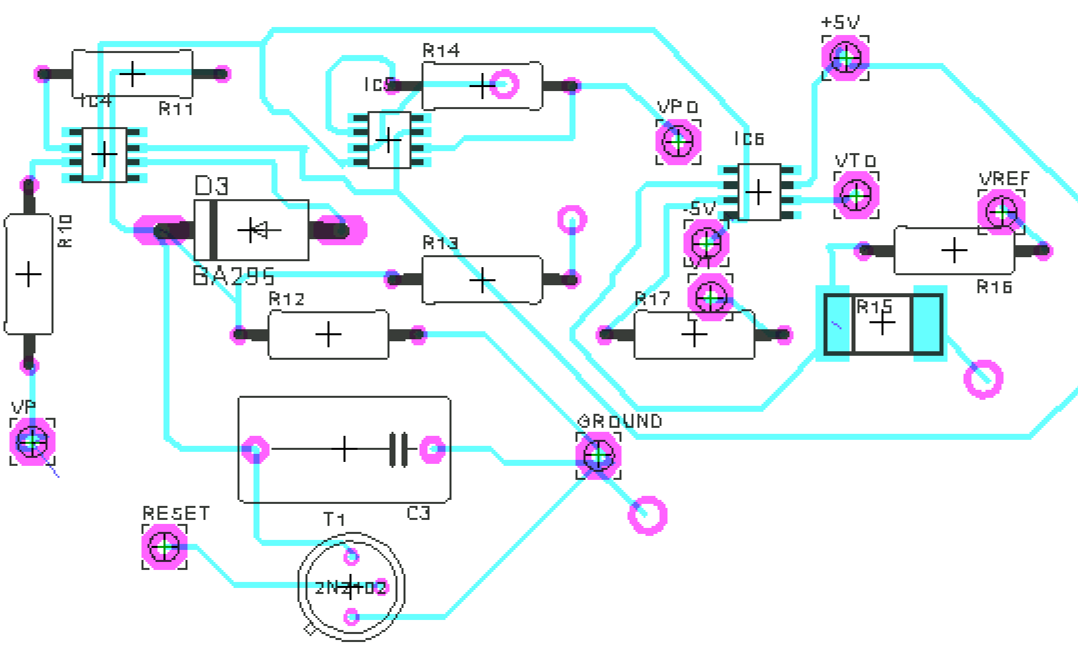

Fig 17 . PCB for peak value and threshold value circuits .

CONCLUSIONS :

Initially , we give the input pulses to the pre – amplifier circuit which amplifies the signal by 5 times . This amplified signal is then made unipolar by using the absolute value detector circuit . We set the threshold voltage by implementing threshold detector circuit .
The peak value which is obtained by the peak value detector is then sampled by the ADC if the magnitude of the pulses is greater than the threshold voltage . For those pulses whose magnitude is less than the threshold voltage , the ADC is idle i.e it does not sample the signal .
The peak is sampled using a 12 – bit ADC hence we get 4096 different digital levels corresponding to the Vref that is set .
All these cicuits have been implemented on bread – board using LM 741 for low frequencies of input voltage . On the PCB level , we are using operational – amplifiers having high slew rate (THS 4302 and AD 8000) . The sampling is done by ADC 12040 .

ACNOWLEDGEMENT :

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