EDL Group D07: Project Report

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A set up for measuring capacitance vs voltage characteristics of MOSCAPs

Abstract
This project involves design and fabrication of a setup to measure the HFCV characteristics of the MOSCAP wafers. We have modeled MOSCAP as a capacitor, and biased it with a small signal sinusoidal voltage riding on the DC. The current through MOSCAP is measured, converted into voltage from which, the value of capacitance is calculated.
We have designed circuits for achieving the above, and they were giving results on the breadboard. Our PCBs, though were designed by following the guidelines, turned out to be noisy, and could not give the required results. So, presently, we have a proof of concept on the breadboard level.

1. Introduction

The CV characteristics of the MOSCAP is widely used as a diagnostic tool to know the nature and amount of defects in the MOSCAP. We can also derive important parameters like doping, oxide thickness etc of the wafer from the CV data. In the present report, we describe an approach towards building such a setup for CV measurement of MOSCAPs.

2. Problem statement

To build a setup for the High Frequency Capacitance vs. Voltage measurement of MOSCAPs.
Given a MOSCAP wafer, we need to generate an array of capacitance of the wafer at operating high frequency and the corresponding applied DC bias voltage.

3. Theory

The capacitance of the MOSCAP wafer varies as it passes through the accumulation, depletion and inversion regions. This change is brought about by a varying DC bias voltage applied at the gate.

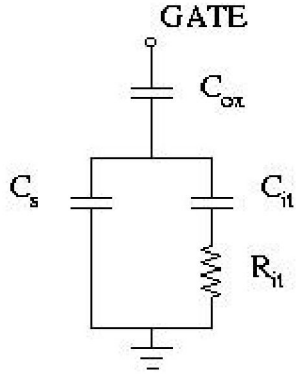


Fig 1: Eq. ckt. of MOSCAP at all frequencies,

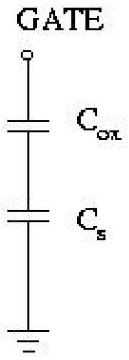


Fig 2: Eq. ckt at high frequencies

Above Fig 1 shows the equivalent circuit of the MOSCAP at all frequencies. At high frequencies, the equivalent circuit becomes as shown in Fig 2. This is due to the fact that the interface traps can not respond to changes happening at very high frequency.
Now considering the circuit of Fig.2 at high frequency, the total capacitance of the MOSCAP is:

$$C_{eff} = (C_{ox} \times C_s) / (C_{ox} + C_s) \quad (1)$$

Where Cox is the oxide capacitance and Cs is the depletion capacitance of the substrate. Now lets see how the total capacitance of MOSCAP should vary as the bias voltage is changed:

1. **Accumulation Region:**

Here, we have applied a negative voltage to the N-type MOSCAP, and majority carriers are attracted towards the gate oxide. Hence the length of the depletion region reduces, hence Cs becomes much more than Cox. This happens because any capacitance (per unit area) is given by:

$$C = \varepsilon / d \quad (2)$$

Where ε the permittivity of that medium and d is is the distance between the plates of the parallel plate capacitor.
Thus the C_{eff} now essentially becomes C_{ox}, which is the value of the oxide capacitance.

2. **Depletion Region:**

As the voltage is increased, Cs starts reducing as the depletion region starts to form, which increases d. Now the value of the C_{eff} starts reducing. Eventually reaching minima where we have a minimum value of the Cs. The total capacitance measured at this point is Cmin.

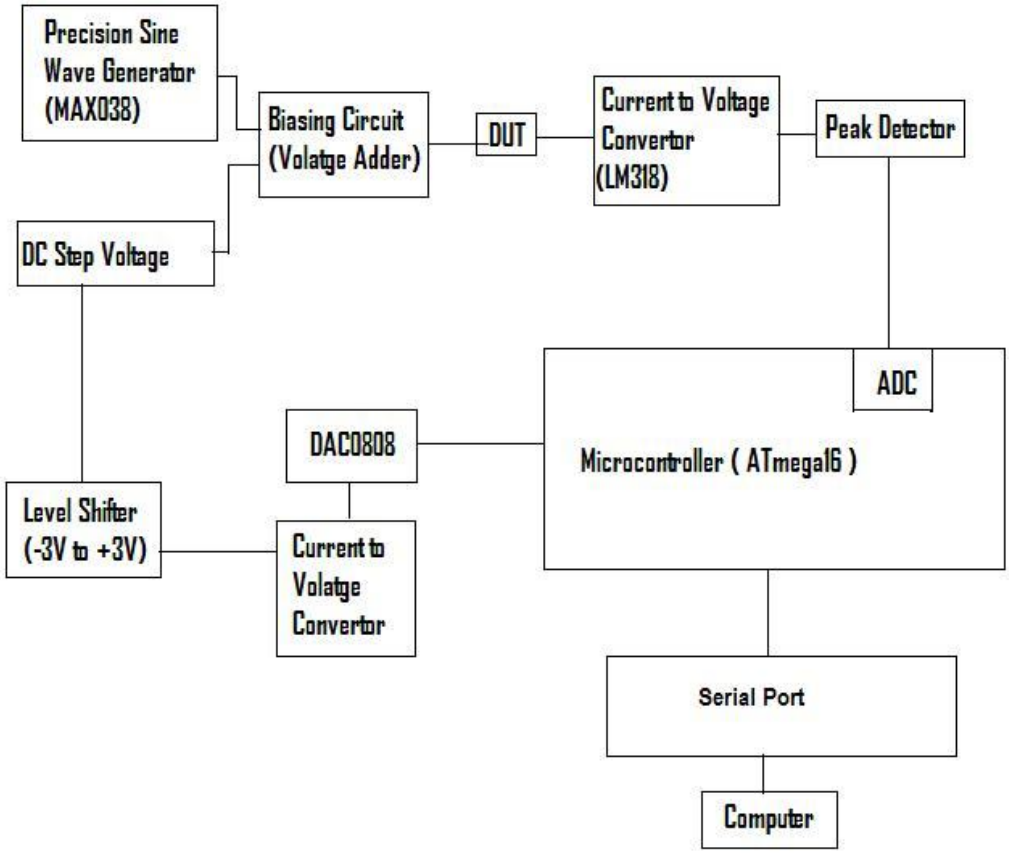
3. **Inversion Region:**

As the voltage becomes sufficiently positive (more than the threshold voltage), we get a inversion layer, inside the MOSCAP. Now the charges in this inversion layer are the minority charges. But minority charges can not respond to the higher frequencies, so we don't have any small signal change in the capacitance Cs. Thus the total capacitance stays at the Cmin for HFCV measurements.
If the step voltage is increased in very fast manner, and we try to take a measurement before giving time to charges to settle down, we might measure a capacitance which is lower than Cmin. This is called deep depletion. One needs to avoid the deep depletion condition by taking measurements after a certain time delay, and by limiting the slop of the step waveform applied to the wafer.

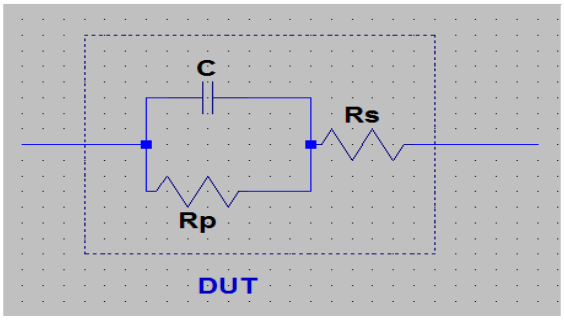
4. Design Approach

We plan to give an ac voltage superposed on a step voltage to the MOSCAP, and then measure the ac current flowing through it, to get the value of the capacitance of MOSCAP at

that particular DC bias voltage. Values stored in an array of this voltage and the corresponding capacitance will be fed to a graph plotter and from which, we can generate a CV curve.

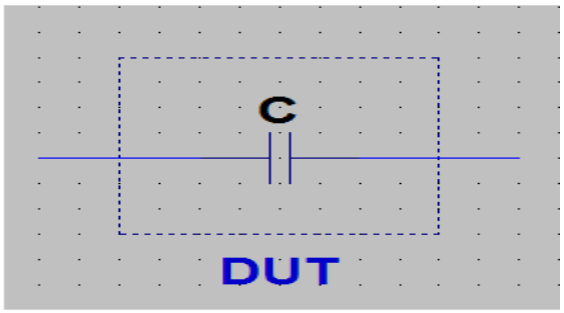


Our DUT is a MOSCAP wafer, and in general, any capacitance can be modeled by following equivalent circuit.

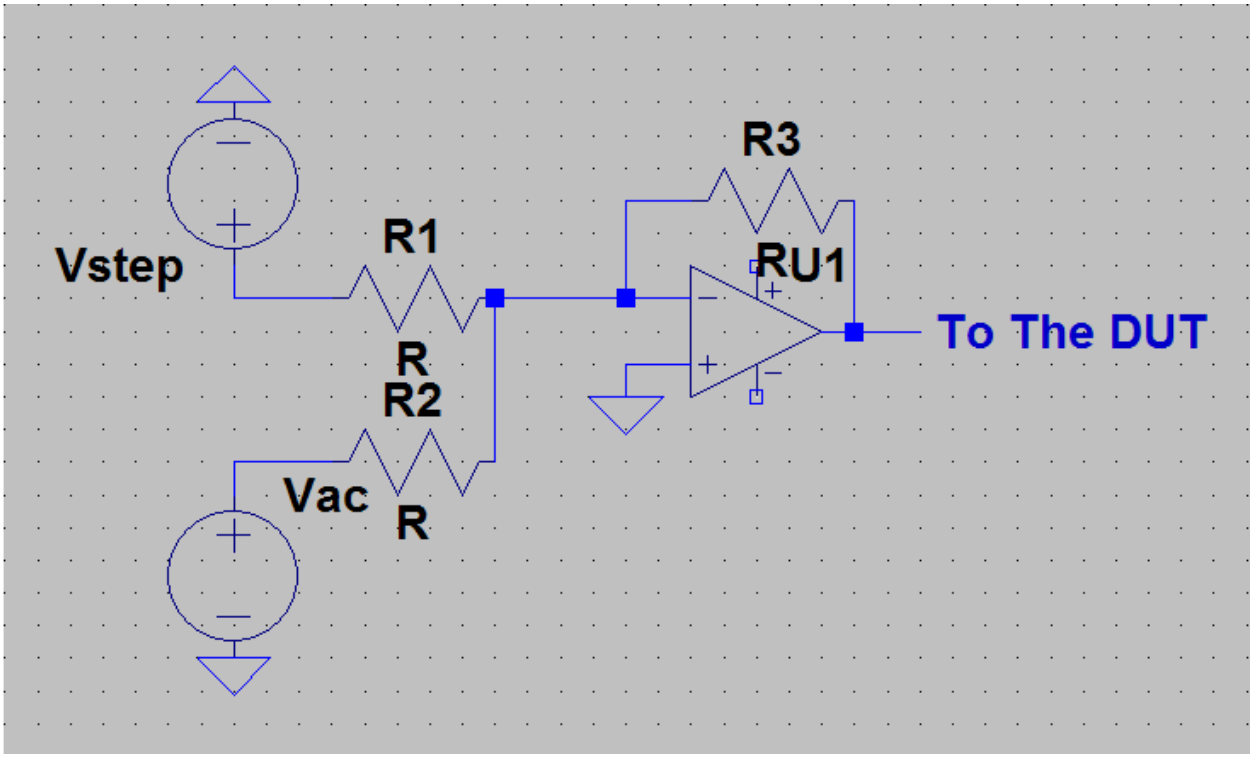


But for small values of the DUT capacitance C, and high values of the shunt resistance Rp, the series resistance can be ignored from the equivalent circuit model. Also, the typical values of the shunt resistance for good quality nitride MOSFETS are more than 10^9 ohm.. At such large values, the R_p is essentially infinite, and corresponds to an open circuit. Hence we have modeled

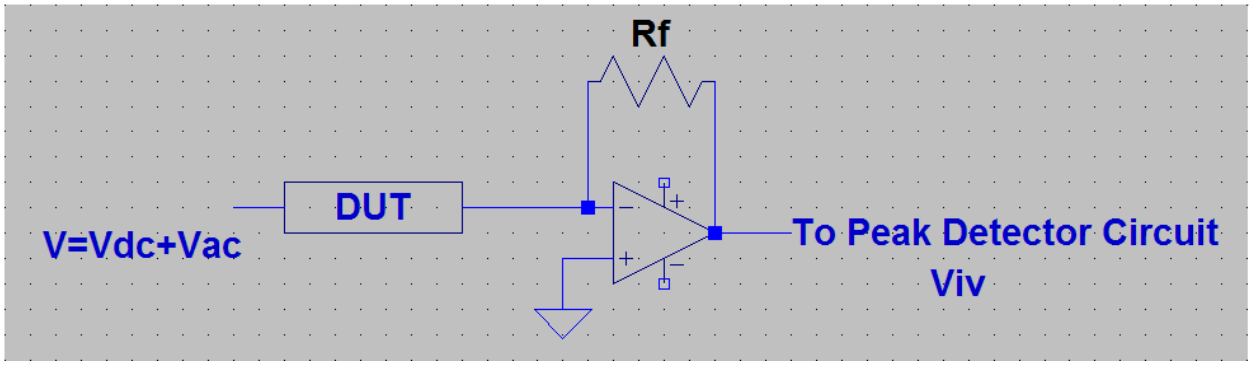
the DUT as just a capacitor. Simulation results show that this approximation is reasonable for good wafers, with high Rp.



The MOSCAP is biased as mentioned above by a unity gain op amp adder circuit.
Where R1=R2=R3.



The value of small signal voltage is chosen to be 40 mv , which lies well within the range of small signal voltages used by the commercial CV meters . This value is not too low so that it won't get badly affected by the noise; also it's not too high so that it will affect the DC bias voltage. The current flowing through the MOSCAP is measured by a current to voltage converter circuit, which produces a decently high value of ac voltage for corresponding current.



Assuming the non inverting input of the op amp2 in the current to voltage converter circuit is grounded, we have the voltage across DUT to be:

$$V = V_{ac} + V_{dc} \quad (3)$$

Assuming that the capacitance of the DUT is C, and then the current flowing through the DUT, measured after the DC step voltage has reached steady state for that particular step is

$$I = C\frac{d}{dt}[V] = C\frac{d}{dt}[V_{ac}] = C \times A_0 \times \omega \times \cos(\omega t) \quad (4)$$

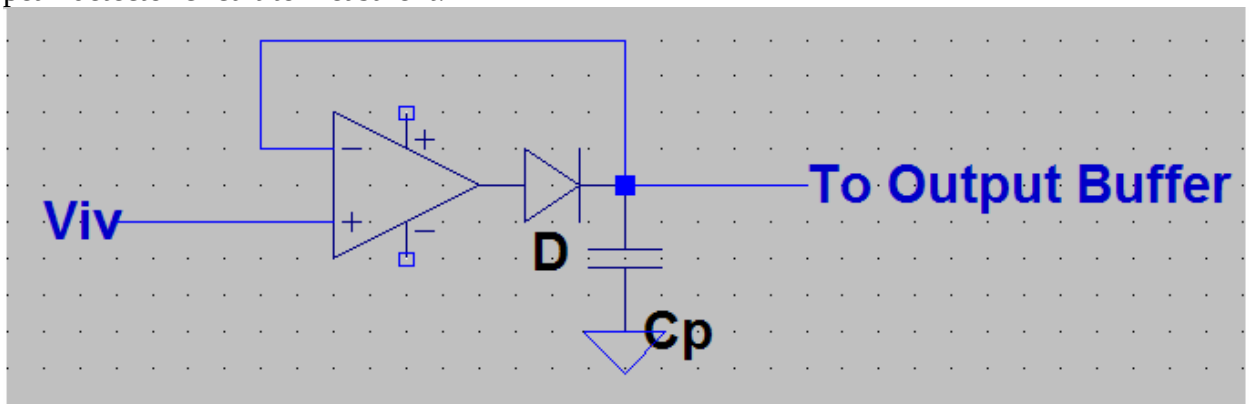
This is because in steady state, $\frac{d}{dt}[V_{dc}]$ is zero.

The voltage measured at the output of current to voltage converter is

$$Viv = I \times R_f = K \times A_0 \omega R_f C \times Cos(\omega t) \quad (5)$$

Where R_f is the resistance in the feedback path. And the K is ideality factor for the OP AMP used in the circuit. This is found experimentally.

This step does the function of current to voltage conversion, as well as providing gain. This ac voltage's amplitude is directly related to the capacitance of the MOSCAP. So we are using a peak detector circuit to measure it.



Ideally, the output of the peak detector, Vp should be the maximum value of Viv

$$V_p = KA_0 \omega R_f C \quad (6)$$

And the output buffer is a simple voltage follower, thus Vout=Vp. As we can see, if we measure this Vout, we can easily find out the DUT capacitance C, as we already know A_0 , ω , R_f ,K.

$$V_{out} = KA_0\omega R_f C . \quad (7)$$

Unfortunately, the relation between the peak of sinusoidal signal input to the peak detector, and the value of DC output voltage obtained at the output of circuit is only approximately linear. We have experimentally found that relation for the particular IC we are using. Now, if more accuracy is required, the real input voltage peak Vp* is found from a look up table, which has an already stored array of input and corresponding voltage of the peak detector circuit.
Then the final equation is

$$C = Vp^* /(KA_0\omega R_f) \quad (8)$$

Now, the software implemented in the microcontroller/computer should do the following jobs:

1. Generate a DC step waveform sweeping from -3 to 3 volt form DAC
2. Measure V_p through ADC
3. Find out V_p* form the look up table.
4. Calculate Capacitance from Eqn (8)
5. Generate an Array of C and corresponding Dc bias input V_{dc}.

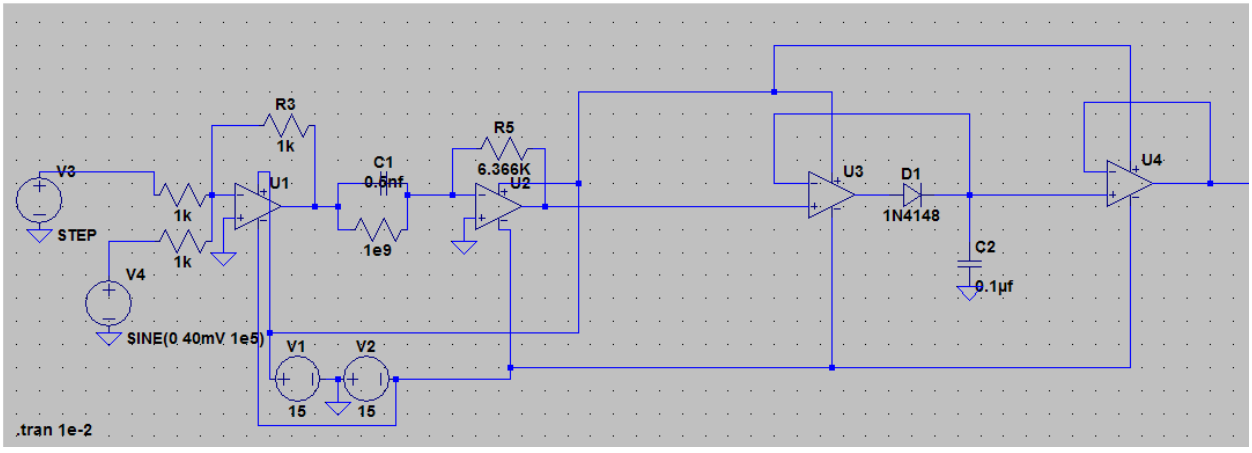
5. Circuit Design:

Analog Part

Waveform Generation:

We can use MAX038 IC for required waveform generation. Instead, we can use function generators in the lab to provide the same. We have tried to build our own waveform generator. But in testing, we would be using function generator in lab, due to its flexibility.

Overall circuit diagram :



The MOSCAP biasing circuit

Here we wanted to superpose the small signal ac voltage on the dc step voltage. So we have decided to use a unity gain voltage adder. The small signal is of 100Khz. We have decided that op amp LF357 would be ideal for this purpose. This has wide GBW of 20Mhz, settling time of 1.5us, and a slew rate of 50 V/us. LF357 is also unity gain stable, and there is hardly any attenuation in the given circuit at 100 KHz.

The Current to Voltage converter circuit

Here, wee need to convert the small current through MOSCAP, to a larger voltage value. We needed an op amp which will have a high gain at 100Khz, and with high input impedance, to minimize the error due to offset current. We have chosen LF356, a FET input op amp with GBW of 5Mhz.. LF 357 would have been a better option due to its high GBW of 20Mhz, but there were some practical difficulties in using LF357 [Appendix 1].Hence we have put LF356 instead of LF357 is the final circuit for demo.
Also, it was noted that the value of k as mentioned in eqn () was 1.32.
Presently, we were dealing with MOSCAPs with a capacitance in the range of 1nf to 0.1nF. We need to use the range of ADC most effectively within 0 to 5 volt. Now consider following two cases:

1. C=0.1nf, Rf=150K, f=100KHz, A0=40mV. And K=1.32

Then $V_p = KA_0\omega R_f C = 0.497$Volt

2. C=1nF, Rf=150K, f=100KHz, A0=40mV. And K=1.32

Then $V_p = KA_0\omega R_f C = 4.97$ Volt.

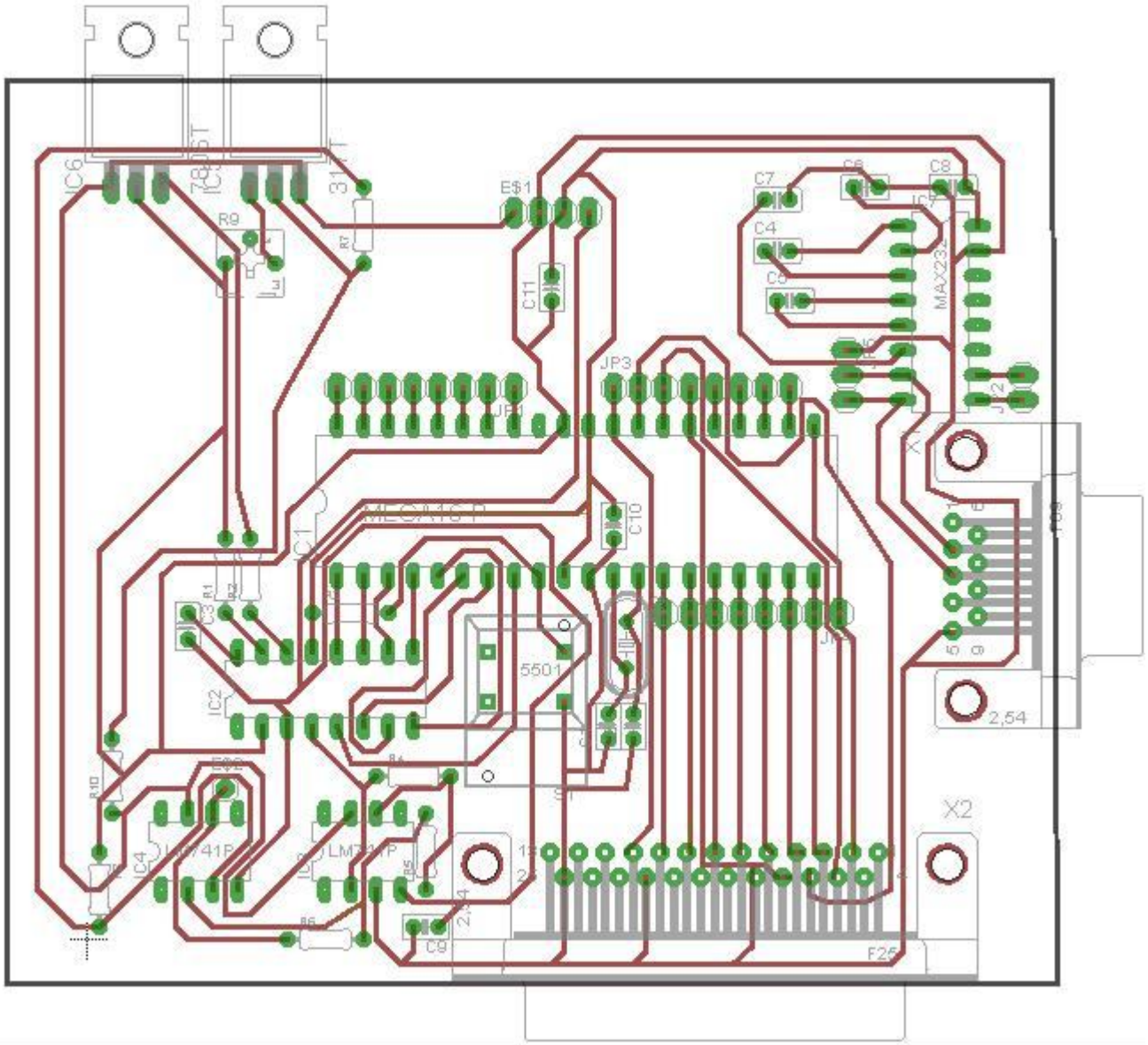
This means as the value of the capacitance varies from 0.1nf to 1nf, the Vp varies from 0.497v to 4.97 v. In this way, we can minimize the quantization error by using the range of ADC effectively. Hence the value of Rf was chosen to be 150K. If we needed to improve the range of CV meter by a factor of 10, just reduce the Rf by a factor of 10 to make it 15K. This process is limited by the minimum voltage at which peak detector gives non zero output.

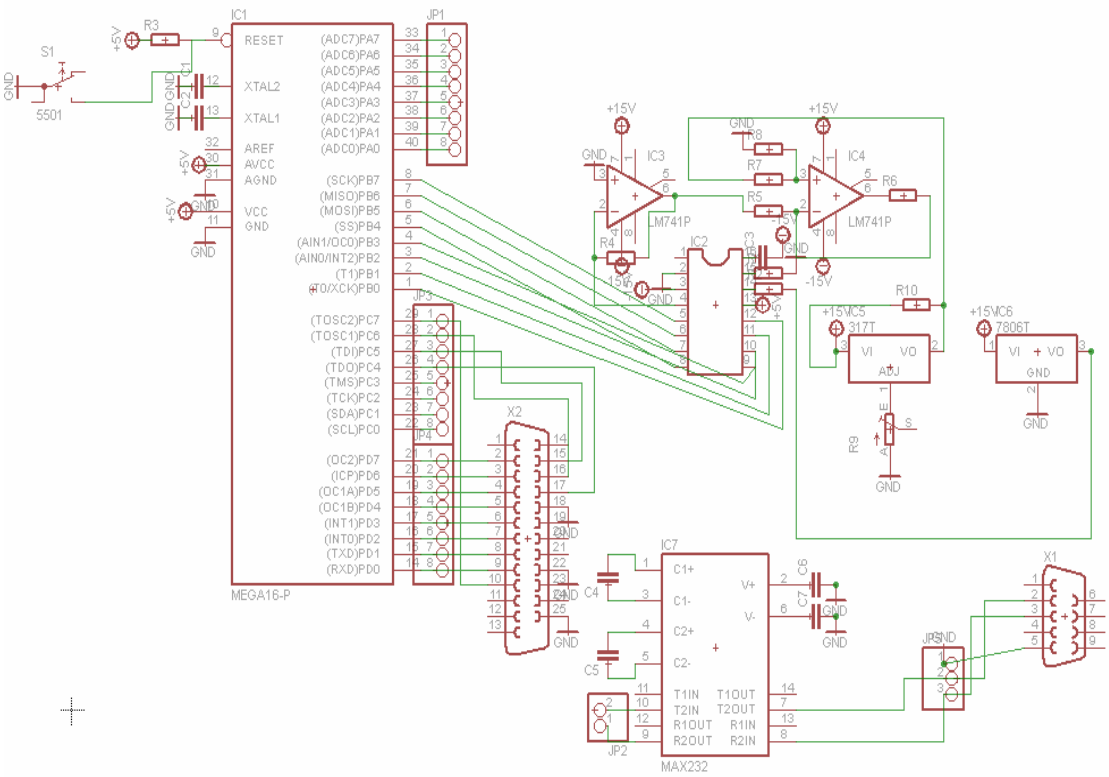
The Peak Detector Circuit

Here, we required an op amp with High input impedance(so that the capacitor charge will not leak as op amp offset current) and high slew rate, so that the voltage measured across the capacitor will follow the peak properly. LF 357 is used here also, due to its desirable properties.
The value of capacitor should not be very large, as then its charging will be limited by the SR of Op amp. Also, it should not be very small, as otherwise, instead of maintaining the flat peak of the signal, the output will start following the input. Experimentally, best results were obtained with Cp=0.1uF.
The relation between DC output of peak detector circuit (Vp*), and the actual value of the peak sinusoidal input to it (Vp), is found experimentally. And we have got an approximately linear relation there. Since Vp* is less than Vp, we are not stretching the ADC to its limits by making input to it as large as 4.97 v as mentioned in last section.

Digital part :

Digital Part PCB





As described in the introduction, the capacitance of MOSCAP changes with applied DC bias. Since we are interested in characterizing the MOSCAP, we need to apply a variable dc bias along with the small signal sinusoidal voltage. A DAC has been used to provide a rising step voltage for this purpose. The step size was decided in the following way:

Amplitude of sinusoid = 40 mV
⇨ step size > 40 mV
The essence of C-V characteristics of a MOSCAP can be captured in the voltage range -3V (accumulation) to +3V (strong inversion).
Hence, a range of 6V is required.
Thus, maximum number of steps = 6V/40mV = 150
Maximum number of bits = $\text{Log}_2(150)$= 7.23

An 8 bit DAC (DAC0808) was thus chosen and the number of steps was halved using software. Using a reference voltage (Vref) = 6V, and subtracting the output from a fixed 3V voltage, the ladder voltage function has been generated.
A simple operational amplifier circuit using LM741, has been used to carry out the subtraction part.

Choice of microcontroller

The project demanded the following from the microcontroller

- Ability to control a DAC which could generate the rising step voltage.
- An inbuilt ADC which could sample the output from the analog part
- Communicate the data to a computer where the final C-V plot may be generated.

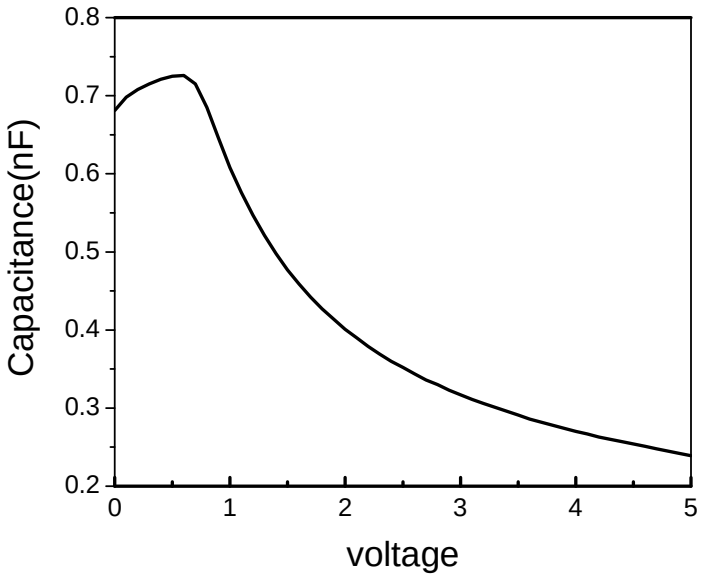
Atmega16 was selected because of the following reasons
First, it has an inbuilt 10-bit ADC which provides an accuracy of ±2 LSB. We are using only the first 8 MSBs. It has 4 ports, one of which has been used for input selection of ADC (PORT A). PORT B is used for giving input to DAC. The remaining two ports are for data transfer to the computer.

Data transfer

Provisions of both parallel port and serial port have been provided on the PCB.

6. Testing Procedure:

We have got a MOSCAP wafer, mounted on a special stand. It has two wires coming out of it: gate and substrate, which can be straight away inserted in the place of the DUT. We have also found out the CV characteristics of this MOSCAP wafer by a commercial CV meter.



As it can be seen, the capacitance of this wafer lies between 1 to 0.1 nF. The bias voltage for negative range is not shown due to some problem in that device. Now, for demo purpose, we have adjusted the range of our CV meter to be 1 to 0.1nf, to get best resolution.

Experimental Results and Discussion

Analog Part

Waveform Generator:
We had designed a waveform generator using MAX 038 IC. But it was not very flexible in terms of varying the frequency and amplitude. So while testing purposes, we have used the function generator in the LAB.

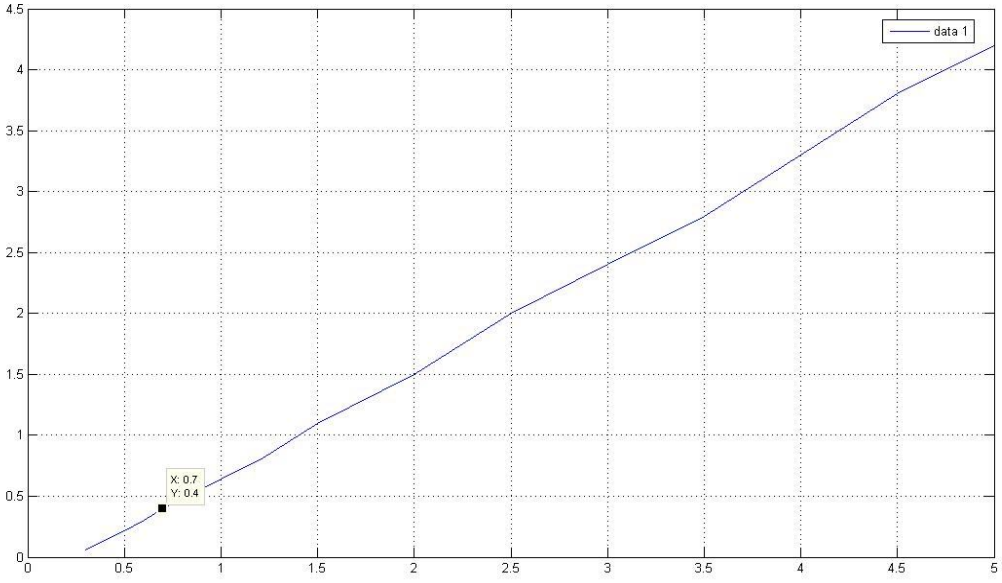
MOSCAP Biasing circuit:

We had initially simulated the circuit using Switcher CAD, a PSPICE tool. The results were satisfactory, and hence the op amp adder configuration was selected for this purpose. The experimental results with the IC LF357 were quite good, and hardly any detectable attenuation was present in the output.

The Current to voltage converter circuit:

The value of K was measured by comparing the expected output voltage= $A_0 \omega R_f C$ and the actual out put voltage = $KA_0 \omega R_f$ Thus Actual/Expected gave the value of K. This K was found for various values of capacitances between 0.1nF to 1nF. And it turned out that approximately, K=1.32 .

The Peak Detector circuit:
The relation between the Vp and Vp* is shown below. Where the y axis shows Vp* and X axis shows Vp. They are approximately related by following equation:

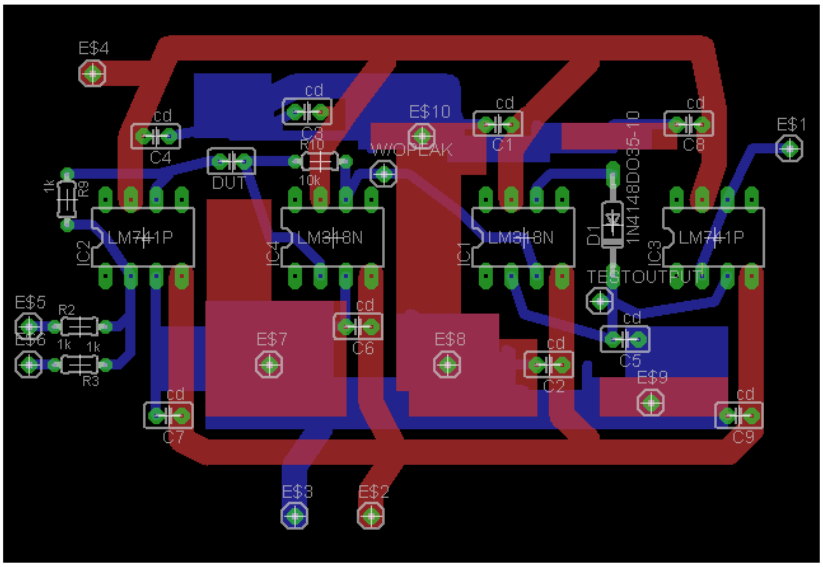


PCB Making:

Since we were using high frequency with small amplitude signals, extra care was required to be taken while designing the PCB. Following guidelines were followed:

1. Keep power lines and signal lines at opposite sides
2. Keep power lines wider
3. Put a ground plane in the open space left anywhere in the board.

The Analog PCB



7. Conclusion and suggestions:

Thus we have designed a CV meter for the measurement of CV characteristics of the MOSCAP. Though a robust product was not fabricated, a proof of concept has been given by our efforts.

Suggestions for further development:

1. Use SMD components for lesser parasitic capacitances
2. Use a USB for data transfer to the computer
3. Use advanced methods and shielding for reduction of the noise in the circuit.

Appendix 1

Unfortunately, we found out that very few pieces of LF357 follow the specs given in the datasheet. So the reliability of the device was very poor. So, it has been used only in circuits which have a constant value of the gain.

Appendix 2

Documentation: We had formed a google group for this EDL, and we used to store the important/relevant documents on that group. We had also decided timelines, but unfortunately, could not follow them accurately. But we have been documenting the work we have done for this EDL on a daily basis on a goodle doc.

References:

1. User manual of PAR410 capacitance meter
2. User manual of HP 4284A Precision LCR meter.
3. SEMICONDUCTOR MATERIAL AND DEVICE CHARACTERIZATION, Third Edition, Schroder