LOCK IN AMPLIFIER

EE318: ELECTRONICS DESIGN LAB I REPORT

GROUP 6

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THE DESIGN PROBLEM

The lock in amplifier uses the powerful tool of phase sensitive detection to extract signals from conditions where the noise has overwhelmed the signal of interest.

Phase Sensitive Detection:

A lock-in, or phase-sensitive, amplifier is simply a fancy AC voltmeter. Along with the input, one supplies it with a periodic reference signal. The amplifier then responds only to the portion of the input signal that occurs at the reference frequency with a fixed phase relationship. By designing experiments that exploit this feature, it's possible to measure quantities that would otherwise be overwhelmed by noise.
The lock-in amplifier operates on a very simple scheme:
Consider a sinusoidal input signal,
$V(t) = V_0 \sin(\omega t + \varphi)$.
Suppose we also have available a reference signal
$V_R(t) = \sin(\Omega t)$.
The product of these two gives 'beats' at the sum and difference frequencies
$V_R(t)\, V(t) = V_0 \{ \cos[\omega t - \Omega t + \varphi] - \cos[\omega t + \Omega t + \varphi] \}$

Thus now if we pass this signal through a low pass filter: we will only get those frequency components of this signal which are close to zero frequency. Thus only the component of the input signal with $\omega = \Omega$ and constant phase difference with the reference φ will appear at the output. All the other frequency components are forced to zero. Also the random noise signal with frequency component Ω will be forced to zero due to its non-constant phase. This is what works behind the powerful extraction techniques using a lock in amplifier. Thus even noise very close to the reference frequency is removed attenuated by a large amount.

Thus the output of the LIA will be low pass output of
$V(t)\, V_R(t) = V_0 \{\cos[\phi] - \cos[\Omega t + \phi]\}$ with $\omega = \Omega$
=> Output = $V_0 \cos[\phi]$
If we know ϕ we can find V_0 *from the output, this presents another part of the design problem to find* ϕ.

The design of a Lock in amplifier requires considering the following aspects:

1)Signal preprocessing: Here we make the signal favorable for the hardware that performs phase sensitive detection. Primarily the way we implement multiplication in hardware requires certain minimum voltage level of the signal to be properly multiplied. Thus we can perform some amplification and simple filtering in this stage**.**

2)**Phase Sensitive detection:** To perform phase sensitive detection we need to multiply the signal with a sinusoid of the reference frequency. In digital domain this is easy. However in the analog domain we do this by multiplying the signal with a square wave which is just a switching operation in hardware.

A square wave is essentially a sum of odd harmonics of the reference frequency written as:

$$x_{\text{square}}(t) = \frac{4}{\pi}\sum_{k=1}^{\infty}\frac{\sin\left((2k-1)2\pi ft\right)}{(2k-1)}$$
$$= \frac{4}{\pi}\left(\sin(2\pi ft) + \frac{1}{3}\sin(6\pi ft) + \frac{1}{5}\sin(10\pi ft) + \cdots\right).$$

Thus multiplying the signal with the square wave followed by a low pass filter gives a sum of all odd harmonics components in the signal scaled by these coefficients. If the signal of interest has just one component of frequency matching with the reference frequency, the low pass output will be dominated by the frequency component of the reference frequency. This is also the job that requires signal preprocessing (during which we remove all signal frequency components away from the reference frequency).

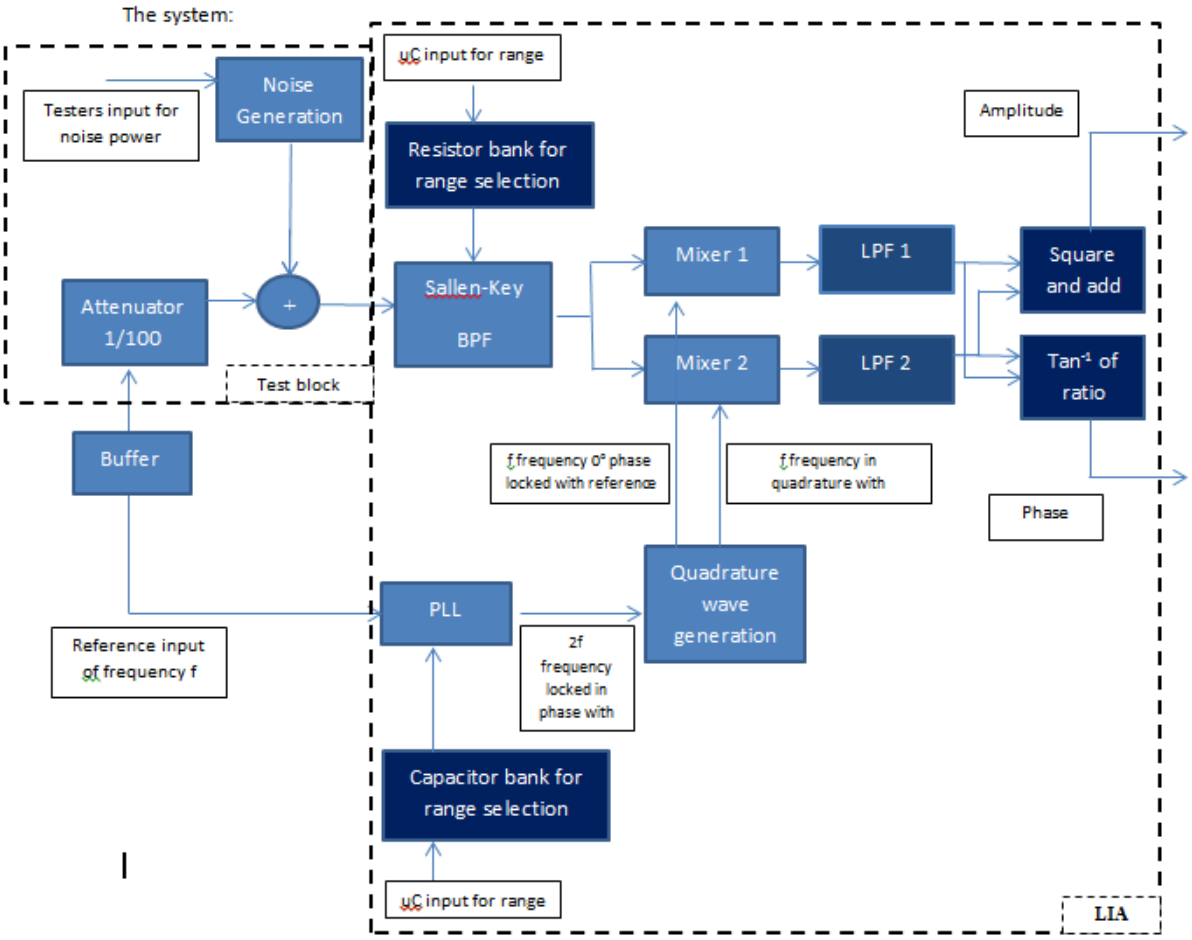
3)**Phase Measurement**: As seen the output is of the form $V_0 \cos[\phi]$. Thus we need to measure ϕ somehow to be able to completely describe the signal using the pair (V_0, ϕ).
One way to do it that we took is to perform the phase sensitive detection in two parallel channels 90 degrees out of phase. Thus the outputs of the channels will be of the form $V_0 \cos[\phi]$ and $V_0 \sin[\phi]$.
From here we can easily find both V_0 and ϕ.

4) **Input reference signal lock:** The LIA takes in a reference signal which need not be a sinusoid or square wave. It can essentially be any periodic signal with a fixed frequency and we then internally generate a signal locked in phase and frequency to the fundamental harmonic of the input reference. Also for phase measurement we require two such internally generated switching signals 90 degrees out of phase.

5)**High Q, low cut-off low pass filter:** The low pass filter forms a very essential part of the LIA. It provides the DC output corresponding to the amplitude of the signal at reference frequency and thus better the low pass filter less will be the effect of noise at the adjacent frequencies. Digital filters are good in this case because they can be designed for very low cut off and high quality factor however one has to overcome the problem of quantization errors and dynamic range to meet the required specs. However Digital filters do not face the problems of non-linearity and ambient noise effects.

In the coming sections, we will describe how each of these blocks were implemented and the pros and cons of the adopted method.

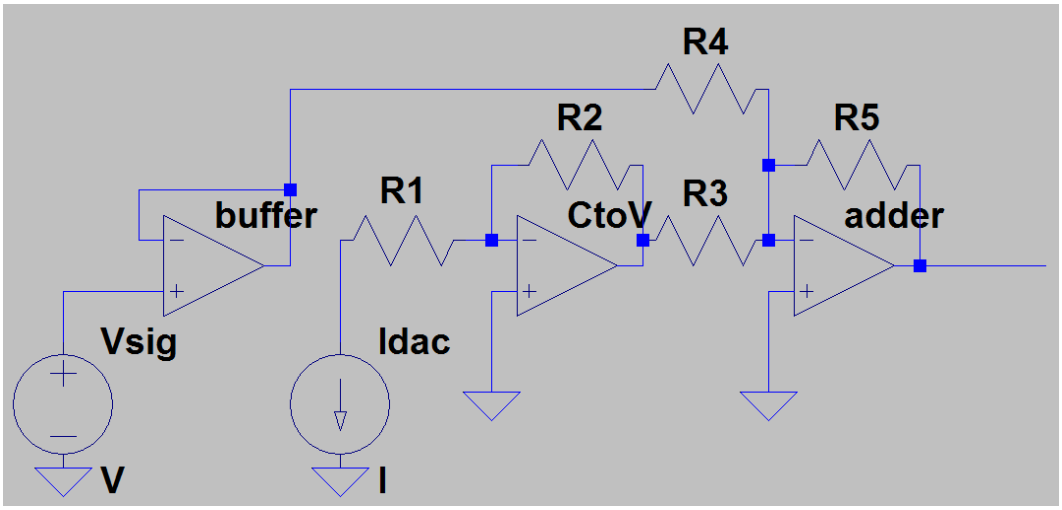
BLOCK DIAGRAM OF THE LIA SYSTEM



IMPLEMENTATATION OF BLOCKS:

1) Test block:

The system is put in place for distorting the original signal and in a way simulates a real life system under test/ measurement. It has a simple inverting adder that attenuates the signal by a factor of 100 and adds a white Gaussian noise of set power. The white Gaussian noise is generated by passing a pseudorandom variable to a DAC by means of a uC code written to send pre calculated values of a WGN variable.



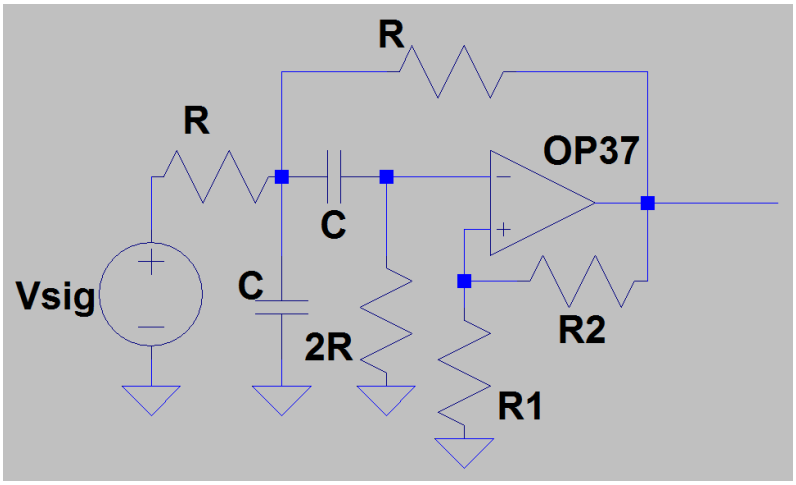
For the noise hence generated, we have the value of the noise variance given by:

σ_{noise} = σ*(Vref/256) where σ is the variance of the computer generated WGN and V_{ref}/256 is the scaling factor that converts the 8 bit numbers via the DAC and the I to V converter to voltage.

Thus the output of the test block is inverted signal of V_{sig} attenuated by a factor of 100 with cyclo-stationary White Gaussian Noise of mean -V_{ref}/2 and variance (127/3)*(Vref/256) = V_{ref}/6.

2) **Signal pre-processing:**

We need to remove all frequency components in the input signal at the odd harmonics of the reference otherwise these will also get heterodyned to DC when mixing is done via the switching operation. As long as we are filtering the signal we can also amplify the signal as amplifying the signal at an earlier stage is better as compared to amplifying it later after our system components have added further noise to the signal. Thus our signal preprocessing block comprises of an LNA followed by a bandpass filter centered at the reference frequency of Sallen Key topology.



$$G = 1 + \frac{R_2}{R_1}$$

$$\text{Amplifier Gain } = \frac{\text{G}}{3 - \text{G}}$$

$$Q = \frac{1}{3 - G}$$

$$Center\ frequency = \frac{1}{2\pi RC}$$

In our design we need to remove all odd harmonics thus the bandwidth of the filter should be less than 2*center frequency which means that the Q factor must be greater than 2.

Keeping

R1= 10.22 kΩ

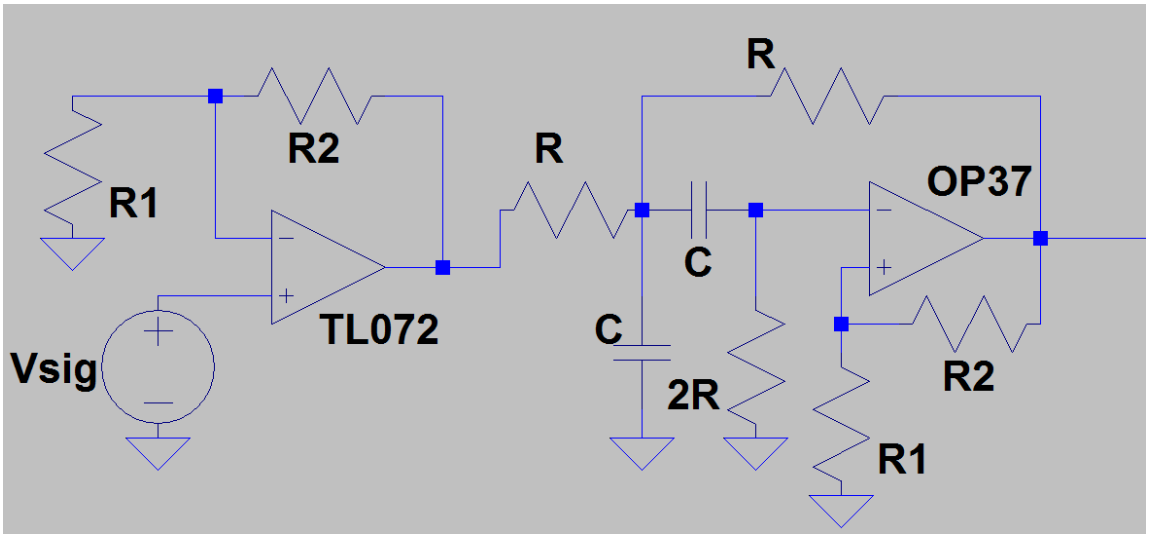
R2 = 17.8 kΩ

We get a fixed Q factor of 3.87 and an amplifier gain of 10.61

The Sallen key topology was chosen as it can be designed for a high Q factor, Gain and its center frequency can be fixed independently.

Although it is expected that this gain and Q factor should not change with center frequency, practically it was observed that when the center frequency is varied over a large range the gain drops as center frequency increases. This is due to the finite gain bandwidth product of the Op-amp. Thus we used the high speed dual swing Op-amp OP37 with a unity gain bandwidth of 63MHz.

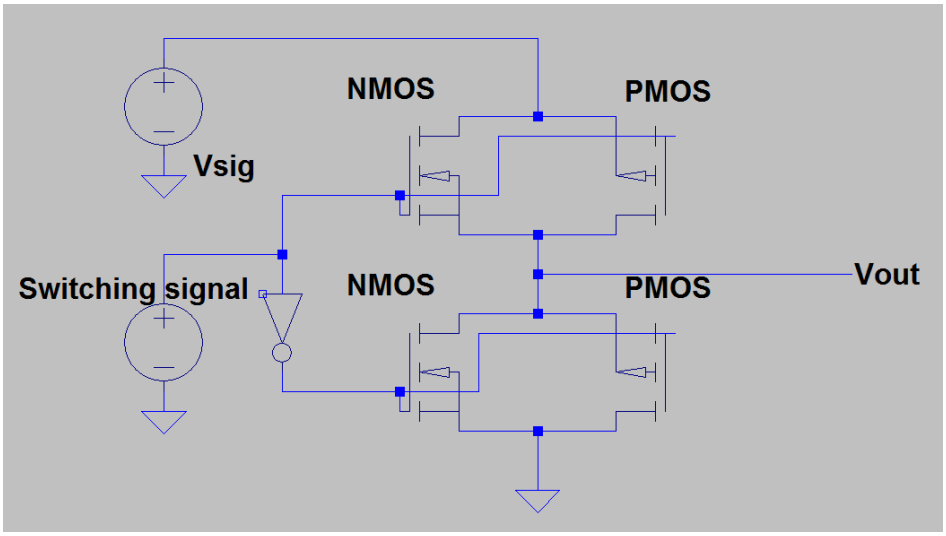
The LNA is made from a JFET input Op-amp (TL072) in the non-inverting amplifier configuration with a fixed gain of 11. The advantage of JFET input is in its high speed and low input bias current.



The Center frequency of the Sallen key can be changed simply by changing the resistor value R. For this we used digital potentiometer ICs from Analog Electronics (AD5421BRZxx) that can be controlled by I2C protocol from a microcontroller. For this we also wrote an automatic frequency detection code that would detect the frequency of the reference signal. Then we can accordingly set the value of R for the center frequency.
The overall performance of the preprocessing block at different center frequencies was as follows

Center Frequency	Input	Output	Gain
kHz	mV	V	
2	20	1.58	79
20	20	1.3	65

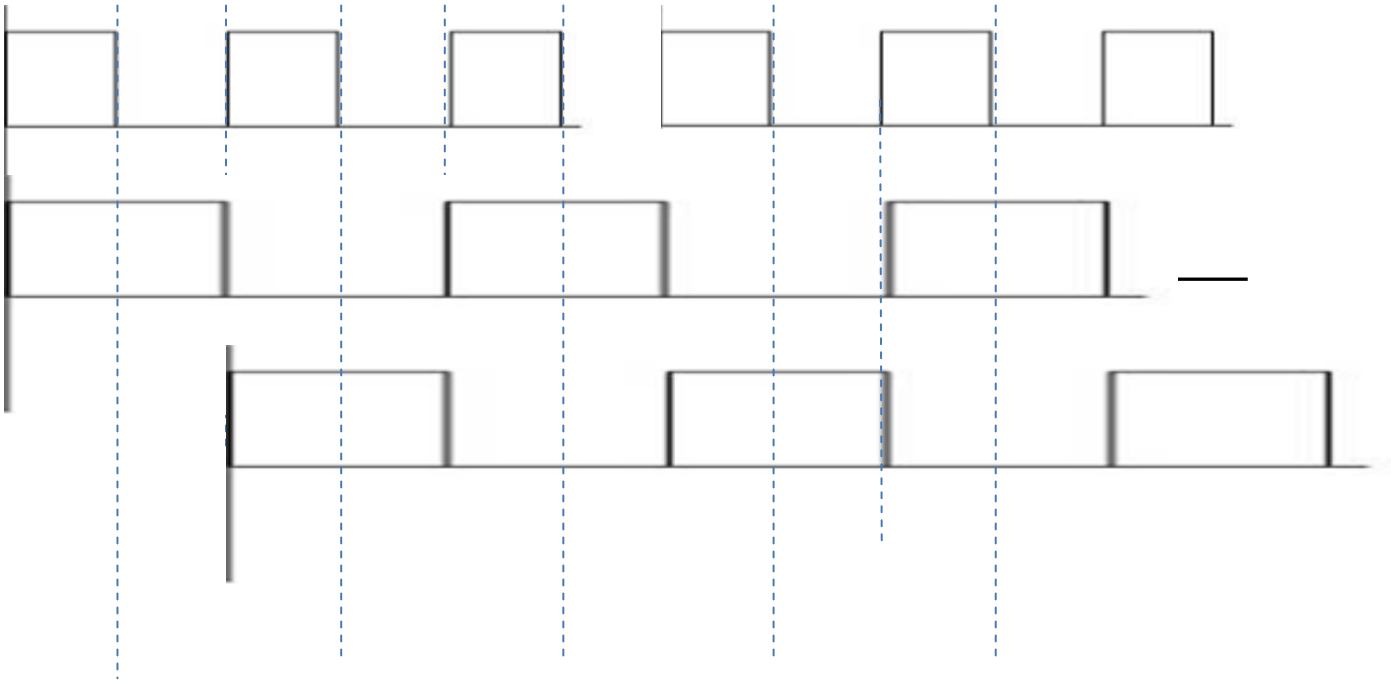
3) Phase Sensitive Detection:



The phase sensitive detection is performed by switching the output of the preprocessing block on two parallel channels with the switching signals 90 degrees out of phase.

Simple MOSFET switches (CD4007) were employed for this purpose. They were chosen as they add much lower noise to the output as compared to other options like the analog switches and have fast enough switching for our frequencies of interest (up to 100 KHz).

4)Internal reference signal generation:
We need two 90 degrees out of phase signals for switching.



We generate these as follows:

Toggling the output at each of the falling and rising edge of the signal gives two signals of frequency f which are 90 degrees out of phase. Thus to generate the required switching signals we need a 2f frequency wave. We obtain this by passing the reference frequency to a PLL with a divide by 2 counter in the feedback. Thus the PLL gives a 2f frequency locked in phase with this reference. The toggling is then done by simple edge triggered toggle flip flops operating at clocks 180 degrees out of phase.
Using the PLL, though simple, has the disadvantage of giving phase jitters and limited lock range which forces us to change a capacitor to switch between ranges.

5)Low pass filter:

The analog signals from the two mixer outputs is then given to an ADC and sampled by the uC.

However in our case as we were using Atmega16 the range of input for the ADC was 0 to 5V while the mixer outputs were going from -60mV to 60mV. Thus our mixer output had to be scaled and added to a DC offset to bring it into the range of the ADC. This is one of the problems that is always associated with the digital part of a LIA because as the range of amplitudes for the signal and noise conditions changes, the scaling factor has to be changed to get an optimum resolution.

Low pass filter design:

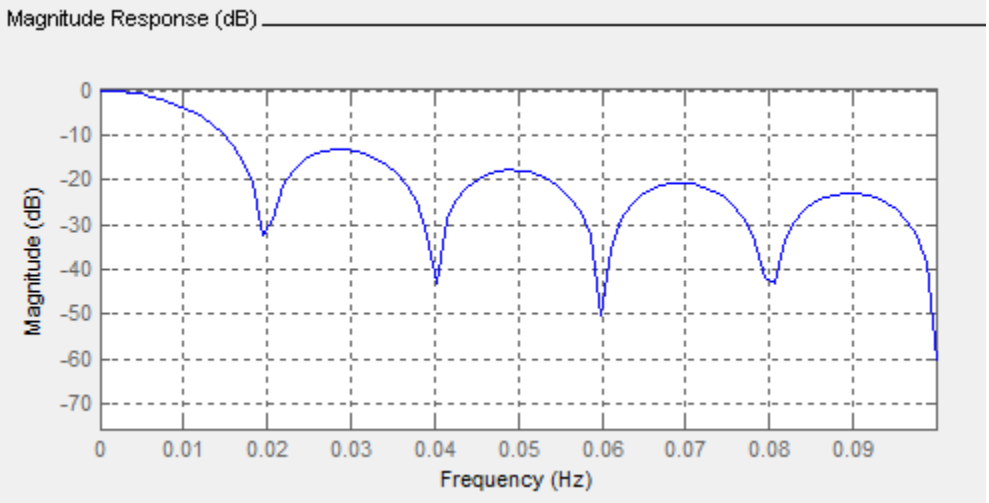
The sampling frequency is 40 Hz

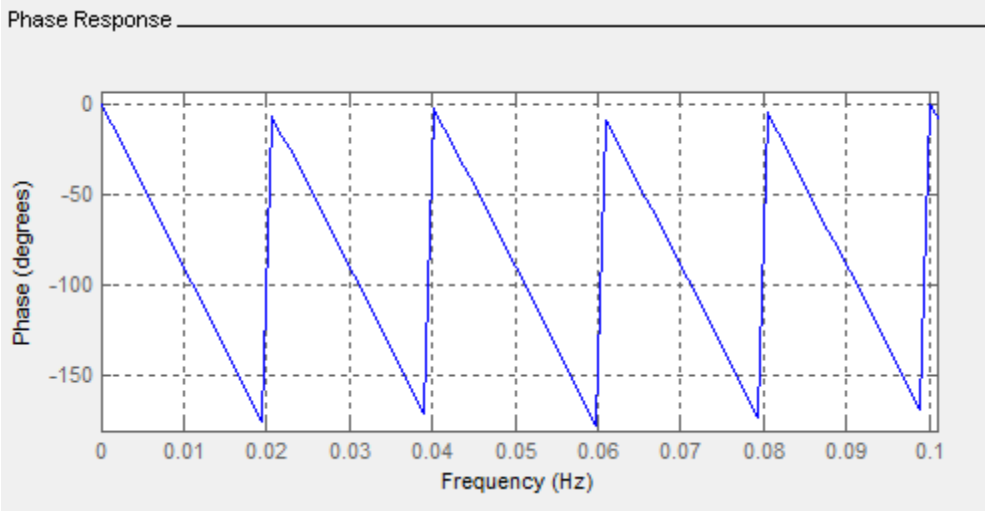
And low pass coefficients are:

$$h[n] = \begin{matrix} \frac{1}{1000} \text{ for } n = 0 \ldots 999 \\ 0 \; otherwise \end{matrix}$$

The ADC resolution is 10 bits with a reference of 5V thus we have quantization error of +/- 2.44mV

Thus the filter response is as follows:





The output of the lowpass filter acting on each of the channel is then used to find the amplitude and phase difference of the signal with the reference signal as follow:

$$V_0 = \sqrt{a_1^2 + a_2^2}$$

$$\varphi = \tan^{-1}\left(\frac{a_2}{a_1}\right)$$

Where a_1 is channel 1 output of the lowpass filter

a_2 is channel 2 output of the lowpass filter

6)Microcontroller interface to the PC:

The microcontrollers has the responsibility of sampling data from the hardware for the purposes of calibration, collection of result data, reference frequency detection and sends out data to the hardware for noise generation, range control.

The main job of result data collection is done via a 10 bit ADC and the result of conversion is sent to the PC by the USART with the RS 232 protocol. We have used a serial to USB converter in between the USART of the microcontroller and the laptop USB to allow the communication with USB as well.

CALCULATION OF NOISE POWER AND THE SNR

The noise for the experiment was generated from the computer. Using MATLAB, a sequence of random numbers was generated using the wgn function for White Gaussian Noise. These numbers were then read out randomly from the file using a C++ code, and were sent via USART to an ATMEGA 16. The ATMEGA 16 outputted the received numbers to a DAC connected on its PORT C. The 8 bit DAC has a reference voltage which is used to control the power of the noise in the signal. We go about deriving the autocorrelation and the noise power as follows.

The random numbers sent via USART have a Gaussian Distribution. The DAC displays the voltage corresponding to each random number for a fixed sample time T_o = 25ms. The windowing of the WGN results in the noise being colored. We observe that the noise at the output of the DAC is Cyclostationary White Gaussian Noise.

The Autocorrelation of the Cyclostationary WGN is a function of time t. We observe that the DAC noise is wide sense cyclostationary because the samples from which it is being generated are WSS. We can get the autocorrelation as follows:

"Generalization" of the Einstein-Wiener-Khinchin theorem for wide-sense cyclo stationary random processes: Let $X(t)$ be a WS cyclo S random process with "period" T_0. Then $X_S(t) = X(t+\theta)$ where θ is uniformly distributed between $-\frac{T_0}{2}$ and $\frac{T_0}{2}$ is WSS with mean

$$E\left[X_S(t)\right] =< m_X(t) >_t = \frac{1}{T_0}\int_{-\frac{T_0}{2}}^{\frac{T_0}{2}} m_X(t)dt$$

and autocorrelation

$$R_{X_S}(\tau) = E\left[X_S(t+\tau)X_S(t)\right] = \frac{1}{T_0}\int_{-\frac{T_0}{2}}^{\frac{T_0}{2}} R_X(t+\tau,t)dt$$
$$=< R_X(t+\tau,t) >_t = R_X^a(\tau)$$

where $R_X^a(\tau)$ is the time average of the autocorrelation function of $X(t)$. Then the power spectral density of $X(t)$ is defined as

$$S_X(f) = \mathcal{F}\left\{R_X^a(\tau)\right\} = \int_{-\infty}^{\infty} R_X^a(\tau)e^{-j2\pi f\tau}d\tau$$

For any random process $X(t)$, $E[X^2(t)] = R_X(t,t)$, thus if $X(t)$ is WS cyclo S

$$P_X = \lim_{T\to\infty} \frac{1}{T}\int_{-T/2}^{T/2} R_X(t,t)dt = \frac{1}{T_0}\int_{-\frac{T_0}{2}}^{\frac{T_0}{2}} R_X(t,t)dt = R_X^a(0) = \int_{-\infty}^{\infty} S_X(f)df$$

since $R_X(t,t)$ is periodic in t with period T_0.

We calculate $R_X(t,\tau = 0) = E[X(t+ \tau = 0)*X(t)]$, which is as follows:

$R_X(t,\tau = 0) = \sigma^2$; if $-T_o/2 < t < T_o/2$
$= 0$; else

From the above calculations we get
Pn (noise power) = σ^2
σ = Vref / 6 in our case.

This is because the per division voltage at the DAC output is Vref / 256 because the DAC is 8 bit. Also the standard deviation of the random numbers generated by MATLAB is 127/3.

Thus σ = (Vref/256) * (127/3) = Vref/6

Thus we get the noise power being introduced into the system.

RESULTS

The results for the LIA were taken at various values of noise power. The value of the output signal measured by the Low Pass Filter is tabulated with the input signal to the LIA. Also the SNR figures have been quoted along in the table.
In the observation tables below, Vref corresponds to the reference voltage given to the DAC which is generating the noise. Vi is the input voltage to the system. Vo is the output as measured from the LPF output. The frequency of the reference signal given to the LIA is 1.972 KHz.

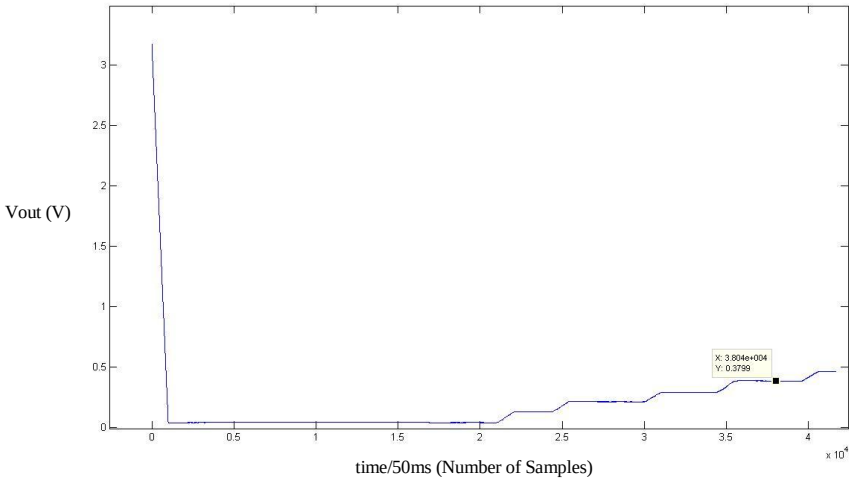
1. Vref = 0V (only ambient noise present)

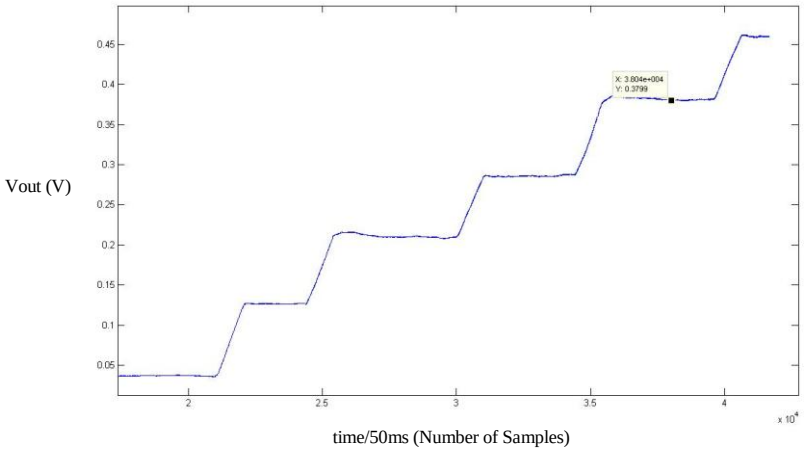
Vi (mV)	Vo (mV)	Phase (rad) (lag)
1	38	0.8
2	126	0.8
3	210	0.8
4	286.5	0.79
5	381	0.795
6	461	0.792

Here the reference voltage to DAC generating the noise is zero. As such no AWGN from the computer is being added to the signal at this stage. The only noise present is the ambient noise which is quite low compared to the signal.

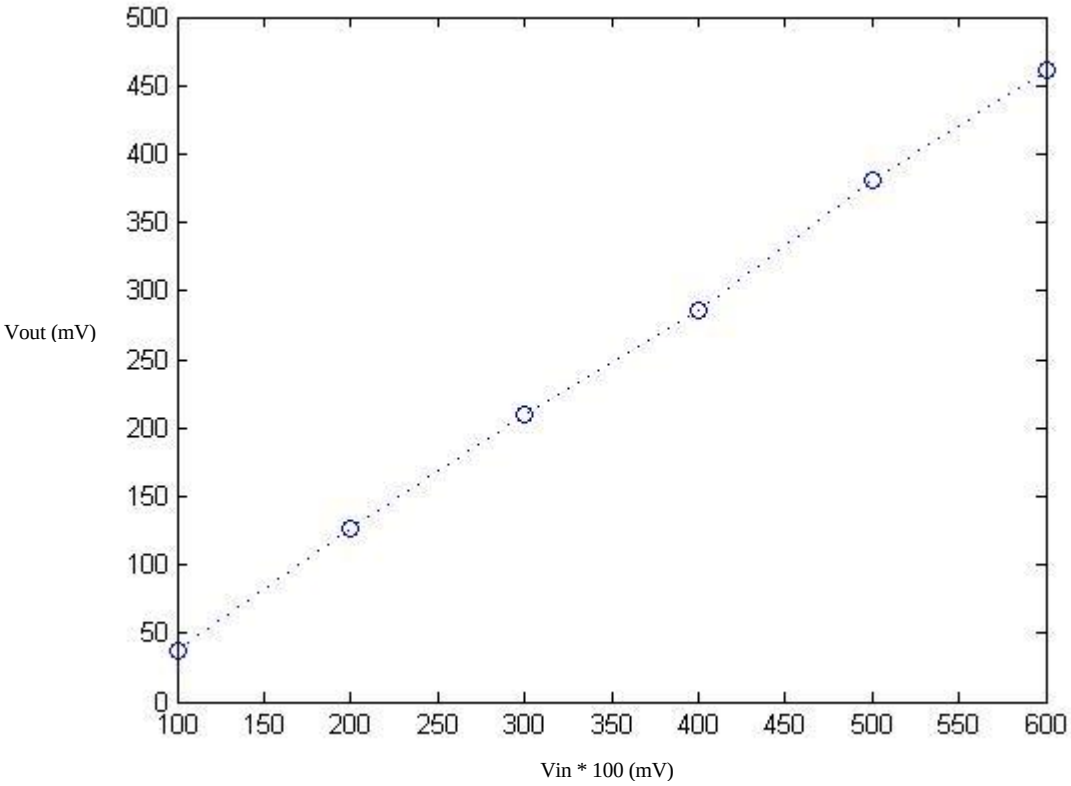
The phase seen is the phase difference between the switching signal and the input signal to the mixer.

The plot of the LPF output from MATLAB is shown below.





The plot of Vo versus (Vi *100) is shown below:

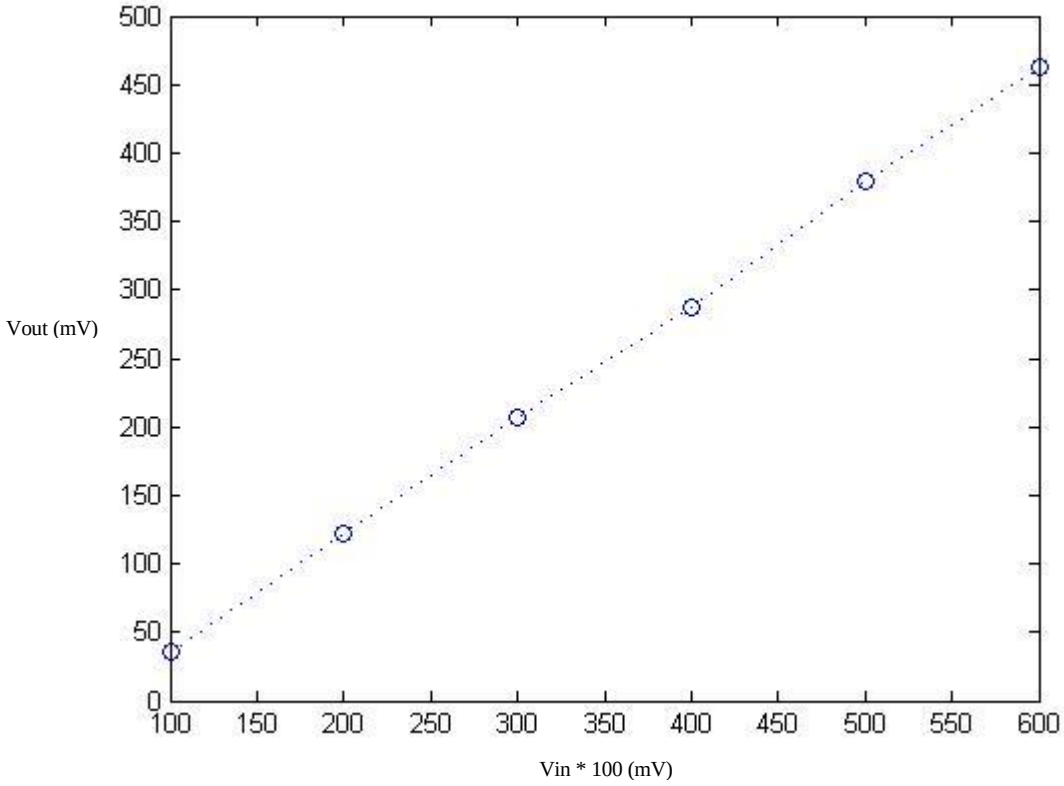


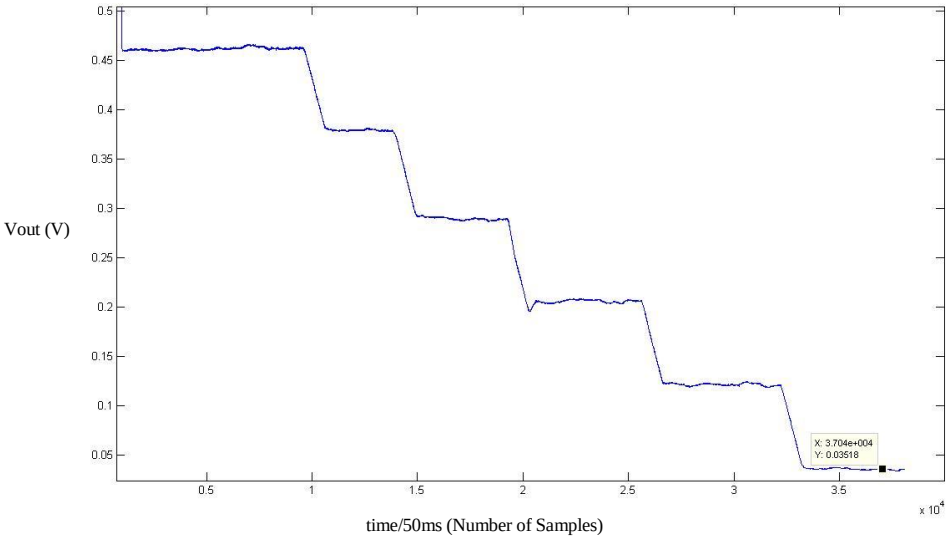
The above figure is a zoomed image of the previous figure. We can see the rise in the LPF output as the input voltage was increased in steps of 1mV.

2. Vref = 41.1mV; Pn (noise power) = (Vref ^{2})/36 = 4.69 * exp(-5)

Vi (mV)	Vo (mV)	Phase (rad)	SNR	Error %
1	35.2	0.79	0.010655869	7.368421053
2	122	0.78	0.042623475	3.174603175
3	207	0.795	0.095902818	1.428571429
4	288	0.792	0.1704939	-0.523560209
5	381	0.798	0.266396718	0
6	462	0.792	0.383611274	-0.21691974

Vo versus (Vi *100) plot is:

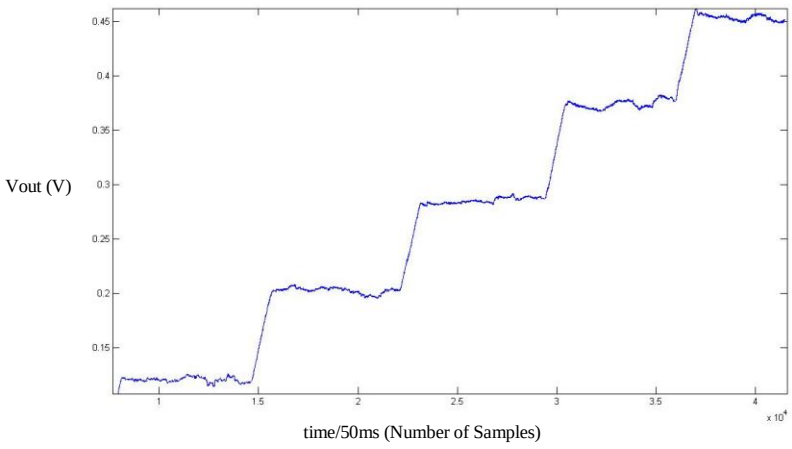




The output of the LPF is shown in the above figure. The Vi was decreased in the steps of 1mV each time.

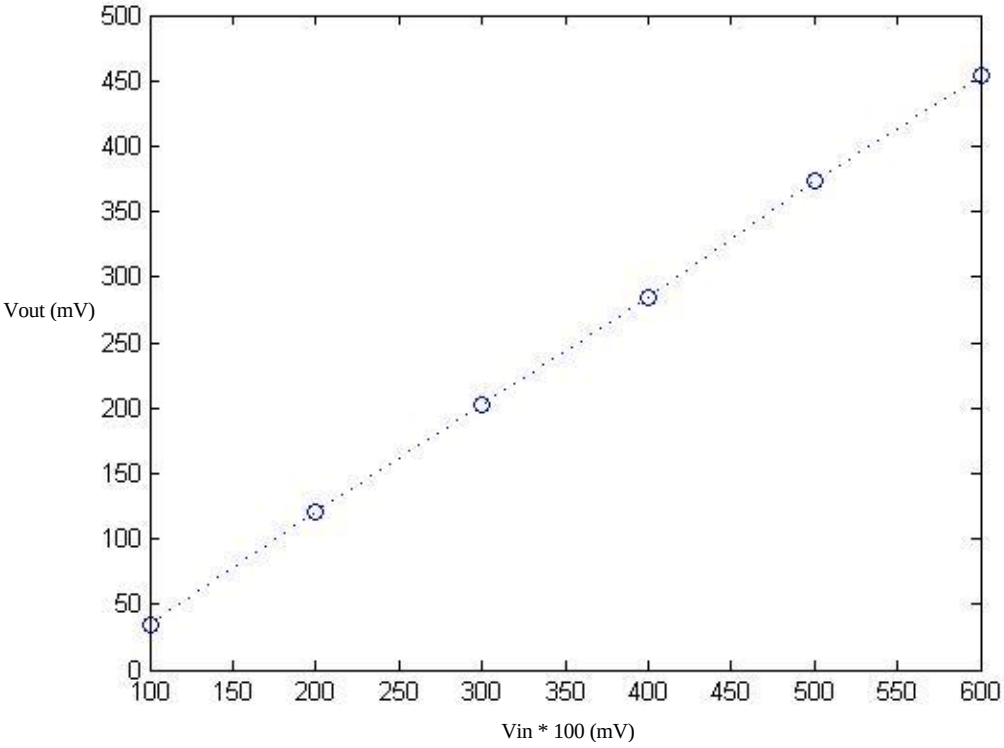
3. Vref = 99.7mV; Pn (noise power) = (Vref ^{2})/36 = 2.76 * exp(-4)

Vi (mV)	Vo (mV)	Phase (rad)	SNR	Error %
1	35	0.79	0.001810849	7.894736842
2	120	0.78	0.007243395	4.761904762
3	202	0.795	0.01629764	3.80952381
4	284	0.792	0.028973582	0.872600349
5	373	0.798	0.045271222	2.099737533
6	454	0.792	0.065190559	1.518438178



The above figure shows the LPF output. We can see now that because of the increased noise power, the output of the LPF is not very stable and deviates by a small amount from the expected result. This is an indication of the failure of the instrument to give correct results as the SNR decreases. We quantify this value a little later.

The Vo versus (Vi *100) plot:

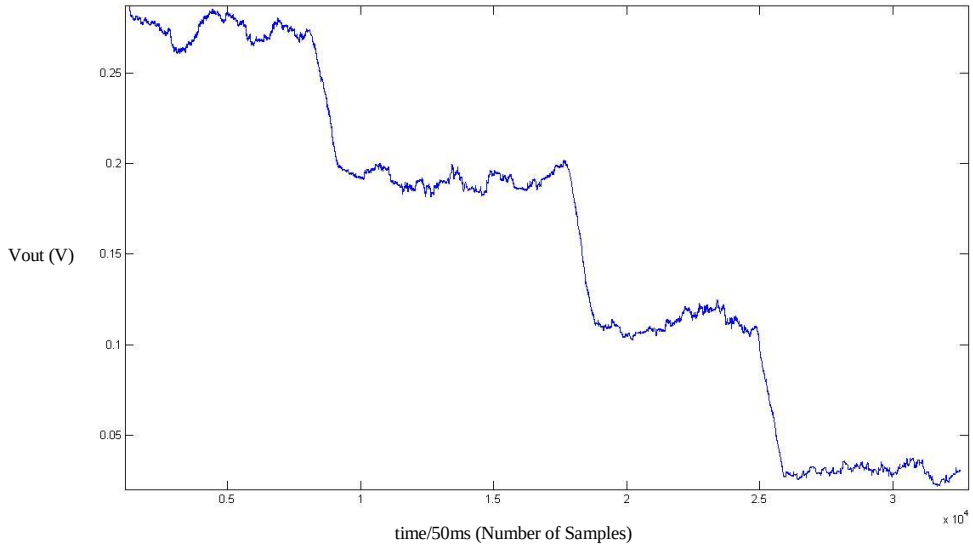


The plot is still quite linear which displays the ability of the instrument to work at these low SNR values.

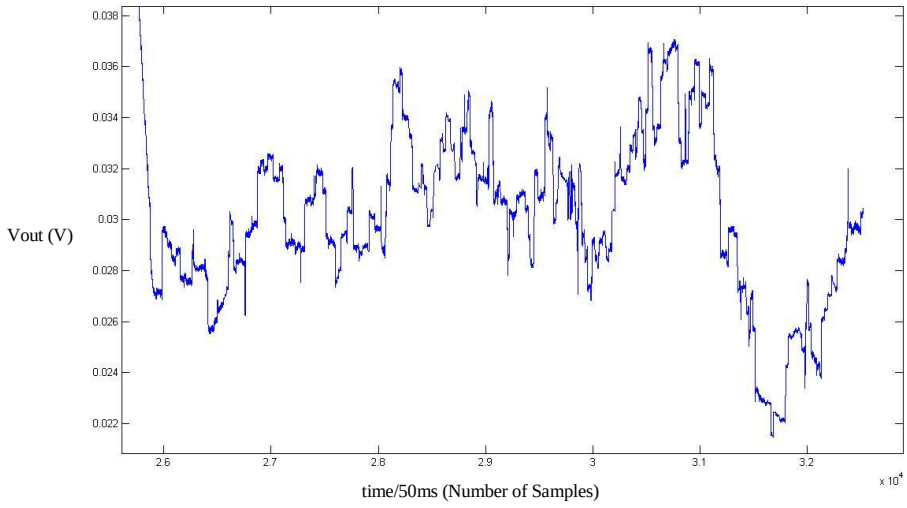
4. Vref = 202mV; Pn (noise power) = (Vref ^{2})/36 = 1.133 * exp(-3)

Vi (mV)	Vo (mV)	Phase (rad)	SNR	Error %
1	31	0.79	0.000441133	18.42105263
2	102	0.78	0.001764534	19.04761905
3	191	0.795	0.003970201	9.047619048
4	275	0.792	0.007058134	4.013961606
5	371	0.798	0.011028335	2.624671916
6	445	0.792	0.015880802	3.470715835

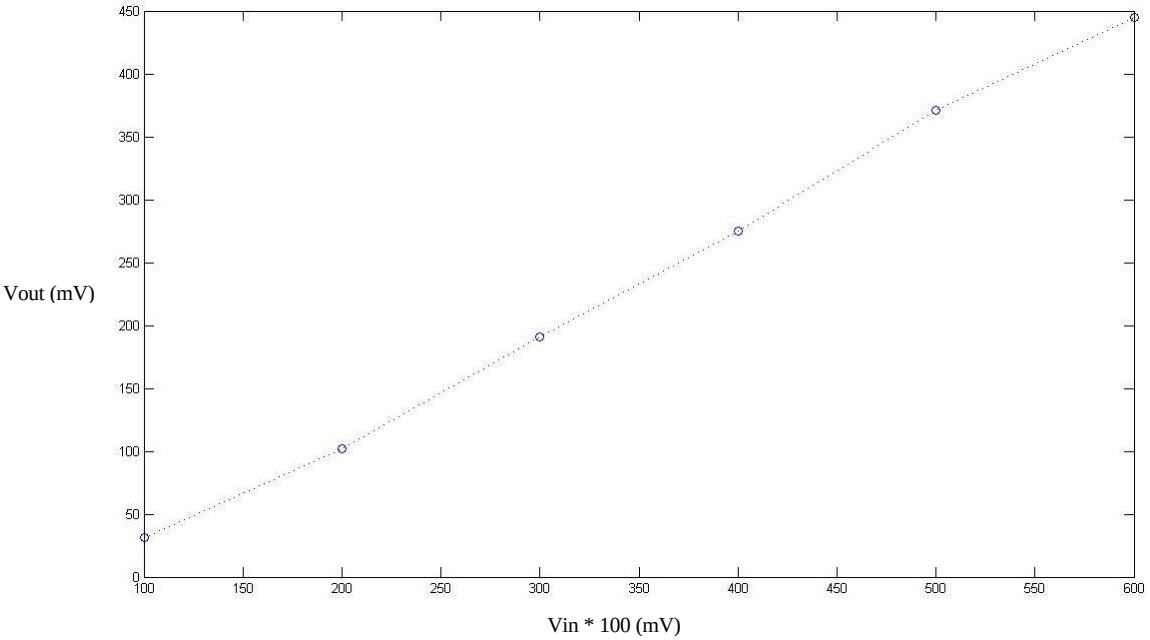
Here we can see that there a significant difference in the output values at low SNR compared to the values in case 1 where the computer generated noise was zero. We can see the failure of the LIA to work at such low SNR's in terms of the output of the LIA not stabilizing to a fixed value, but oscillating about some mean value. The observations in the table were taken by calculating the mean value of these oscillations.



A zoomed figure is shown below:



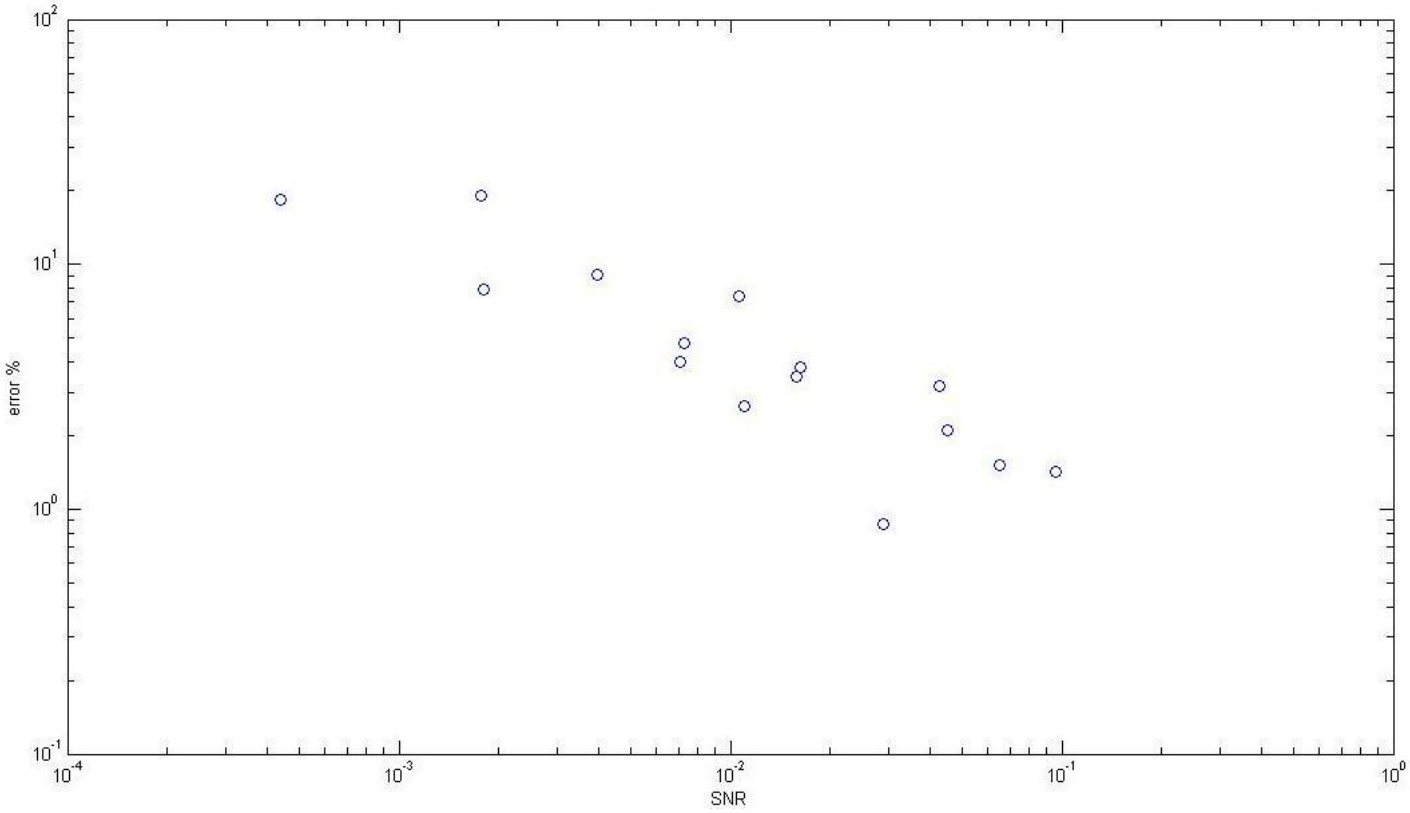
The above figure shows the variation of the LPF output for a fixed input. We can see the value to vary by around +- 10 mV. We should note here that the minimum resolution of the microcontroller ADC used to take in the output values is 5 mV. Hence the observed errors are quite reasonable for the resolution of ADC we have used.



The points plotted can be seen to be best fitting to a line, though the values at very low SNR are with large errors.

INFERENCES

The error percentage values calculated above were with respect to the values observed at zero added noise. Depending on the error percentage allowable in the measurements we can get a measure of the minimum SNR for which the system will work. A scatter plot of the error percentages with the SNR is shown below:



The above plot depicts the trend in the variation of the error % with the SNR. The error in the measurement increases with the decrease in SNR as expected.

REPEATABILITY OF RESULTS

The results obtained above were observed to be fairly repeatable. However there is slight variation in the results when experiments are repeated from scratch. The reasons for these variations can be stated as follows:

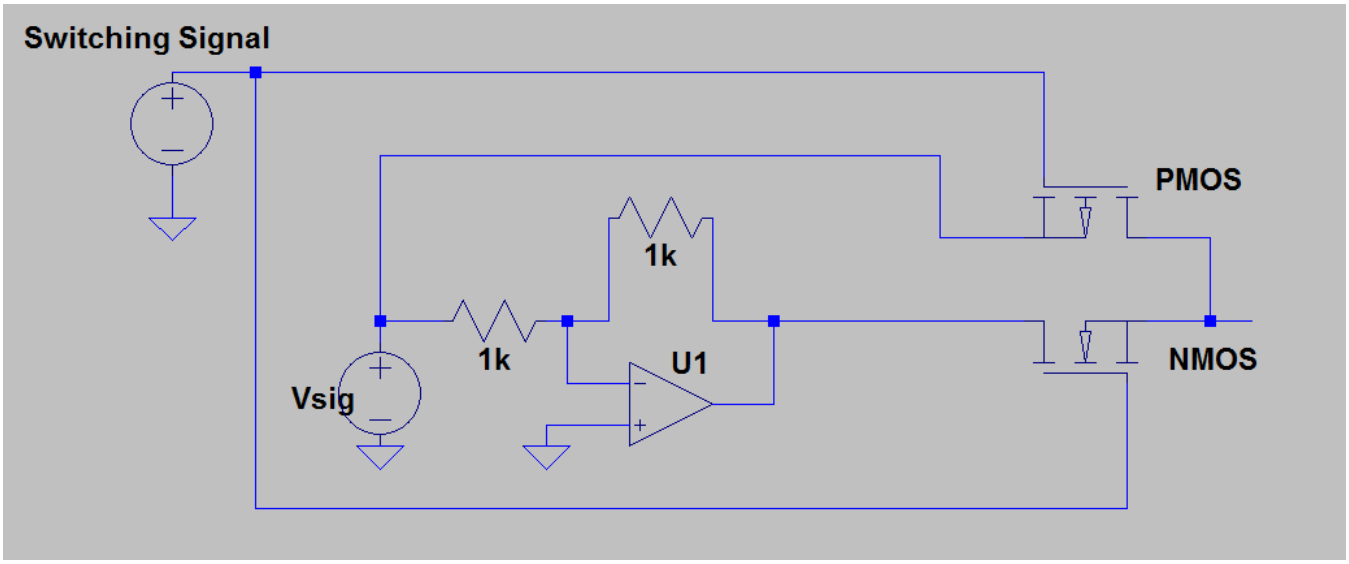
1) When the experiment is repeated it is not possible to maintain the exact same conditions such as the input signal amplitude or frequency.

2) During the ADC conversion we have added a DC offset which is a fraction of the supply voltage derived from a simple voltage divider. Thus when the supply voltage changes slightly between two experiments, we need to recalibrate the DC value to be subtracted from the low pass output to get back the signal amplitude. This problem can be solved if we used an ADC whose range can take both +ve and –ve voltages, thus avoiding this DC offset addition all together or by putting an auto calibration code at the beginning of power on.

IMPROVEMENTS IN THE PRESENT SYSTEM

Improved mixer:

Presently the mixer multiplies the signal with a 0-1 signal value which has an average of ½. A -1 to 1 bipolar signal however has a 0 average value. As a result the low frequency noise will still appear at the output in the low frequency region without any heterodyning however if we use a bipolar square wave all low frequency noise will be heterodyned to ω frequency and will be removed.
Moreover due to the average of ½ in the 0-1 wave and 0 average in -1 to 1 bipolar signal, the harmonic appearing in the output for a 0-1 signal multiplication are DC, ω, 2ω, 4ω, 6ω …. while with -1 to 1 signal the output will have harmonics at DC, 2ω, 4ω ….
Thus using a bipolar square wave for multiplication allows us to go up to much lower reference frequency ω for the same low pass filter at the end of the system.



The above circuit allows us to have a bipolar mixing giving the desired mixing by -1 and 1.

ADDITIONAL FEATURES IMPLEMENTED

The following blocks have been implemented however they have not been integrated into the current system.

1) Variable frequency control :

Currently the system implementation assumes an input frequency of 2kHz for the signal. The centre frequency of the Sallen key bandpass filter has been designed at 2kHz, with a Q factor of 3.87. Hence, with changing frequencies, we would have to change the hardware of the pre processing block to change the centre frequency.

We had conceptualized the implementation of the above system using a simple digital frequency detection block. This block assumes the input signal to be a square wave (in our case, we have the output of the comparator used to get a square wave from the input reference). The signal is tested for falling edges and the frequency is calculated by using simple hardware interrupts and timers.

For altering the centre frequency of the bandpass filter, we propose using digital potentiometers. These potentiometers alter the resistances R,R and 2R(refer Sallen Key filter schematic above). The values for the corresponding resistances are calculated using the formula for the centre freq of the filter. For a value of C=0.01uF, we have the current value of the resistances at 2kHz. Assuming that our system operates in a frequency range of 2-20kHz, we would have to increase the values of the resistors to 100kohm for achieving a centre freq of 20kHz.

The digital potentiometers tested for the above implementation consist of 3 basic types, mainly differing in the maximum resistances achievable. We have pots with maximum value of 10kohm, 100kohm and 1Mohm. We use a combination of 100kohm and 10kohm for achieving the above mentioned range. Thus the resistance resolution available is 10kohm/256 (each pot has a resolution of 8 bits).

R_{res} = 10kohm/256 ~ 39ohm

As such we have our frequency resolution given by approximately,

$f_{R+Rres} = 1/2\pi(R+R_{res})C \sim (1-R_{res}/R)/ 2\pi RC = f_R - R_{res}/2\pi R^2C$

Thus,

$f_{Rres,max}$ ~ 6Hz (for R = 10kohm)

As such, our resolution is always less than 6Hz.

We implemented the I^2C protocol to change the resistance values.

2) External 5 digit BCD Analog to Digital Converter :

The current system uses the internal ADC of the ATMEGA16 microcontroller, which has a resolution of 10 bits. We can improve the voltage sensitivity of our system by using an external 5 digit BCD. The current sensitivity of the system is 5mV, with the 10 bit ADC with a range of 0-5V.

The ADC mentioned above has a range of -2V – 2V which would give us a sensitivity of approximately 4/20000V = 0.2mV.

An added advantage of the above ADC is the removal of additional DC biasing circuitry required to shift the level of the mixer outputs to +2.5V. This would remove the noise added to the mixer outputs due to the DC level shifting circuitry. Additionally, it would also help in overcoming the repeatability issues with the system due to the removal of the DC corrective factors from the code for the LPF implemented in code.

3) Voltage protection circuitry :

The system has an upper level of operating input range, mainly due to the limits imposed in the CMOS ICs used in the switching mixer. For the same, the system needs to have voltage protection circuitry consisting of clippers to limit the input signal are every stage. This would help in making the system more robust w.r.t. the input signal amplitude given.

4) Calibration :

The final outputs displayed for the system are multiplied by a constant scaling factor due to the gains of the pre processing and the DC biasing circuitry. We expect these gains to vary slightly with varying frequency of the signal(assuming we have implemented variable frequency control). We need to have a pre calibrated set of values corresponding to the gains of the analog block at all possible frequencies, which can be done by giving suitable test signals at all frequencies possible by variable frequency control. Essentially we need to have a look up table of gains at all frequencies to suitable calibrate our LIA at all frequencies.

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