EE318 Electronic Design Lab Project Report, EE Dept, IIT Bombay

WIRELESS ECG MEASURING MODULE

Group 8

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ABSTRACT-

Our first aim was to create a portable fingerprint attendance reader. The idea was to make a device that can be used by the professors to take attendance in class conveniently and accurately. But due to late arrival of the fingerprint sensor we could not proceed on the idea as the time left was not enough for the completion of the project.

After discussions with Prof Jayanta and Prof Dipankar we finalized on two more spin offs from our project-

1) Wireless ECG machine
2) Device to measure the I-V characteristics on another two terminal device.

We designed the hardware such that it is capable of carrying out all the three above mentioned task.

What is ECG ?

Heart muscle cells are polarized at rest. This means the cells have slightly unequal concentrations of ions across their cell membranes. An excess of positive sodium ions on the outside of the membrane causes the outside of the membrane to have a positive charge relative to the inside of the membrane. The inside of the cell is at a potential of about 90 millivolts (mV) less than the outside of the cell membrane. The 90 mV difference is called the resting potential. The typical cell membrane is relatively impermeable to the entry of sodium. However, stimulation of a muscle cell causes an increase in its permeability to sodium. Sodium ions migrate into the cell through the opening of voltage-gated sodium channels. This causes a change (depolarization) in the electrical field around the cell. This change in cell potential from negative to positive and back is a voltage pulse called the action potential. In muscle cells, the *action potential* causes a muscle contraction. The sum action potential generated during the depolarization and repolarization of the cardiac muscle can be recorded by electrodes at the surface of the skin.

A recording of the heart's electrical activity is called an electrocardiogram (EKG).

The ECG is converted into electrical voltage by electrodes. A typical surface electrode used for ECG recording is made of Ag/AgCl, as shown on Figure 3. The disposable electrodes are attached to the patients' skin and can be easily removed.

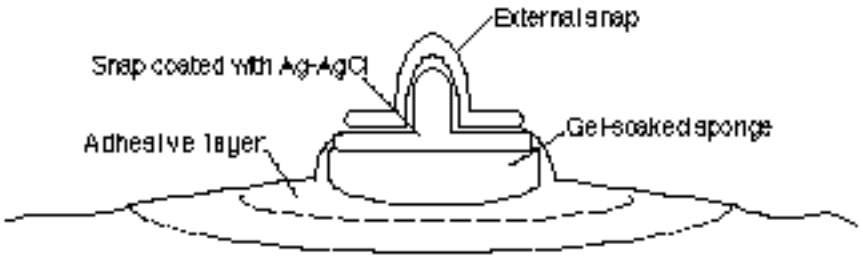
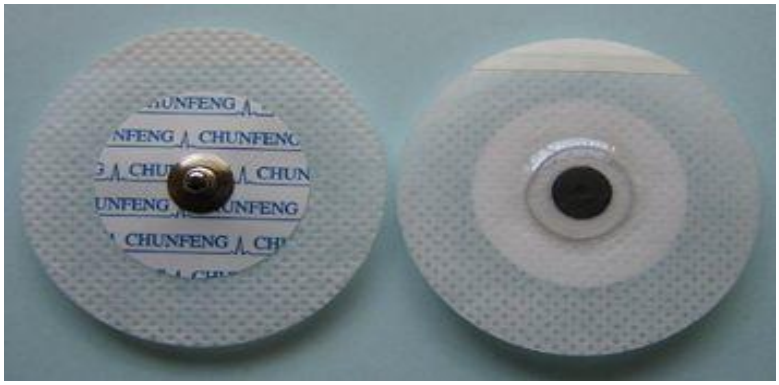


Figure 3 A disposable surface electrode.



The cardiac mechanism of ECG is shown on Figure 4. In the top figure, the electrocardiogram (ECG) initiates the cardiac cycle. The cardiac sounds are also shown. The bottom figure shows that ejection occurs when the pressure in the left ventricle exceeds that in the arteries.

Once the electrodes convert the ECG into electrical voltage, these voltage can be fed into an instrumentation amplifier, and then be processed.

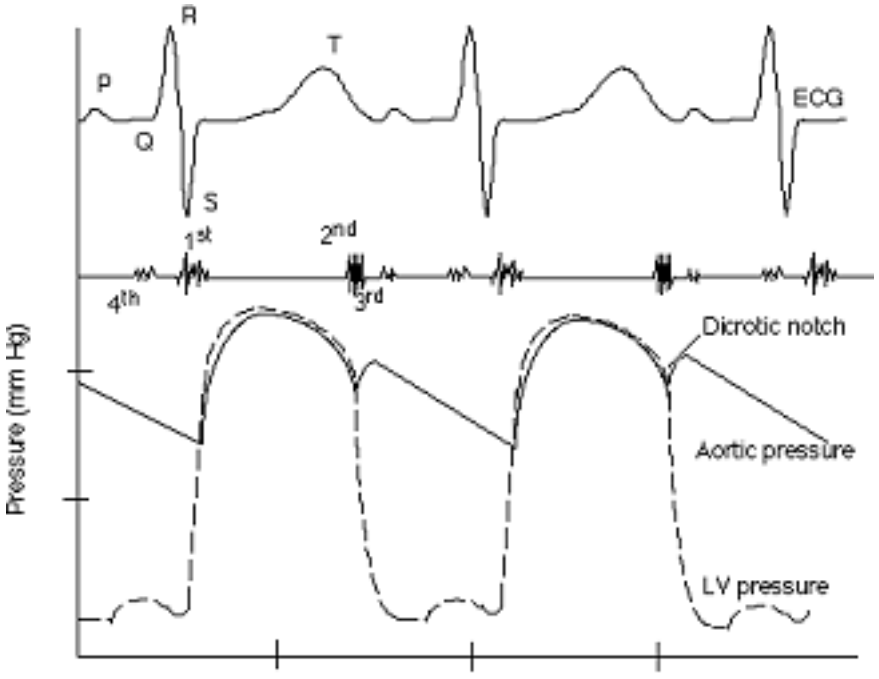
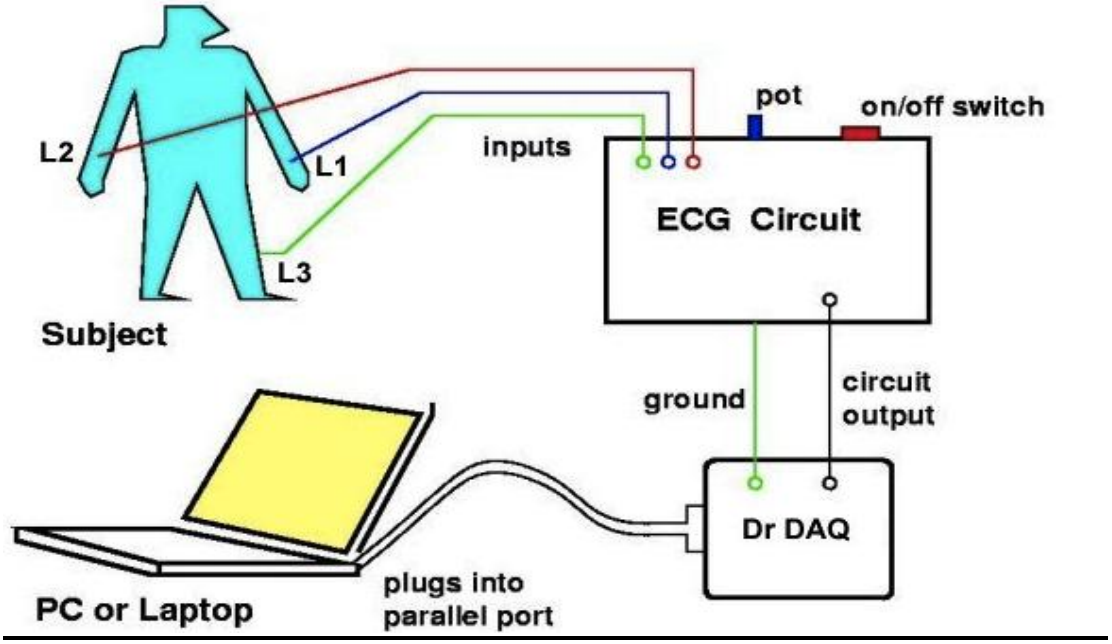


Figure 4 The ECG cardiac cycle.

Basic Block diagram



Detailed Block diagram

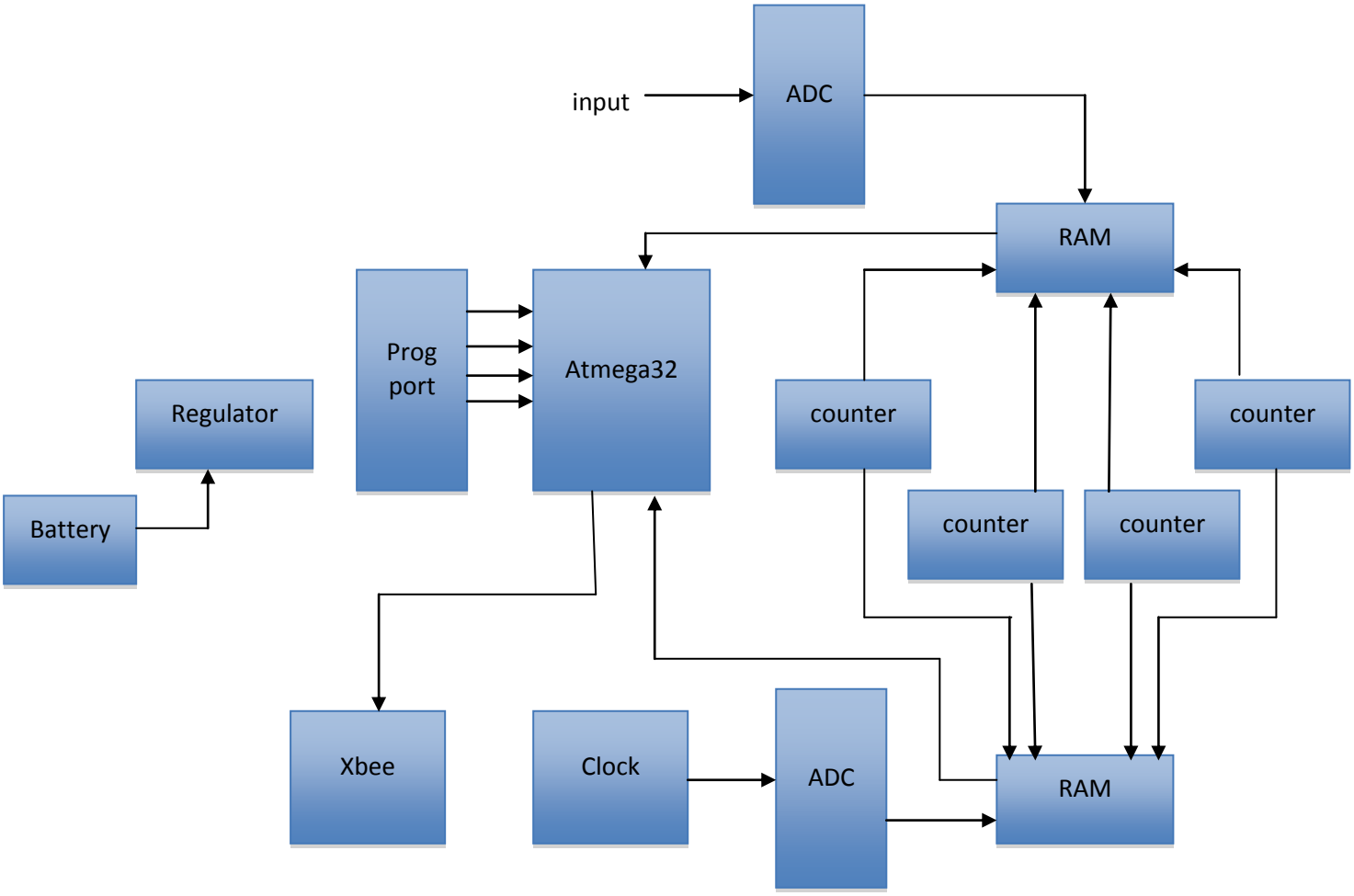


Fig1. *Block diagram*

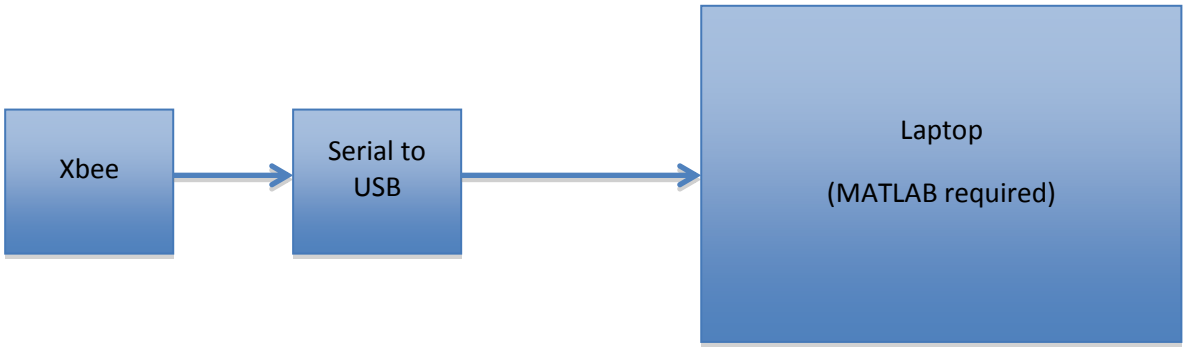
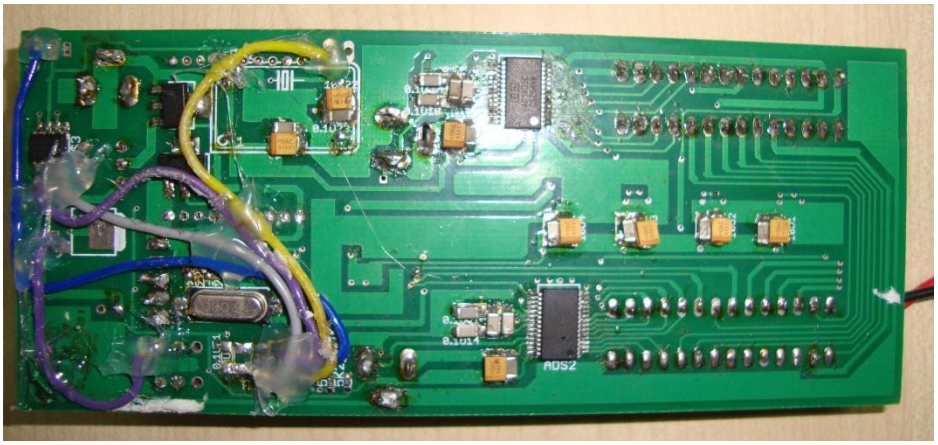
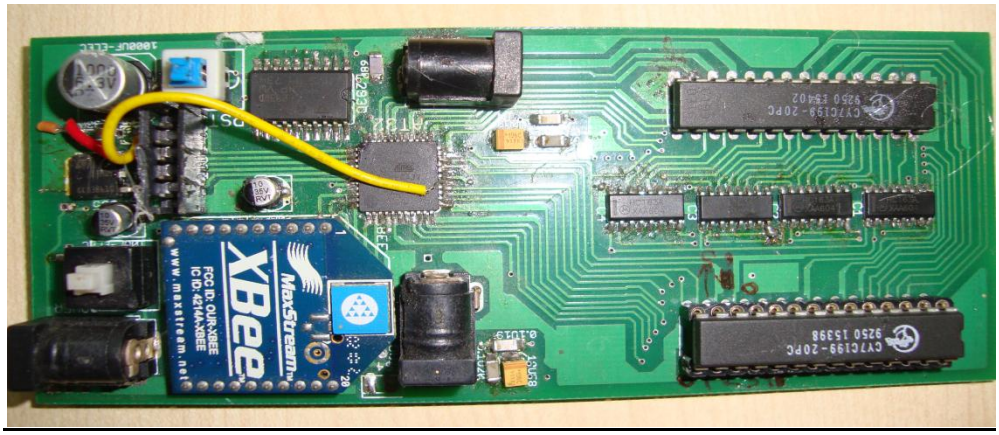


Fig 2. *Block diagram of receiver*

Hardware description





NOTE--

Our first aim was to make the fingerprint attendance reader. But due to late arrival of the fingerprint module we had to modify our project a little. After discussion with all the professors we had two options-

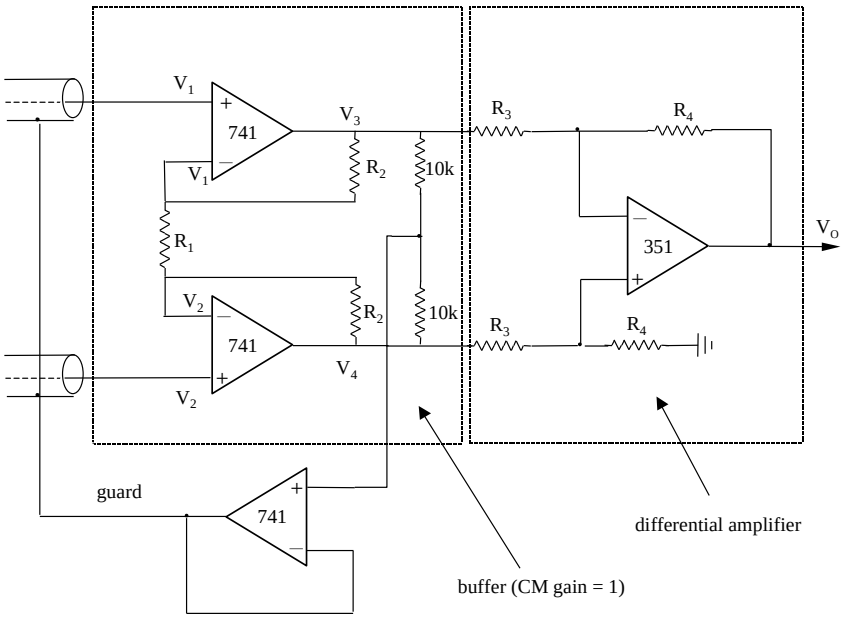
- Device to generate the I-V characteristics of any other device having two terminals.
- Wireless ECG signal.

The above two were chosen as it required little modification to our existing design.

Therefore we decided to make an data acquisition board that can handle any of the above mentioned signals

ECG Amplifier-

The ECG signal amplification was done through the following circuit. It is an instrumentation amplifier made with 3 LM741 Op-amps. It has a CMRR of around 90dB.



ADC-

For the ECG sensor we required an ADC to sample the data and a RAM which can store this sampled data. We intend on providing the same clock to both the RAM and the ADC. For this we want the ADC to sample the data at the positive part of the clock and the RAM to store the data on the negative part. During the time when the ADC is sampling the data, the RAM is disabled and the counters are incremented to store the data in the new address. Keeping this in mind we chose the following components-

Reason for choosing this ADC-

Our first aim was to make the fingerprint attendance reader. But due to late arrival of the fingerprint module we had to modify our project a little. After discussion with all the professors we had two options-

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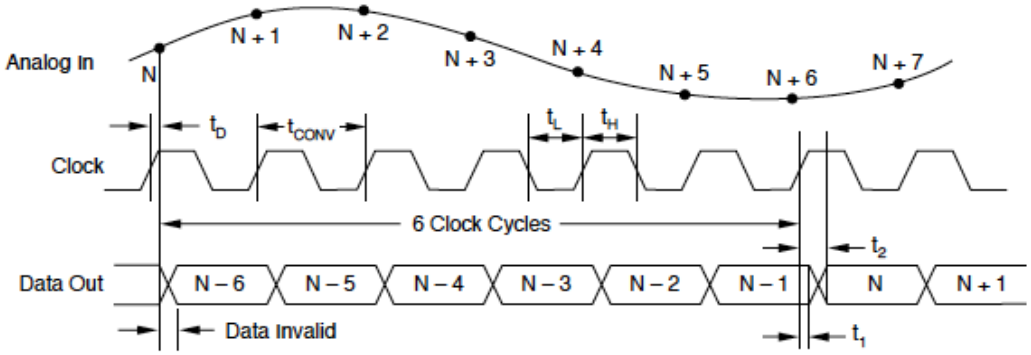
Therefore we decided to make an data acquisition board that can handle any of the above mentioned signals. To take care of analog signals of high frequency we required an ADC of high sampling rate and having an input of 0-5V.

After going through a lot of datasheets we finalized the ADS805 from TI. It has the following key features-

- Max sampling rate 20MHz
- 12 bit
- High SNR: 68dB
- Low Power: 300mW
- Flexible input range

The ADC samples the data at the positive edge of the clock. It takes 6 clock cycles to sample a given analog data. It has a parallel output of 12 bit out of which we are using only 8 bit keeping the rest low.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	50		100µs	ns
t_L	Clock Pulse LOW	24	25		ns
t_H	Clock Pulse HIGH	24	25		ns
t_D	Aperture Delay		3		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12	ns

Fig. *Timing diagram of ADC*

RAM-

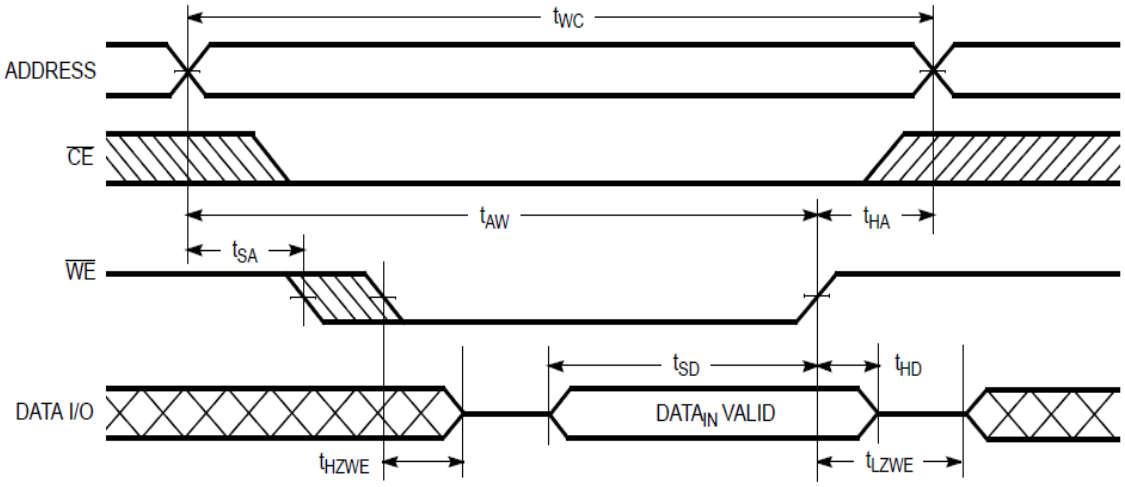


Fig. *Timing diagram of RAM*

Criteria for selecting this RAM-

- It must store data at the negative pulse of the clock.
- The time taken for valid data storage must be less than half the clock cycle.

Keeping this in mind we choose the Cypruss CY7C199 RAM which has the following key features-

- High speed—10 ns
- CMOS for optimum speed/power
- Low active power—467 mW (max, 12 ns “L” version)
- Low standby power—0.275 mW (max, “L” version)
- Easy memory expansion with CE and OE features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

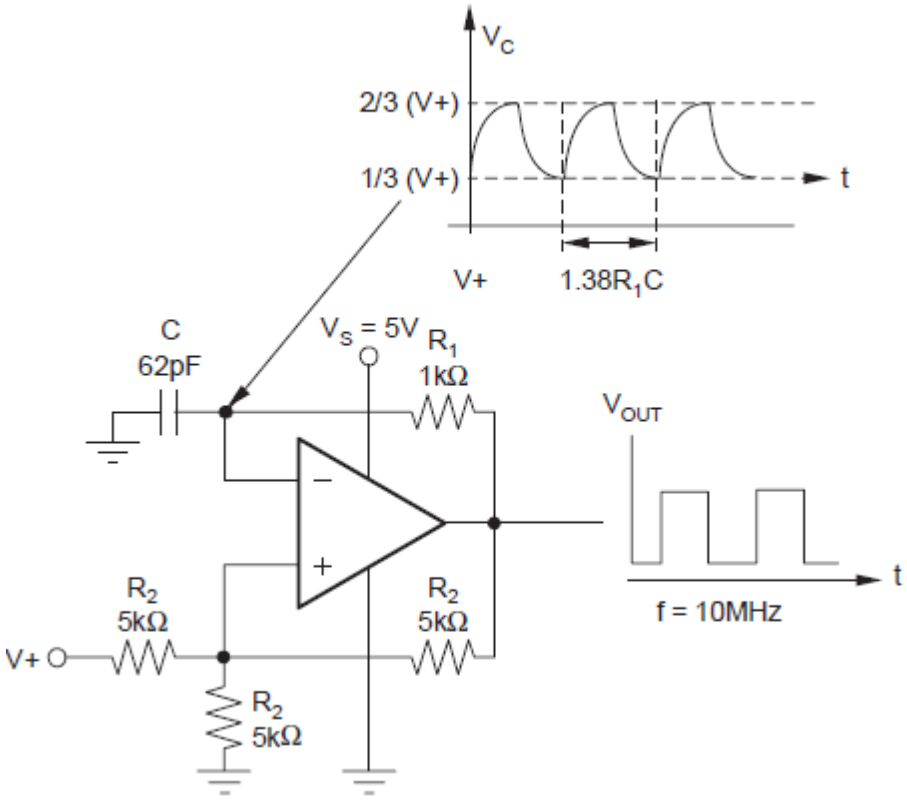
Counter-

The use of the counter is to provide the RAM with an address to store the data. The RAM should have the address before it starts sampling the data. So we must choose a counter such that it increments its value on the positive edge of the clock because the RAM stores the data in the negative pulse.

We have used the **74ACT163** binary counter from Fairchild Semiconductors.

Clock-

To supply a clock signal of 10MHz the following circuit was implemented with a TLV3502 IC. In Figure below, the R2 network sets the trip threshold at 1/3 and 2/3 of the supply. Since this is a high-speed circuit, the resistor values are rather low in order to minimize the effect of parasitic capacitance. The positive input alternates between 1/3 of V+ and 2/3 of V+ depending on whether the output is low or high. The time to charge (or discharge) is 0.69R1C. Therefore, the period is 1.38R1C.



Wireless Transmission-

Fig. *Xbee module*

For wireless transmission of data we have used the Xbee module by MaxStream.

Some of its key features are listed below—

- Indoor/Urban: up to 100’ (30 m)
- Outdoor line-of-sight: up to 300’ (100 m)
- Transmit Power: 1 mW (0 dBm)
- Receiver Sensitivity: -92 dBm
- RF Data Rate: 250,000 bps
- TX Current: 45 mA (@3.3 V)
- RX Current: 50 mA (@3.3 V)
- Power-down Current: < 10 µA

POWER REGULATOR-

Every electronic circuit is designed to operate off of some supply voltage, which is usually assumed to be constant. A voltage regulator provides this constant DC output voltage and contains circuitry that continuously holds the output voltage at the design value regardless of changes in load current or input voltage (this assumes that the load current and input voltage are within the specified operating range for the part).

Mostly there are two types of regulators that are easily available in the market-

1) Linear regulators.
2) Switching regulators.

The one we have used in our project is **LMZ14202H** from National semiconductor which is a 2A simple switcher power module. This part of the report explains in details the working and characteristics of the **LMZ14202H** regulator and also why we choose this particular regulator over the others.

Lets start with the Linear regulators.

Linear regulators-

A linear regulator operates by using a voltage-controlled current source to force a fixed voltage to appear at the regulator output terminal (see Figure 1).

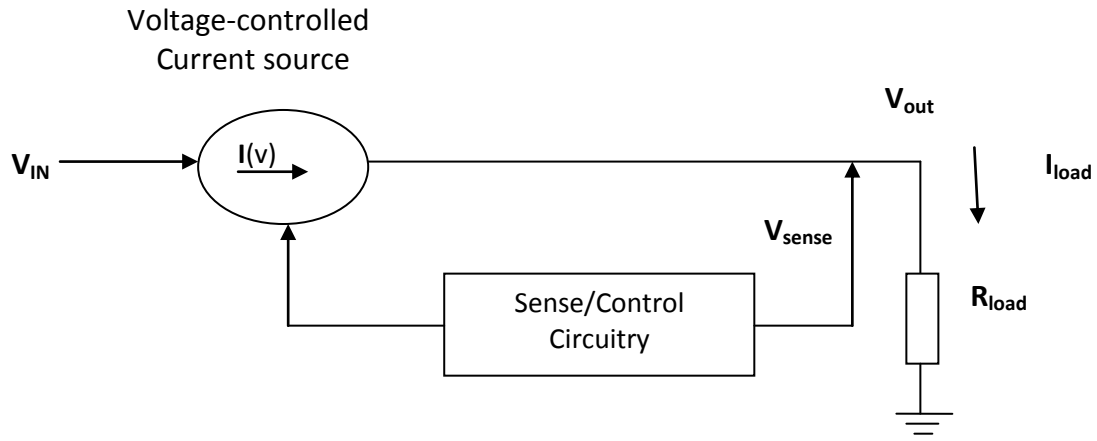


Fig 1. LINEAR REGULATOR FUNCTIONAL DIAGRAM

The control circuitry must monitor (sense) the output voltage, and adjust the current source (as required by the load) to hold the output voltage at the desired value. The design limit of the current source defines the maximum load current the regulator can source and still maintain regulation.

The output voltage is controlled using a feedback loop, which requires some type of compensation to assure loop stability. Most linear regulators have built-in compensation, and are completely stable without external components. Some regulators (like Low-Dropout types), do require some external capacitance connected from the output lead to ground to assure regulator stability.

Another characteristic of any linear regulator is that it requires a finite amount of time to "correct" the output voltage after a change in load current demand. This "time lag" defines the characteristic called transient response, which is a measure of how fast the regulator returns to steady-state conditions after a load change.

There are three basic types of linear regulator designs:

1) Standard (NPN Darlington) Regulator
2) Low Dropout or LDO Regulator
3) Quasi LDO Regulator

The single most important difference between these three types is the dropout voltage, which is defined as the minimum voltage drop required across the regulator to maintain output voltage regulation. A critical point to be considered is that the linear regulator that operates with the smallest voltage across it dissipates the least internal power and has the

highest efficiency. The LDO requires the least voltage across it, while the Standard regulator requires the most.

The second important difference between the regulator types is the ground pin current required by the regulator when driving rated load current. The Standard regulator has the lowest ground pin current, while the LDO generally has the highest (differences between the types is detailed in the following sections). Increased ground pin current is undesirable since it is "wasted" current, in that it must be supplied by the source but does not power the load.

Switching regulators-

The switching regulator is increasing in popularity because it offers the advantages of higher power conversion efficiency and increased design flexibility (multiple output voltages of different polarities can be generated from a single input voltage).

Switching converter types:
Buck: used the reduce a DC voltage to a lower DC voltage.
Boost: provides an output voltage that is higher than the input.
Buck-Boost (invert): an output voltage is generated opposite in polarity to the input.
Flyback: an output voltage that is less than or greater than the input can be generated, as well as multiple outputs.

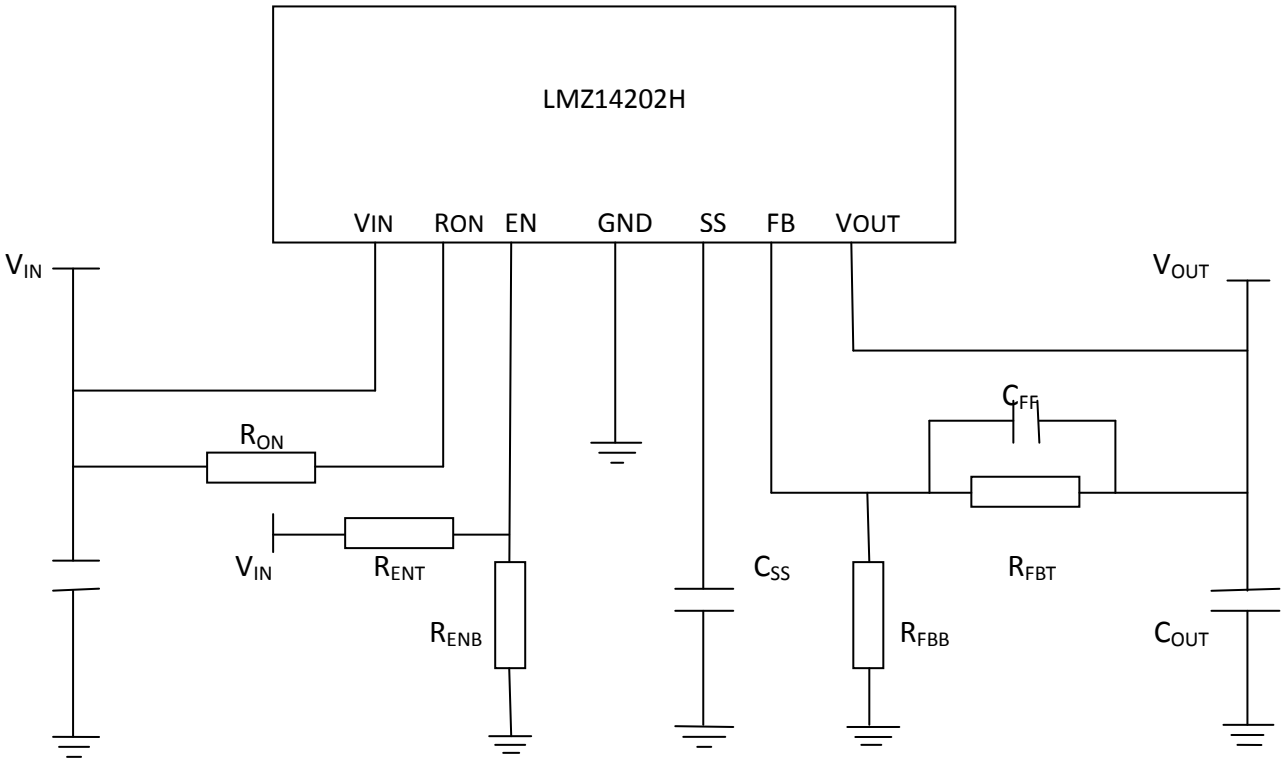
Some multiple-transistor:
Push-Pull: A two-transistor converter that is especially efficient at low input voltages.
Half-Bridge: A two-transistor converter used in many off-line applications.
Full-Bridge: A four-transistor converter (usually used in off-line designs) that can generate the highest output power of all the types listed.

After going through a list of regulators available we finalized on the **LMZ14202H** from National Semiconductor.

Electrical Specifications-

1) Up to 2A output current.
2) Input voltage range 6V to 42V.
3) Output voltage as low as 5V.
4) Efficiency up to 97%.

Simplified Application Schematic-



VOUT	RFBT	RFBB	RON	VIN Range
5V	5.62k	1.07k	100k	7.5...42V
3.3V	3.32k	1.07k	61.9k	6.5...42V
2.5V	2.26k	1.07k	47.5k	6...30V
1.8V	1.87k	1.50k	32.4k	6...25V
1.5V	1.00k	1.13k	28.0k	6...21V
1.2V	4.22k	8.45k	22.6k	6...19V
0.8V	0	39.2k	24.9k	6...18V

Problems faced and troubleshooting

1) **Problem of ground plane**

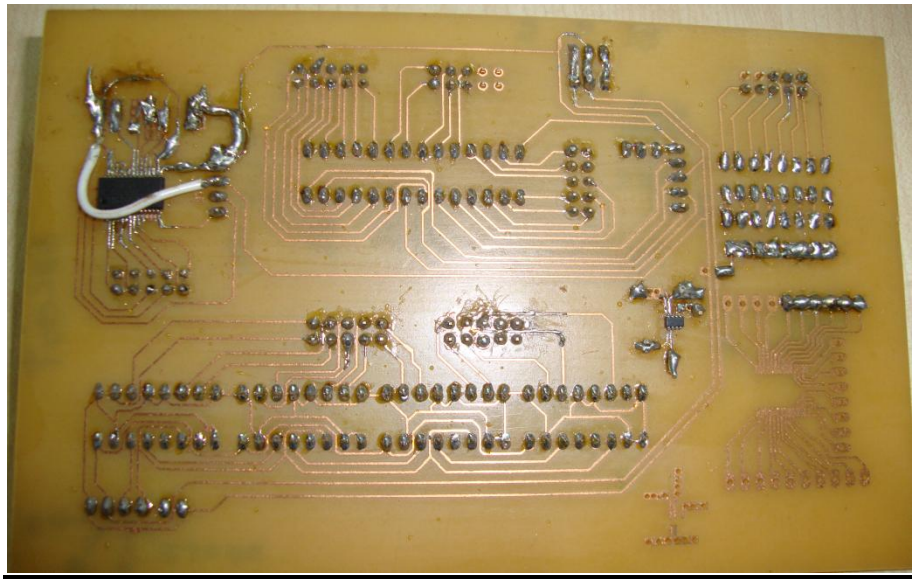


Fig. *Original circuit with thin ground line*

The first circuit we designed had a single thin ground line. The ADC samples the voltage between the reference and the ground. But the ground voltage is not exactly zero, it has some voltage spikes at 10MHz. Therefore the output of the ADC is different from what is desired.

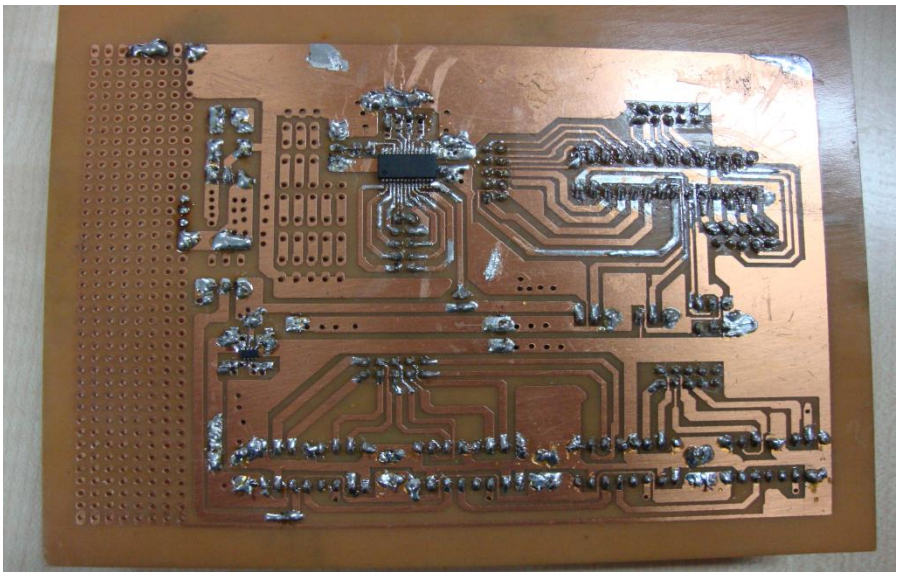


Fig. *Final circuit with large ground plane*

To solve the above mentioned problem we increase the surface area of the ground plane thus reducing the resistance of the track. This led to the reduction of the spikes and thus solved our problem.

2) Clock single to the circuit

To synchronize the data a single clock was used for the whole circuit. This signal with an output of the microcontroller so that when we need to read the data from the RAM the µC

can provide the clock. During this time we need to disable the IC (TLV3502) providing the clock. To do this we made the VCC of the IC low during this time with the help of the µC. This created a problem. The clock output of the µC was only 2V instead of 5V. This was because the TLV3502 was not on a high impedance state and took in a lot of current.

To solve this we replaced the TLV3502 with a new IC TLV3501 which had a chip enable pin. So now instead of making the VCC low we made this chip enable pin low and the problem was solved.

Future work

We intend to include the following in our device in future-

- Variable sampling rate
- Continuous time data transfer at a higher frequency