WRTLT 2015

The 16th IEEE Workshop on RTL and High Level Testing

Indian Institute of Technology Bombay
Mumbai, India, Nov 25 – 26, 2015
https://www.ee.iitb.ac.in/wrtlt15/

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Call for Papers

The purpose of this workshop is to bring researchers and practitioners on LSI testing from all over the world together to exchange ideas and experiences on register transfer level (RTL) and high level testing.
WRTLT'15, the sixteenth workshop, will be held in conjunction with the 24th Asian Test Symposium (ATS) in Mumbai, India. We expect this workshop to provide an ideal forum for interactive discussion on important topics of future system-on-a-chip (SoC), 3D ICs. Areas of interest include but are not limited to:

-RTL fault modeling, ATPG, DFT, BIST
-High-level/behavior fault modeling, testing and synthesis for testability
-Functional fault modeling and test bench generation
-3D IC testing
-SoC/NoC testing, test scheduling, core-based testing, interconnect testing
-Reliable SoC : system level reliability, self repair, fault tolerant SoC
-Microprocessor testing , design verification
-Low power testing
-Test compression, ATPG, DFT, BIST
-Hardware trojan detection, secure testing.

Submission:

Authors are invited to submit paper proposals for presentation at the workshop. The proposal may be an extended summary (1,000 words) or a full paper (4-6 pages, two columns). The submission should include: title, full name and affiliation of all authors, 50 words abstract, keywords and the name of contact author, in a standard IEEE two-column format. The submission will be considered evidence that upon acceptance the author(s) will present the paper at the workshop. Digest of Papers will be handed out

Important Dates
Paper submission: Aug 17, 2015
Notification of acceptance: Sep 15, 2015
Camera ready manuscript: Oct 10, 2015

General Information
MS Gaur, MNIT, India (gaurms@gmail.com)

Program Related Information
Satoshi Ohtake, Oita Univ., Japan (ohtake@oita-u.ac.jp)
Susanta Chakraborty, IIEST, India (susanta_chak@yahoo.co.in)




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