WRTLT 2015 Advance Program

16th IEEE Workshop on RTL and High Level Testing

Indian Institute of Technology Bombay, Mumbai, India

November 25, 2015

16:30 Opening

16:50 Keynote Address

TBA

17:50 Coffee Break

18:10 Session 1 ATPG and Diagnosis

Chair: TBD

1 A Prototype of a Hardware SAT Solver for Similar Large Instances and Its Application to Test Generation

Tsuyoshi Iwagaki, Shoichi Ohmoto, Hideyuki Ichihara and Tomoo Inoue

2 A Sequence Generation Method to detect Hardware Trojan Circuits

Masayoshi Yoshimura, Tomohiro Bouyashiki and Toshinori Hosokawa

3 A Fault Diagnosis Method for a Single Universal Logical Fault Model Using Multi Cycle Capture Test Sets

Hideyuki Takano. Hiroshi Yamazaki. Toshinori Hosokawa and Koii Yamazaki

4 Diagnosis Pattern Generation to Distinguish Inter-Gate and Intra-Gate Faults in CMOS Logic Circuits

Cheng-Hung Wu. Kuen-Jong Lee and Sheng-Tze Wang

19:50 Break

20:00 Dinner

November 26, 2015

9:00 Invited Talk

TBA

9:40 Session 2 3D IC Testing

Chair: TBD

1 Power Aware 3-D IC Testing using Genetic Algorithm

Tanusree Kaibartta and Debesh Das

2 Test Circuit for Electrical Interconnect Tests of 3D ICs without Boundary Scan Flip Flops

Masaki Hashizume, Shoichi Umezu, Yuki Ikiri, Hiroyuki Yotsuyanagi and Shyue-Kung Lu

10:30 Coffee Break

10:45 Session 3 Verification

Chair: TBD

1 Mapping analysis between RTL/high-level and gate-level designs with inductive invariants on partial behaviors

Masahiro Fujita, Qinhao Wang and Yusuke Kimura

2 Model Checking based verification of Hardware Trustworthiness

Yingxin Qiu and Huawei Li

3 A Framework for Verification of Hard Tied Signals of SoC

Prokash Ghosh, Sandip Ghosh and Raghavendra Srinivas

12:00 Lunch Steering Committee Meeting

14:00 Session 4 FPGA Test and BIST Techniques

Chair: TBD

1 Analysis of SRAM-Based FPGA SEU Sensitivity to EMI and TID: the need for combined tests

Juliano Benfica, Bruno Green, Letícia Bolzani Poehls, Fabian Vargas, Nilberto Medina, Nemitala Added, Vitor de Aguiar, Eduardo Macchione, Marcilei Da Silva, Martín Perez, Miguel Sofo Haro, Ivan Sidelnik, Jerónimo Blostein, Jose Lipovetzky and Eduardo Bezerra

2 A Field-Test Architecture for Circuits Configured on FPGAs

Sho Kano and Satoshi Ohtake

3 A Circular BIST Architecture Using Internal Responses of Circuits for Reseeding and Extra Observation

Chung-Min Shiao, Wei-Cheng Lien and Kuen-Jong Lee

15:15 Coffee Break

15:35 Session 5 Circuit Design

Chair: TBD

1 Improved Synthesis of Reversible Circuits

Bikromadittya Mondal, Pradyut Sarkar and Susanta Chakraborty

2 Note on Dependable Logic Design by Ambipolar Device and Its Fault Modeling

Dan Takahashi and Masayuki Arai

3 BDD based PDF Testable Combinational Circuit Design

Toral Shah, Virendra Singh and Anzhela Matrosova

16:50 Closing