Department of Electrical Engineering

M.Tech. Admissions 2025-26

Abstracts of Projects
(only for PRA category)

Note:

1) This booklet contains abstracts of project for which RA positions are open.

2) These positions are other than Institute RA positions.

3) Institute RA work in various teaching labs of the department while Project RA are assigned duties on specific project.

4) Institute RA is free to choose any topic in his/her specialization for M.Tech. Thesis but Project RA may have to work for their thesis in the area of project only.

5) If you are selected for Project RA position, you will be assigned a project from your preferences and based on your performance in written test/interview. **Once selected for any project, it will not be permitted to change from one project to another.** Candidates will be asked about their preferences at the time of interview.

Project Investigator: Prof. Shiladri Chakraborty

Title of the project: **Design and development of matrix-type, single-stage fast charger for light electric vehicles**

Desired specialization: EE 3 (Power Electronics & Power Systems)

Abstract of the project:

Vehicle electrification in India will primarily revolve around light electric vehicles (LEVs), including two-wheelers (scooters, motorcycles) and three-wheelers (auto-rickshaws, mini-trucks). Despite various governmental initiatives like FAME aimed at promoting EV adoption, a significant technical hurdle hindering wider acceptance is their prolonged charging times. To address this technology and research gap, this work proposes developing an ultra-fast LEV charger, which can charge from 0 to 80% battery capacity in less than 15 mins. Technically, this means the development of 10 kW and 25 kW charger circuits for 2Ws and 3Ws, respectively.

While a standard approach towards building a high-power circuit would be to parallel several smaller power modules, the improvement of the proposed work would be to minimize the number of modules necessary by suitably designing each module at much higher power. This would mitigate control complexity among the parallel modules and also offer cost and size benefits due to reduced BOM count. The main technical innovation enabling these advantages is to employ a novel low-switch-count, single-stage, three-phase-AC topology.

Project Investigator: Prof. Shiladri Chakraborty

Title of the project: **Multi-functional wireless charger for LEVs with minimal on-board power electronics**

Desired specialization: EE 3 (Power Electronics & Power Systems)

Abstract of the project:

The near-absence of wireless charging solutions for 48 V LEVs highlights a significant research gap, which this project aims to address. The primary topic in focus is the formulation, design, and development of a 2.2 kW wireless charging prototype for a 48 V LEV system. Several key technical challenges must be addressed in this context : efficient and feasible coil misalignment-tolerant operation, high stresses across the compensation networks, appropriate voltage matching between the LEV battery voltage (48 V) and the power factor correction DC-bus voltage (400 V), minimal weight and size of on-board power electronics, bidirectional capability to enable vehicle-to-grid operation and incentivise customer adoption, magnetic field emission shielding, foreign object detection, and other related areas. The value proposition of the work is to promote the adoption and deployment of wireless charging as a cutting edge and convenient technology in the EV sector.

Project Investigator: Prof. Sandeep Anand

Title of the project: **Power Electronics for Electric Vehicles**

Desired specialization: EE 3 (Power Electronics & Power Systems)

Abstract of the project:

EVs is the stepping stone towards truly sustainable transportation solutions. The electric drivetrain consists of electric motor, its controller and onboard charger. Range anxiety and performance are some of the concerns among EV users. Hence, for a high performance and long range EV, a light weight, compact and energy efficient drivetrain is essential. Some of the topics covered under this call are:

- Motor controllers for electric vehicles
- Online health monitoring of power electronics used in Electric vehicles
- Power electronics for medium voltage dc fast chargers
- Integrated topologies for electric vehicle power electronics
- SiC based inverter for EV applications

If you find any one or more of the following topics interesting, then you must apply for this project:

- Onboard EV charger circuits
- DC-DC converters
- EV fast chargers
- Motor Drives / Inverters
- GaN & SiC based circuits.

Project Investigator: Profs. Sandeep Anand, Shiladri Chakraborty, Kishore Chatterjee, B.G. Fernandes, Anil Kulkarni

Title of the project: **NCPRE: Silicon Carbide (SiC) based medium voltage solar inverter**

Desired specialization: EE 3 (Power Electronics & Power Systems)

Abstract of the project:

Power electronics converters play a very important role in renewable generation. The ever-increasing demand for better efficiency, reliability, and compactness has made the requirement of innovation in the area of power electronics very important. The wide band gap (WBG) devices are a new disruptive technology which would drastically change the power electronic industry. Silicon Carbide (SiC) based power devices are now commercially available and offer better performance in terms of on-state resistance and gate capacitance. These advantages help in achieving high efficiency and power density in power converters. However, there are interesting research problems in designing and developing power electronic converters using these SiC devices. This project aims to carry out research in the area of advanced power electronic converters. There are 3 open positions in this project.

If you find any one or more of the following topics interesting, then you must apply for this project:

- Design and development of Gate driver for SiC-based devices
- Topology selection and circuit design for medium voltage solar inverter
- Magnetics design for medium-voltage medium-frequency transformers development
- Controller for medium voltage solar inverter, along with grid integration
- Condition monitoring techniques in solar inverter
- Accelerated aging and failure models of SiC devices
- Futuristic technologies for improving reliability (Active Power Decoupling and Active Thermal Control)

Project Investigator: Prof. Bhaskaran M

Title of the project: **Design of Type-II superlattice photodetectors via TCAD simulations**

Desired specialization: EE 7 (Solid State Devices)

Abstract of the project:

The project will explore the design space and optimisation of type-II superlattice photodetectors for outer space applications. The project will collaborate with ISRO/SSPL to make concrete TCAD + device simulation based design inputs to ISRO in order to fabricate.

Project Investigator: Prof. Ashwin A. Seshia

Title of the project: **Microelectromechanical platforms for 2D materials**

Desired specialization: EE 5 (Electronic Systems), EE 7 (Solid State Devices)

Abstract of the project:

This project will investigate the integration of 2D materials on microelectromechanical platforms. There has been significant interest in emerging 2D materials (such as MoS2) due to their electronic, optical, and mechanical properties. The project will involve aspects related to the fabrication of devices, modelling of the device physics, and experimental characterization of fabricated devices to evaluate static and dynamic electromechanical response. Dynamic strain engineering in these materials will be studied and the interaction with transport properties including in configurations such as vibrating beam transistors. Integration of these materials onto Si/SiN micromechanical membranes for sensor applications will be explored.

Project Investigator: Prof. Ashwin A. Seshia

Title of the project: **MEMS-based gas sensors**

Desired specialization: EE 5 (Electronic Systems), EE 7 (Solid State Devices)

Abstract of the project:

Miniaturized low-power gas sensors based on MEMS technology have several applications including air quality monitoring, biomedical diagnostics, and industrial process control. This project will

develop a nanofabrication process for MEMS-based gas sensors based on electrochemical principles in the IITB nanofabrication facility.

Project Investigator: Prof. Madhav P. Desai

Title of the project: **High performance edge accelerator design and validation**

Desired specialization: EE 1 (Communication & Signal Processing), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

A high performance edge compute platform is under implementation. The project involves digital system design and verification, System software development and validation, FPGA prototyping and application porting.

Project Investigator: Prof. Anshuman Shukla

Title of the project: **Multifunctional Battery Charger with Wide Operating Range for EV Applications**

Desired specialization: EE 3 (Power Electronics & Power Systems), EE 5 (Electronic Systems)

Abstract of the project:

The primary objective of this project is to develop a novel charger technology capable of charging multiple electric vehicles (EVs) with a wide range of voltage and power requirements. Its modular design allows for customization and scalability to meet diverse customer needs and installation requirements. The project will progress through several Technology Readiness Levels (TRLs).

Project Investigator: Prof. Maryam Shojaei Baghini

Title of the project: **Analog/Mixed-Signal IC and System Design for Magnetic Sensing**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

The aim of this project is to design, develop, test and prototype two target prototypes:
1- System Design: Electronic system for magnetic sensing using commercially available Hall sensor integrated circuits (IC's)

2- IC Design: A novel signal conditioning integrated circuit (IC) for the magnetic sensing technology based on the Hall effect for a set of target applications.

Project Investigator: Prof. Maryam Shojaei Baghini

Title of the project: **Electronic System and CMOS IC Design for Soil Sensing**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

This project is sponsored by industry. The objective of this project is to design a soil sensing electronic system and a CMOS IC for agriculture applications.

Project Investigator: Prof. Maryam Shojaei Baghini

Title of the project: **CMOS IC Design and Electronic System for RF Energy Harvesting (Antenna to the Load)**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

In this project an RF/Mixed-Signal CMOS IC for a complete very low-energy EM-wave energy harvester will be designed, fabricated and demonstrated. Design optimization methods and EDA (electronic design automation) tools will be used throughout the project.

Project Investigator: Prof. Maryam Shojaei Baghini

Title of the project: **Water quality monitoring system for physicochemical parameters and pollutants**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

This project is continuation of a completed project on a prototype system designed and developed by several M. Tech RA students as well as Ph.D. and research fellows as a collaborative project between Electrical Engineering and Chemical Engineering Department of IIT Bombay. The project is supported by IITB Research Hub for Green Energy and Sustainability (GESH). The M. Tech student will have opportunity to learn and contribute to the electronic system as her/his M. Tech project RA fellowship and design of analog CMOS integrated circuit (IC) for sensing applications as her/his M. Tech project.

Project Investigator: Prof. Prasanna Chaporkar

Title of the project: **Core Network for 6G and Beyond**

Desired specialization: EE 1 (Communication & Signal Processing)

Abstract of the project:

With the release of “Bharat 6G vision” by our hon’ble prime minister and finalization of 6G (IMT-2030 and beyond) requirements by ITU-R, it is an opportune time for the researchers in the country to engage in R&D activities in the Sixth Generation (6G) technology, the future of mobile communications.

To this end, we, a team of researchers from IIT Bombay (IITB), propose to undertake research activities towards the designing a modular, scalable, and flexible core network for the 6G system. The project would likely facilitate early IPR and technology development for 6G system in the country and may also allow us to make significant contributions to the global 6G standards.

Project Investigator: Prof. Prasanna Chaporkar

Title of the project: **Sustainable 6G: AI/ML techniques for Energy-aware and Intelligent Wireless Networks**

Desired specialization: EE 1 (Communication & Signal Processing)

Abstract of the project:

We propose to build an energy-aware 6G system using AI/ML to automate network design and control. The solution aims to reduce energy consumption and enhance network efficiency by integrating AI/ML based network management for both RAN and Core network functions.

Project Investigator: Prof. Prasanna Chaporkar

Title of the project: **NSF-Meity: NeTS: Small: Towards Learning Enabled Sustainable Service Handling in 6G**

Desired specialization: EE 1 (Communication & Signal Processing)

Abstract of the project:

Speedy digitization and rising demand for communications services are resulting in continued increases in energy consumption in cellular networks. GSMA, in its 2019 report, estimates that cellular networks contribute to a total annual emissions of approximately 220 MtCO2e (0.4%) in global emissions, which may double by 2025.

Energy-aware network design to reduce energy consumption in mobile networks and improve energy efficiency will significantly benefit humanity. The research themes: Energy-aware ML-driven core network, Energy-aware ML-driven radio access network and Service-aware adaptive security mechanism are detailed in the proposal. It signifies immediate research focus directed toward realizing the ambitious goal of developing a resource-efficient and sustainable 6G system.

Project Investigator: Prof. Laxmeesha Somappa and Rahul Singh

Title of the project: **Collision Avoiding RFID IC design for Inventory Management**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

Radio-frequency identification (RFID) presents a promising technological solution for diverse applications such as automated checkout systems, warehouse inventory control, and supply chain logistics. Nevertheless, its practical application remains constrained by the inability of current state-of-the-art RFID systems to adequately meet requirements concerning manufacturing cost, operational range, and dependable performance, including effective collision avoidance protocols. Our objective is to engineer a reliable and secure RFID integrated circuit specifically designed to mitigate these challenges within an inventory management context, necessitating expertise in analog, RF, and digital IC design, as well as subsequent system-level development.

Project Investigator: Prof. Laxmeesha Somappa and Rahul Singh

Title of the project: **VLSI SoC design Exploration and IP Management**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

A VLSI SoC design includes design of multiple IPs spanning across Analog, Mixed-signal, Digital and RF IC design principles. Effective IP reuse is essential in realizing such SoCs. This project involves designing of such IPs, developing automated verification and test flows for faster design-test cycles.

Project Investigator: Prof. Laxmeesha Somappa

Title of the project: **IC and System design for Brain Computer Interface**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

The objective of this project is to develop a biomedical Integrated Circuits (ICs) and Systems that can record brain signals, identify seizures and immediately arrest seizures for target epilepsy patients in India. This will be an indigenous biomedical system that will be developed with state of the art performance. Students will be involved in the development of the following indigenous semiconductor IPs (intellectual property) and systems: high-density neural recording (b) highly programmable neural stimulators (c) power management circuits for neural systems (d) Implantable system development using the designed ICs.

Project Investigator: Prof. Rajesh Zele

Title of the project: **RF CMOS Transceiver Circuit design**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

After training in our aiCAS lab, the students will work on RF transceiver design for phased array/ MIMO systems to build efficient wireless communication chips. The student will work with senior PhD mentors for hands-on training, eventually leading to a tapeout of their ideas in nanometer CMOS technologies. The students will spend time in the industry for internships and work closely with Industry mentors.

Project Investigator: Prof. Rajesh Zele

Title of the project: **Mixed-signal (ADC/DAC) CMOS IC design for ultra-low-power Biomedical applications**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

The students will focus on data communication IC design for biomedical implants. After training, the students will build upon the previous chips designed in the aiCAS lab. They will design ultra-low power ADC/DAC for power-efficient biomedical links. The students will spend time in the industry for internships and work closely with Industry mentors.

Project Investigator: Prof. Rajesh Zele

Title of the project: **High-speed serial link design for chiplet communications in AI/ML applications**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

The student will be exposed to CMOS analog/mixed-signal IC design flow using cutting-edge nanometer semiconductor technology. The students will participate in the design of high-speed serial data links for chip-to-chip (chipset) communication—for example, interchip communication between NVidia GPUs. The students will spend time in the industry for internships and work closely with Industry mentors.

Project Investigator: Prof. Rajesh Zele

Title of the project: **CMOS high-performance Digital IC design for RF communications SOC (System-On-Chip)**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

The student will get end-to-end exposure to CMOS digital IC design flow using cutting-edge nanometer semiconductor technology. You will start from architecture, Matlab simulations, RTL to gds flow, FPGA implementation,— all the way to Place and route, sign-off verifications and then tapeout. The student will closely work with RF/Analog/Mixed-Signal IC design team for system spec. The students will spend time in the industry for internships and work closely with Industry mentors.

Project Investigator: Prof. Preeti Rao

Title of the project: **Speech & NLP Tools for Automatic Spoken Language Assessment**

Desired specialization: EE 1 (Communication & Signal Processing), EE 5 (Electronic Systems)

Abstract of the project:

Deep learning models are helping automatic speech recognition and text processing achieve performances close to human expert based judgements provided small amounts of high quality labeled data coupled with self-supervised training. We are building tools for text difficulty evaluation, speech fluency assessment, and text and audio synthesis for reading comprehension practice with generative AI.

Project Investigator: Prof. Rahul Singh

Title of the project: **High-speed integrated circuits for wireless optical linkns**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

"High-speed Integrated Circuits for 6G (wireless) optical links
• GoI's initiative on accelerated 6G research
• High-speed/wide bandwidth TIAs and modulation drivers
• Tapeouts in SiGe/CMOS process nodes
• Interfacing with Photonic systems
• Skills: Strong interest in RF/Analog/Digital IC Design".

Project Investigator: Prof. Rahul Singh

Title of the project: **High-frequency/mm-wave Integrated Circuit Design**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

High-frequency/mmWave Integrated Circuit Design
• Agile RF receiver/transmitter front-ends)
• mmWave beamforming phased-arrays
• Calibration Circuits
• Skills: Strong interest in RF/Analog/Digital IC Design

Project Investigator: Prof. Rahul Singh

Title of the project: **Integrated Circuits for Interfacing with Quantum Systems**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

Integrated Circuits for Interfacing with Quantum Systems
• Part of National Quantum Mission
• RF/Analog/digital IC design of read-out/control circuits from system-level specifications to highly-integrated chip prototypes.
• Measurement and testing, access to complex RF instrumentation).
• Multiple tapeouts in CMOS/SiGe process nodes.

Project Investigator: Profs. Veeresh Deshpande and Shalabh Gupta

Title of the project: **High-Speed Interconnect PHY layer design for chiplet communication**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

For advanced CMOS nodes (7 nm and below), there is need to separate logic from other functional blocks into physically different chips (known as chiplets) for performance-cost tradeoff. Between these chiplets, the communication needs to be high-speed, similar to inter-block communication within the SoC. In this project, the aim is to develop the circuit design and perform the tapeout for inter-chiplet high-speed communication physical design. The protocols like UCIe or BoW will be considered. This project is in collaboration with Prof. Shalabh Gupta (EE, IITB). One of the applications of this design will be development of chiplet based SoC and integration in the upcoming advanced chiplet packaging laboratory at IITB.

Project Investigator: Prof. Shalabh Gupta

Title of the project: **High-speed analog(/digital) integrated circuits for wireline/optical communication links**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

In this work, you would be designing and testing high-speed electronic integrated circuit for optical links & wireline interconnects. Circuits such as phase-locked loops, clock and data recovery circuits / SerDes, drivers, trans-impedance amplifiers etc. will be designed and integrated at a system level. You would be collaborating with other team members.

Good knowledge in the area of analog circuits, analog/digital communication systems, and interest in working with high-speed experimental setup will developed. Strong fundamentals and some hardware skills are important, others skills can be picked up after joining the group.

Sample publication:
S. Chugh, R. Ashok, P. Jain, S. Naaz, A. Sidhique and S. Gupta, "An Analog EIC-PIC Receiver with Carrier Phase Recovery for Self-Homodyne Coherent DCIs," IEEE Transactions on Circuits and Systems II: Express Briefs (2022). https://doi.org/10.1109/TCSII.2022.3167673

Project Investigator: Prof. Shalabh Gupta

Title of the project: **High-speed photonic integrated circuits for optical communication links**

Desired specialization: EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

In this work, you would be designing and testing photonic integrated circuits for high-speed optical communication links. Building blocks such as electro-optic modulators, drivers, photodetectors, optical filters etc will be designed integrated at a system level. You would be collaborating with other team members.

Requirements: Good fundamentals and some hardware skills are important, others skills can be picked up after joining the group.

Sample publication:
S. Chugh, R. Ashok, P. Jain, S. Naaz, A. Sidhique and S. Gupta, "An Analog EIC-PIC Receiver with Carrier Phase Recovery for Self-Homodyne Coherent DCIs," IEEE Transactions on Circuits and Systems II: Express Briefs (2022). https://doi.org/10.1109/TCSII.2022.3167673

Project Investigator: Prof. Shalabh Gupta

Title of the project: **Communication signal processing and electronics for high-speed wireline/optical communication links**

Desired specialization: EE 1 (Communication & Signal Processing), EE 5 (Electronic Systems)

Abstract of the project:

In this work, you would be developing communications/signal processing algorithms and techniques, and developing hardware for high-speed optical/wireless links. The work would also involve playing with advanced digital modulation schemes and carrying out experiments with state-of-the-art equipment with other team members.

Good knowledge in the area of analog/digital communication systems, and interest in working with high-speed experimental setup will developed. Good fundamentals and some hardware skills are important, others skills can be picked up after joining the group.

Sample publication:
R. Kamran, S. Naaz, S. Goyal, and S. Gupta, "High-Capacity Coherent DCIs using Pol-Muxed Carrier and LO-Less Receiver," IEEE/OSA Journal of Lightwave Technology, 38(13), 3461 - 3468 (2020). https://doi.org/10.1109/JLT.2020.2972913.

Project Investigator: Prof. Debasattam Pal and Kumar Appaiah

Title of the project: **Matrix precoders for MIMO wireless links: A time-domain approach**

Desired specialization: EE 1 (Communication & Signal Processing), EE 2 (Control & Computing)

Abstract of the project:

The use of multiple-input multiple-output (MIMO) techniques has become the norm in modern wireless communication systems, since they provide increased data rates and enhanced reliability. One essential ingredient in realizing these benefits is by the use of matrix precoders that are typically unitary matrices that can be used to beamform the transmissions for optimal reception. With the advent of 5G and beyond systems, the very wide band nature of the communication channel necessitates that the precoder be fed back for a wide range of frequencies from the receiver to the transmitter, thereby increasing the feedback overhead in such systems, despite their being more significant line of sight components that result in more sparse time-domain representations. To address this issue, we propose to use time-domain matrix precoders, since they capture the unitary structure of the precoding matrices while providing realizable time domain filters. Recent work has shown that precoders can be viewed as matrix all-pass filters, with the coefficients being easier to feedback owing to the sparse time-domain channel realization. In this project we aim to construct such time-domain all-pass filters as matrix precoders from a limited data set given by the desired filter's matrix-valued phases at a finite set of frequencies. Our approach towards solving this is through interpolation of the data by a matrix of rational function entries. This is a well-known open problem from complex analysis: the boundary case of subspace Nevanlinna-Pick interpolation problem (B-SNIP). In our recent work we have shown how the open problem of B-SNIP can be solved by compensating the data-set with derivative-like additional data. However, this solution raises a number of crucial questions that needs answering for a comprehensive solution of the matrix precoder design via B-SNIP. The proposed project is aimed at resolving these issues. We briefly state these issues here: 1. B-SNIP admits non-unique solutions. Our existing method chooses a solution in an ad hoc manner. A full characterization of all solutions of B-SNIP is needed to choose the most desirable precoder that is also stable in the time domain. 2. We have already shown that a key parameter in the solution is the Schwarz-Pick matrix, which in turn is parametrized by the above-mentioned derivative-like parameters that are additionally supplied as input. These additional parameters allow us to vary the solution, and thereby obtain a precoder that outperforms others. This optimization problem needs to fully understood and formalized. 3. Since the precoder design is based on the frequency domain data, it is of utmost importance that the method be immune to unwanted perturbation in the data. The extent of robustness of our solution to B-SNIP needs to be investigated

and quantified; necessary mitigation technique to this effect needs to be devised. 4. The devised techniques' performance needs to be verified experimentally.

Project Investigator: Prof. Virendra Singh

Title of the project: **Security of Futuristic Technologies (AI/ML/AR/VR/CPCS/Hardware Design/Quantum Computing)**

Desired specialization: EE 1 (Communication & Signal Processing), EE 2 (Control & Computing), EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

Artificial Intelligence (AI) is creating a huge impact on the world by integrating its service into all possible facets of our daily life needs. Many sectors like finance, healthcare, automobiles, marketing, social media, chat-bots, etc., are using AI models like Neural Networks(NN), Large Language Models(LLMs), Reinforcement Learning(RL), etc., for their decision-making process. As it is known that with pros come cons, even a single vague decision of the model will lead everything to stake. An example of this can be a self-driving car identifying a stop sign as a speed sign which leads to destruction. There are many more such scenarios where the decisions of the AI models are making the world miserable. So, finding the vulnerabilities, providing security to the model, and making the model robust in any scenario is very crucial. In this growing machine-dependent world securing those machines is on high priority else it may lead to massive human destruction.

This project examines instances where adversarial attacks on AI systems have been employed to manipulate decision-making processes, compromise data integrity, and erode public trust. By understanding these vulnerabilities, we can draw connections to their broader implications for addressing pressing global challenges such as cyber-security, misinformation, and ethical considerations in AI deployment and thus explore potential countermeasures and defensive strategies to fortify AI systems against adversarial threats. This includes advancements in robust model architectures, enhanced training methodologies, and the development of explainable AI to increase transparency and accountability.

On the other hand, CPS (Cyber Physical Systems), which is composed as system of systems, has to be intelligent and trustworthy. The main aim of this research is to develop effective and efficient design methodologies for trustworthy cyber physical cognitive systems. It can be seen as a system of systems with dependable cyber physical system and trustable AI as a core components. The examples of such systems can range from Autonomous vehicles, Smart grids, Smart cities, Smart agriculture, Drone based Surveillance to sophisticated Pacemakers. Hence, the project will aims at developing design methodologies for intelligent trustworthy Cyber Physical Cognitive Systems (T-CPCS) to enable Smart-X in societies.

Project Investigator: Prof. V. Rajbabu

Title of the project: **Machine learning for dron image analysis**

Desired specialization: EE 1 (Communication & Signal Processing), EE 5 (Electronic Systems)

Abstract of the project:

The main goal of this project is to estimate various crop indices/parameters from multi-spectral band agricultural drone images. Later we will be estimating yield from a specified area. The tools involved will be from image processing and machine learning. This is a sub-project under a larger drone project and hence the scope will become broader depending on data availability from drones.

Project Investigator: Prof. Kumar Appaiah

Title of the project: **Novel FPGA-assisted coherent detection systems for energy-efficient and high-capacity optical communication**

Desired specialization: EE 1 (Communication & Signal Processing), EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

Energy-efficient and High-capacity optical communication systems are encumbered by pulse spreading caused by dispersion as well as receiver phase issues and IQ imbalance. This project aims to implement an FPGA-based solution that would track the errors in the receiver subsystem and adaptively correct these to reduce energy consumption and scale data rates and in optical communication systems.

Project Investigator: Profs. Kumar Appaiah and Sibi Raj B Pillai

Title of the project: **EM Propagation Models for Wireless**

Desired specialization: EE 1 (Communication & Signal Processing), EE 5 (Electronic Systems)

Abstract of the project:

Develop propagation models for enhanced wireless communication in long range scenarios.

Project Investigator: Prof. Anirban Sarkar

Title of the project: **RF Beam Scanning antenna and circuits based Joint Communication and EM Sensing**

Desired specialization: EE 1 (Communication & Signal Processing), EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

Considering the emerging demand of B5G/6G in wireless communications and sensing, the beam scanning antennas and advanced RF circuits play a pivotal role. To fulfill this, the antennas and smart surfaces need to be designed along with RF sensors with advanced sensing signatures. Targeting the

essential parts of the healthcare and defence industry, the projected research area surely serve for combating different diseases using advanced wireless smart sensing as well as for the current defence industries. Overall, the total system will be under the joint communication and sensing.

Project Investigator: Profs. Debanjan Bhowmik, Bhaskaran M.

Title of the project: **High speed multiple-input multiple-output (MIMO) symbol detection in large MIMO systems for wireless communication using electronic and spintronic oscillator Ising machines (OIM) (and associated teaching and research with Synopsys's tools)**

Desired specialization: EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

In this project, we would like to design, simulate (at schematic and post-layout level using Synopsys's HSPICE tool), fabricate and test an electronic ring-oscillator Ising machine integrated circuit chip and show its superiority to both conventional computing methods (ML, ZF, MMSE techniques) and other Ising machines (quantum annealers and CIM) for solving the MIMO detection problem for huge MIMO systems used in wireless communications. The main superiority we expect, as discussed above, is in terms of speed/ time complexity, while providing the same level of accuracy.

Also, in this project, we would design and simulate spintronic oscillator Ising machines with spintronic domain-wall devices as coupling elements. Coming up with appropriate conductance range and values for the coupling elements is very important for getting high accuracy/ low BER for our designed OIM because conductance values determine the oscillator-to-oscillator coupling and hence the mapping of the given MIMO problem to the hardware. The magnetic tunnel junction structure needed both for the oscillator and the coupling element, along with the spin transfer toque (STT) physics in it, needed for the operation will be simulated at an atomistic level using Synopsys's Quantum ATK solver, which combines density functional theory (DFT) and non-equilibrium Green's function (NEGF). Not only the more explored heavy metal-ferromagnetic metal heterostructures will be explored but exotic two-dimensional (2D) spintronic materials will also be explored in the process. Then behavioural SPICE models will be created from these device results and then incorporated into system-level OIM designs using Synopsys's HSPICE tool.

Associated teaching plan and Relevance of Synopsys's Tools: Teaching and research will go hand in hand in the project. The PIs and the student who will get MTech/ PhD fellowship in this project will work as instructors and teaching assistant respectively in various courses offered by Department of Electrical Engineering, IITB, and use Synopsys's tools like Qunatum ATK and HSPICE..
