Department of Electrical Engineering

M.Tech. Admissions 2026-27

Abstracts of Projects
(only for PRA category)

Note:

1) This booklet contains abstracts of project for which RA positions are open.

2) These positions are other than Institute RA positions.

3) Institute RA work in various teaching labs of the department while Project RA are assigned duties on specific project.

4) Institute RA is free to choose any topic in his/her specialization for M.Tech. Thesis but Project RA may have to work for their thesis in the area of project only.

5) If you are selected for Project RA position, you will be assigned a project from your preferences and based on your performance in written test/interview. **Once selected for any project, it will not be permitted to change from one project to another.** Candidates will be asked about their preferences at the time of interview.

Project Investigator: Prof. Sandeep Anand

Title of the project: **Silicon Carbide (SiC) based Solid State Transformer**

Desired specialization: EE 3 (Power Electronics & Power Systems)

Abstract of the project:

Power electronics converters play a very important role in ac to dc conversion. The ever-increasing demand for better efficiency, reliability, and compactness has made the requirement of innovation in the area of power electronics very important. The wide band gap (WBG) devices are a new disruptive technology which would drastically change the power electronic industry. Silicon Carbide (SiC) based power devices are now commercially available and offer better performance in terms of on-state resistance and gate capacitance. These advantages help in achieving high efficiency and power density in power converters. However, there are interesting research problems in designing and developing power electronic converters using these SiC devices. This project aims to carry out research in the area of advanced power electronic converters. There are 3 open positions in this project.

If you find any one or more of the following topics interesting, then you must apply for this project:

- Design and development of Gate driver for SiC-based devices
- Topology selection and circuit design for solid state transformer (SST)
- Magnetics design for medium-voltage medium-frequency transformers development
- Controller for SST, along with grid integration
- Condition monitoring techniques for SST
- Accelerated aging and failure models of SiC devices
- Futuristic technologies for improving reliability (Active Power Decoupling and Active Thermal Control)

Project Investigator: Prof. Sandeep Anand

Title of the project: **Power Electronics for Electric Vehicles**

Desired specialization: EE 3 (Power Electronics & Power Systems)

Abstract of the project:

EVs is the stepping stone towards truly sustainable transportation solutions. The electric drivetrain consists of electric motor, its controller and onboard charger. Range anxiety and performance are some of the concerns among EV users. Hence, for a high performance and long range EV, a light weight, compact and energy efficient drivetrain is essential. Some of the topics covered under this call are:

- Motor controllers for electric vehicles
- Online health monitoring of power electronics used in Electric vehicles
- Power electronics for medium voltage dc fast chargers
- Integrated topologies for electric vehicle power electronics
- SiC based inverter for EV applications

If you find any one or more of the following topics interesting, then you must apply for this project:

- Onboard EV charger circuits
- DC-DC converters
- EV fast chargers
- Motor Drives / Inverters
- GaN & SiC based circuits

Project Investigator: Prof. Shiladri Chakraborty

Title of the project: **Power Electronics Packaging**

Desired specialization: EE 3 (Power Electronics & Power Systems)

Abstract of the project:

The broad goal of this project is to explore next-gen packaging paradigms such as double-sided Cu-sintering embedding, which can address limitations arising from using conventional packaging of fast-switching wide bandgap devices (e.g., SiC, GaN), such as parasitic inductances. The objective is to design, indigenously fabricate, and demonstrate a SiC and GaN half-bridge modules featuring extremely low power commutation loop inductances (<1.5 nH) (low loop inductances -> faster, efficient, glitch-free switching) and double-sided cooling.

Project Investigator: Prof. Maryam Shojaei Baghini

Title of the project: **CMOS IC Design and System Prototyping for Magnetic Field Sensing**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

The aim of this project is to design, develop, test and prototype the following:
1- System Design: Electronic system for magnetic field sensing using commercially available Hall sensor integrated circuits (IC's)

2- IC Design: A novel CMOS signal conditioning integrated circuit (IC) for the magnetic sensing technology based on the Hall effect for a set of target applications..

Project Investigator: Prof. Maryam Shojaei Baghini

Title of the project: **IC Design methods for RF Energy Harvesting**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

The aim of this project is to develop design methods for CMOS integrated circuits for RF energy harvesting and maximum power point tracking based power management. We use integration of classic and machine learning techniques to address the technical challenges.

Project Investigator: Prof. Maryam Shojaei Baghini

Title of the project: **Analog & Mixed-Signal IC Design and Test for On-chip Power Management in Integrated Spiking Neural Networks System-on-Chip**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

This project is a part of an ongoing research project aiming at the design, tapeout and testing of an energy efficient spiking neural network system on a chip. Efficient mixed-signal on-chip power management circuit solutions will be explored, designed and implemented on the chip.

Project Investigator: Prof. Virendra Singh

Title of the project: **Security of futuristic systems (AI/ML/AR/VR/Quantum Computing)**

Desired specialization: EE 1 (Communication & Signal Processing), EE 2 (Control & Computing), EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

Artificial Intelligence(AI) is creating a huge impact on the world by integrating its service into all possible facets of our daily life needs. Many sectors like finance, healthcare, automobiles, marketing, social media, chat-bots, etc., are using AI models like Neural Networks(NN), Large Language Models(LLMs), Reinforcement Learning(RL), etc., for their decision-making process. As it is known that with pros come cons, even a single vague decision of the model will lead everything to stake. An example of this can be a self-driving car identifying a stop sign as a speed sign which leads to destruction. There are many more such scenarios where the decisions of the AI models are making the world miserable. So, finding the vulnerabilities, providing security to the model, and making the model robust in any scenario is very crucial. In this growing machine-dependent world securing those machines is on high priority else it may lead to massive human destruction.

Project 1 (AI for Cryptanalysis of PQC problems): The advent of large-scale quantum computers promises to bring unprecedented computational capabilities, enabling efficient solutions to problems that are intractable for classical computers. While this progress marks a major milestone in computing, it also poses a significant challenge to modern cryptography. To address the challenges posed by quantum computers, NIST initiated the post-quantum cryptography (PQC) standardization process in 2016. The process culminated in selecting several candidate schemes, the majority of which are lattice-based and rely on the hardness of the LWE and the NTRU problem. This project is to develop cryptanalytics technique for PQC problems.

Project 2 (Architecting efficient system for AI/PQC algorithms): This project will envisage to develop novel hardware architecture for the AI and Post Quantum Cryptography algorithms.

Project 3 (Verification of Quantum Programs/Hardware): This project looks at the development of verification procedure to verify quantum computing programs. This also looks at the efficient implementation of such algorithms.

Project 4 (Adaptive Multi-turn Human-AI Code Collaboration): Large Language Models (LLMs) are

rapidly transforming AI-assisted software development. Despite strong performance in single-turn coding tasks, empirical studies show persistent challenges in multi-turn human-AI collaboration. Coding interactions often involve iterative clarification, debugging, and refinement, forming structured conversational patterns such as linear, branching, or exploratory dialogues. However, current LLM interfaces treat conversations as flat sequences of prompts and responses, lacking awareness of evolving interaction structure and user intent.

Project Investigator: Prof. Rahul Singh

Title of the project: **RF/Analog IC Design for Various Applications (Wireless, Quantum etc)**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

RF/Analog IC Design for Various Applications (Wireless, Quantum etc), Digital/Mixed-signal calibration engines for RF/Analog IC.

Project Investigator: Prof. Debanjan Bhowmik

Title of the project: **Quantum and Quantum-Inspired Computing to Solve Optimization Problems in Wireless Communication and Robotics**

Desired specialization: EE 1 (Communication & Signal Processing), EE 2 (Control & Computing), EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

This is an industry funded project, funded by Fractal Analytics, a multi-national AI solutions company. Combinatorial optimization problems surface in different industrial applications. Solving them using conventional algorithms and hardware requires resources that grow exponentially or at least polynomially with problem size. Two particular applications of our interest are symbol decoding in MIMO wireless communication and path panning in robotics. In this project, we will design and implement quantum computing and quantum-inspired oscillator computing schemes for solving these problems with better time complexity than conventional methods.

For more details, refer to latest publications in Prof Debanjan Bhowmik's group: https://scholar.google.com/citations?user=EkI4OAsAAAAJ&hl=en .

Project Investigator: Prof. Laxmeesha Somappa

Title of the project: **IC & System design for brain computer interface**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

The objective of this project is to develop a biomedical Integrated Circuits (ICs) and Systems that can

record brain signals, identify seizures and immediately arrest seizures for target epilepsy patients in India. This will be an indigenous biomedical system that will be developed with state of the art performance. Students will be involved in the development of the following indigenous semiconductor IPs (intellectual property) and systems: high-density neural recording (b) highly programmable neural stimulators (c) power management circuits for neural systems (d) Implantable system development using the designed ICs.

Project Investigator: Prof. Rahul Singh/ Laxmeesha Somappa

Title of the project: **RF IC Design**

Desired specialization: EE 6 (Integrated Circuit & Systems)

Abstract of the project:

IC Design of RF Analog Front-Ends, RF ADC and DAC designs.

Project Investigator: Prof. Laxmeesha Somappa / Rahul Singh

Title of the project: **VLSI AMS, Digital & RF SoC design Exploration**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

A VLSI SoC design includes design of multiple IPs spanning across Analog, Mixed-signal, Digital and RF IC design principles. Effective IP reuse is essential in realizing such SoCs. This project involves designing, fabrication and testing of such IPs, developing automated verification and test flows for faster design-test cycles.

Project Investigator: Prof. Sibi Raj Pillai, Kumar Appaiah, Sharayu Moharir

Title of the project: **Intelligent Spectrum Innovation**

Desired specialization: EE 1 (Communication & Signal Processing)

Abstract of the project:

Synergistic integration of cutting-edge wireless technologies, including Cell-free MIMO, Beam Sweeping, Reconfigurable Intelligent Surfaces (RIS), Semantic-Aware Collaborative Sensing, Mobile Edge Computing (MEC), Multi-Agent Systems.

Project Investigator: Prof. Rajesh Zele

Title of the project: **Design of analog and mixed-signal circuits for high speed serial links in Chiplet communications for DataCenters & AI applications**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

Student will be working closely with team of experienced mentors in aiCAS Lab. After going through all the relevant course work, you will be developing circuits with guidance from mentors and professor for these applications. Your work will be fabricated using cutting edge semiconductor IC fabrication technology such as 28 nm CMOS. You will be colaborating with Industry experts possibly interning in the industry. You will be encouraged to publish your work in conference.

Project Investigator: Prof. Rajesh Zele

Title of the project: **RF and Analog Circuit design for next-generation beamformer system for MIMO/6G/Radar applications**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

Student will be working closely with team of experienced mentors in aiCAS Lab. After going through all the relevant course work, you will be developing circuits with guidance from mentors and professor for these applications. Your work will be fabricated using cutting edge semiconductor IC fabrication technology such as 28 nm CMOS. You will be colaborating with Industry experts possibly interning in the industry. You will be encouraged to publish your work in conference.

Project Investigator: Prof. Bhaskaran M.

Title of the project: **TCAD based simulations of single-pixel photodetectors for space applications**

Desired specialization: EE 6 (Integrated Circuit & Systems)

Abstract of the project:

This project will be a comprehensive design of superlattice based IR photodetectors for space applications. We will be focusing on state-of-the-art TCAD simulations of fabricatable single pixel device designs with strong interactions with ISRO and DRDO.

Project Investigator: Prof. Udayan Ganguly

Title of the project: **Neural Networks Hardware - Efficient Models for Speech & Vision (Spiking & Non Spiking)**

Desired specialization: EE 1 (Communication & Signal Processing)

Abstract of the project:

1. Speech processing Neural Network Algorithms – 1 position
For this role, we will focus on the edge AI applications using neural network algorithms for spoken word recognition, denoising, speaker recognition, time series prediction and control.
The member will develop expertise in Deep Neural Network to Spiking Deep Neural Network

conversion, time series processing (e.g. LSTMs, RNNs), energy-efficient data encoding and model development, model compaction, reservoir computing, etc.

2. Vision processing Neural Network Algorithms – 1 position
For this role, we will focus on Edge AI-based vision processing for drones and space applications where energy and data efficiency are paramount.
Team: You will be working in a cross disciplinary team of Algorithms, IC Designers (AMS) and Device Engineers to build neural network chips

For more info: https://nanomemorylogic.wordpress.com/algorithms/

Project Investigator: Prof. Udayan Ganguly

Title of the project: **Neural Networks Analog Mixed Signal IC Design (Spiking & Non Spiking)**

Desired specialization: EE 6 (Integrated Circuit & Systems)

Abstract of the project:

We are building neurons and synaptic array for efficient edgeAI.
For more info: https://nanomemorylogic.wordpress.com/systems/
https://nanomemorylogic.wordpress.com/circuits/

We are looking for IC Design & Electronic System enthusiasts as PhD students. The prospective members must be motivated to engineer chips through specification development, IC design, foundry tapeout, test board design, testing, and modeling.

Applicants with a strong background in one or more topics will be attractive – (1) analog mixed signal design, (2) digital design, (3) Verilog/VHDL (4) PCB design & Chip testing. Preference is for Electrical/Electronics, Computer Science or equivalent candidates.

1. Neural Network Chip Design (Analog Mixed Signal) – 1 position
For this role, we will focus on the neural network IC design.
The member will develop expertise in advanced IC design tape-out, evaluation board design, testing for neural network chip development.

2. Electronic System Design (Sensor integration with SNN Chip) – 1 position
For this role, we will focus on the system design.
The member will develop expertise to integrate various sensors (microphones, vision cameras, accelerometers) with our AI/SNN chips and evaluation boards.

Team: You will be working in a cross disciplinary team of Algorithms, IC Designers (AMS) and Device Engineers to build neural network chips

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Project Investigator: Prof. Udayan Ganguly

Title of the project: **Devices & Technology - Memory, Synapse, Neurons (Spiking & Non Spiking)**

Desired specialization: EE 7 (Solid State Devices)

Abstract of the project:

We are building neurons and synaptic array for efficient edgeAI.

The SOI transistor based neuron show tunneling current based low power
Memories like RRAM and Ferroelectric RAM based synapses show compact data storage for synaptic applications.

For more info:
https://nanomemorylogic.wordpress.com/resistance-ram/
https://nanomemorylogic.wordpress.com/circuits/

Applicants with a strong background in one or more topics will be attractive – (1) device physics, (2) nanofabrication, (3) TCAD, and compact modeling of transistors/memory, (4) materials engineering. Preference is for Electrical/Electronics, Materials/Metallurgy, Physics-trained or equivalent candidates.

1. Device Engineering (Neuron) – 1 position
For this role, we will focus on the neuron. We use quantum tunneling in silicon and Silicon-Germanium transistors at a 45 nm node to build neurons. The member will develop expertise in design, nanofabrication, testing, and modeling these transistors to emulate the neurons.

2. Device Engineering (Synapse) – 1 position
For this role, we will focus on the synapse.We use Resistive Random Access Memories (RRAM), One-Time Programmable (OTP) Memories, and Ferroelectric memories to develop compact, low-power synapses.The member will develop expertise in engineering electron and atomic motion in insulating oxides (e.g. HfO2, PrCaMnO, etc.) based devices to enable data storage.

Team: You will be working in a cross disciplinary team of Algorithms, IC Designers (AMS) and Device Engineers to build neural network chips.

Project Investigator: Prof. Pradeep Nair

Title of the project: **Perovskite/Silicon Tandem Solar Cells**

Desired specialization: EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

Solar energy conversion has made rapid strides to meet the energy requirements of mankind. Among the various technologies, tandem cells based on Perovskite top cell and Silicon bottom cell are expected to dominate the market in the near future. In this project, through predictive modeling, we aim to understand and optimize the various key challenges related to material characterization, device performance, large scale depolyment, and techno-economic feasibility of Perovskite/Si tandem solar cells. The project involves analysis of experimental data and numerical simulation.

Project Investigator: Prof. Rajbabu Velmurugan

Title of the project: **Continual and federated learning in vision and image processing**

Desired specialization: EE 1 (Communication & Signal Processing)

Abstract of the project:

The field of continual learning has studied how to learn sequentially without forgetting, but largely on toy benchmarks. The field of federated learning has studied how to train across distributed data owners, but almost entirely for singletask, stationary distributions. This project aims to address some of the gaps in both these domains in a connected way, moving from the foundations of continual and federated learning for traditional vision tasks towards a principled treatment of their combination and their application to vision–language models..