Development of a Robust Phase Locked Loop System under Distorted Utility Conditions

M.P. Bhawalkar, Dr. Gopalakrishnan
Department of Electrical Engineering,
PVG’s College of Engineering & Technology, acronyms Pune 411 009, India
E-mail: mpb_elect@pvgcoetac.in

Dr. Y.P. Nerkar
Principal, PVG’s College of Engineering & Technology,
Pune 411 009, India

Abstract—Increased level of automation by using sophisticated equipment employing switched mode supplies, use of power electronic controllers and non-linear loads have increased disturbances and distortions in electric grid. These distorted utility conditions create additional problems of synchronization for line interactive power converters with grid. Further certain transient events like unsymmetrical faults, load unbalance, supply imperfections result in deviation of voltage of one or more phases leading to mis-operation of many phase-control applications. The situations are worst at point of interface of renewable energy sources connected through weak system. This paper proposes a simpler solution based on the detection of positive sequence voltages for tracking grid voltage and phase under unbalanced and highly distorted grid situations. The proposed detection method together with evaluation of PLL through a simulation study is described.

Keywords—Phase Locked Loop (PLL), Utility Disturbances, Positive Sequence Detectors

I. INTRODUCTION

One of the most important problems in renewable energy sources and intelligent grids is to interface and synchronize power electronic converters with neighbouring utility grid. There may be numerous problems at the time of interconnection and even at operative states because of voltage sag, flickers, harmonics, inrush currents etc. Further the increasing use of advanced power controllers such as Static Compensators (STATCOMs), Static VAR Compensators (SVCs), Uninterruptible Power Supplies (UPS) and Dynamic Voltage Restorer (DVR) put additional burden at the time of interfacing weak energy sources. All these interconnecting operations necessarily require accurate information of grid voltage and its phase angle for satisfactory operation. Therefore there is a need of simple and reliable phase detecting or tracking mechanism under unbalanced and distorted grid conditions exist. For this purpose different algorithms and approaches have been tried out. Methods commonly employed for frequency identification are derived from Zero Crossing Techniques (ZCT), Adaptive Discrete Fourier Transform (ADFT) and demodulation techniques. After detection of frequency the methods used for locking the phase can be classified as open loop method such as low pass filters, space vector filters, extended Kalman Filter and close loop systems such as Phase Locked Loop (PLL) [1-6].

Closed loop methods introduce a mechanism for providing accurate information of utility voltage. Many PLL techniques that have been commonly used with closed loop mechanism to track the utility voltage are reported in literature [7]. The PLL widely used in single phase and three phase systems are based on synchronously rotating frame [3]. A typical PLL consists of phase detector, loop filter and voltage controller oscillator blocks. These blocks measure the phase difference between input and derived output signal and then pass to filter to extract dc component from phase error. The DC component is amplified and then passed to voltage controlled oscillator which will be a proportionate integral controller to minimize tracking errors and gives frequency as output signal. Other relevant blocks contribute to extract phase information. On good latching of input signal frequency and output, the output of phase detector eventually tends to be zero. It works fine for majority of single phase applications or strictly under balanced three phase utility and load
conditions. When distorted utility conditions and unbalance in three phase voltages exist, it has resulted in numerous detection errors and associated synchronization problems. Especially in case of micro-grid interface with local grid or renewable energy source integration to weak distribution network the problems are more serious [2]. To avoid these problems robust PLLs are required. Recent close loop phase detection techniques such as adaptive PLL, enhanced PLL, auto-adjustable synchronous reference frame (SRF) PLL, decoupled double synchronous reference frame PLL etc. are good examples [4][6][8].

A robust PLL should have following desirable properties:
1. Fast response
2. Accurate indication of unbalanced conditions.
3. Immunity to change in voltage magnitudes and harmonics in the input signals.
4. Adaptability to changes in utility frequency.
5. Detection of fundamental frequency and positive sequence component under all conditions of unbalance including harmonic pollution.

In the power electronic applications especially in vector control of drives or sensorless drives, PLL finds applications for measuring \( \theta \) i.e. rotor position with respect to stationary frame [5]. Further this information is useful for conversion of three phase voltages and currents into Clarke and Park transformations.

The method of extracting information of phase under normal conditions can be done with PLL developed in where performance is good under distorted conditions as well as with unbalanced supply conditions [9][10]. This paper examines a different approach for an effective and robust phase locked loop for three phase systems and discusses its development. A comprehensive model of PLL is developed with typical SRF, PI/PD regulators, band pass filter, integrator and positive sequence detectors. After discussing the conventional three phase PLL and its limitations, subsequent sections describe the details of simulation studies of the new PLL.

II. THREE PHASE PLL

A conventional three phase PLL based on SRF is shown in Fig. 1. The three phase balanced voltages are transformed into synchronously rotating reference frame from natural reference with the assumptions that zero sequence components are absent as neutral is isolated frame by using Clarke’s transformation \([v_{abc}] \) to \([v_{αβ}]\). Additional transformation is required to get direct and quadrature axis voltages \(v_d\) and \(v_q\) respectively by using Park’s transformation. The angular position theta (\(θ\)) is controlled by a feedback loop which regulates voltage \(v_q\) to zero by a PI regulator under steady state condition. The mathematical equations involved in this process are given below.

\[
\begin{bmatrix}
v_a(t) \\
v_b(t) \\
v_c(t)
\end{bmatrix}
= \begin{bmatrix}
V_m \cos(\theta) \\
V_m \cos(\theta - 2\pi/3) \\
V_m \cos(\theta + 2\pi/3)
\end{bmatrix}
\]

Transferred voltages in \(αβ\) and \(dq\) frames are given by Eq. (2) and Eq. (3) respectively as zero sequence components are assumed to be absent [12].

\[
\begin{bmatrix}
v_a \\
v_b
\end{bmatrix}
= \begin{bmatrix}
1 \\
\frac{-1/2}{\sqrt{3}/2}
\end{bmatrix}
\begin{bmatrix}
v_{α} \\
v_{β}
\end{bmatrix}
\]

\[
\begin{bmatrix}
v_d \\
v_q
\end{bmatrix}
= \begin{bmatrix}
\cos(\theta) & -\sin(\theta) \\
\sin(\theta) & \cos(\theta)
\end{bmatrix}
\begin{bmatrix}
v_α \\
v_β
\end{bmatrix}
\]

Under ideal utility conditions extraction of fast and accurate information of phase and magnitude of utility phase voltages, a higher band width of PLL is
adopted to give $v_q$ close to zero. Eventually under this condition there are no oscillations in decomposed voltage components $v_d$ and $v_q$ obtained from Eqs. (1) to (3). PLL tracks utility voltages without undue tracking errors and minor fluctuations of voltages and frequency are taken care of by the integrator which serves as low pass filter.

Ideal utility conditions are very rare in practice and usually grid voltages are unbalanced and/or distorted due to innumerable reasons. The PLL designed on the basis of SRF only will not be in a position to tackle these non-linearities. It ends up with distortion and errors in measured phase angle and associated locking up. This situation arises due to imperfection in transformations represented by equations (1)-(3) as it assumes that grid voltage is presented by fundamental frequency positive sequence voltage only.

The behavior of SRF-PLL under unbalanced utility voltages is examined in Fig 2. The utility voltages are represented by Eqs (4), (5) and (6) which contain positive sequence and negative sequence voltage fundamental components only.

$$
\begin{align*}
 v_a &= V_a^+ \cos(\omega t) + V_a^- \cos(-\omega t) \\
 v_b &= V_b^+ \cos(\omega t - \frac{2\pi}{3}) + V_b^- \cos(-\omega t + \frac{2\pi}{3}) \\
 v_c &= V_c^+ \cos(\omega t + \frac{2\pi}{3}) + V_c^- \cos(-\omega t + \frac{2\pi}{3})
\end{align*}
$$

where +1 and -1 indicate fundamental frequency positive and negative sequence voltages respectively.

The source voltages as represented by above equations are shown in Fig. 2a. The dq voltages obtained after transformation are shown in Fig. 2b which clearly indicates that ripples of 100Hz are present. The amplitude of ripples will increase with negative sequence voltage level. The major reason for this is the resulting phase shift due to voltage imbalance. Fig. 2c shows deviation of phase angle $\theta$ as it is not perfect saw tooth waveform. Any error in phase detection can lead to mis-operation of grid connected phase control applications, VSDs and other power electronic controllers. Similar situation arises under heavily distorted voltage conditions even though integrator works as a filter. It cannot eliminate distortion in measured phase angle and performance of PLL will degrade as shown in Fig. 2b and Fig.2c. Sometimes a reduction in bandwidth resulting in blocking of or bypassing harmonic components may give good results [7]. Under unbalanced supply voltages, however a mere reduction in bandwidth gain of PLL will not be an error free solution in tracking the grid voltage [8]. It can also be seen from Fig. 2 that amplitude and phase angle may not be precisely obtained from the derived signals. This shows that PLL based on detection of positive sequence voltage and phase angle is a must. To reduce the error in phase detection technique either a low pass filter or a band pass filter on the utility side may have to be incorporated. In this work a band-pass filter is used with cut off frequencies of 48Hz and 52Hz.

III. PROPOSED PLL METHODOLOGY

A second order Butterworth Band Pass Filter (BPF) is traduced here to block unwanted frequency components present in utility voltages. The transfer function is given by Eq. 7 [10]

![Fig 2. a) Unbalanced utility voltages, b) Decomposition of supply voltage into Vd and Vq c) Phase of input voltage (θ) in radians](image-url)
is employed with cut off frequencies of 48 - 52 Hz. In Eq. (7) \( \xi \) indicates damping ratio and \( \omega_n \) is natural frequency. The value of \( \xi \) is 0.707 so that over shoot in response is restricted and \( \omega_n \) is selected as 50Hz. The filter simply allows fundamental frequency components of grid voltages to pass on for further processing. Fig.3 shows magnitude response, bode plot for band pass filter respectively.

![Fig. 3 Band pass filter magnitude plot and Phase plot](image)

BPF is followed by a positive sequence voltage detector based on instantaneous symmetrical components given by Eq (8) [11, 12, 13, 14]. This in turn followed by Clarke and Park transformations blocks, PI regulator and integrator to obtain phase of supply voltage.

\[
\begin{bmatrix}
V_a \\
V_b \\
V_c
\end{bmatrix} = [A]
\begin{bmatrix}
V_{a0} \\
V_{a1} \\
V_{a2}
\end{bmatrix} \tag{8}
\]

Where \([A]\) is given by \( A = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \)

and \( a \) – represents the complex operator \( a = e^{j2\pi/3} \)

There is possibility that a voltage offset may be present along with harmonics in utility voltages. This is predominantly due to conversion circuits such as rectifiers, offsets in measurement devices. The direct axis voltage \( V_{1d} \) is used as a reference voltage signal for end user applications. The quadrature voltage \( V_{1q} \) is forced to zero through PI regulator, low pass filter and integrator. It is used to measure frequency and \( \theta \). This proposed PLL will be called PSD-PLL in this paper as it incorporates positive sequence detector. All these blocks are integrated in Fig 4 to form PSD PLL.

![Fig 4 Block diagram of proposed PSD-PLL](image)

IV. SIMULATION RESULTS AND DISCUSSIONS

The capability and appropriateness of PSD PLL is examined in this section for different power quality events usually occurring in the grid: Case 1 Sudden change in utility voltage, Case 2 Sudden change in frequency (=2.5Hz) and Case 3 Distorted utility conditions. The PLL configuration shown in Fig 4 is simulated in MATLAB platform.

A. Case I Sudden change in utility voltage:

Clearing of faults, recovery of voltage sag, switching of capacitor banks, and heavy load rejection are common problems of sudden changes in utility voltages. An ideal PLL should always track phase of fundamental component of system voltage. In Fig. 5a the utility voltages are normal from \( t = 0 \) to \( t = 2 \) sec when sudden swell in utility voltage is introduced. Transients occurred are shown in Fig. 5a – d These transients in positive sequence voltages last for 1 cycle and steady state is obtained after transients are over. The \( \cos(\theta) \) wave coincides with \( V_{1a} \) indicate that correct synchronization is achieved.

B. Case III PLL Subjected to sudden small changes in frequency (\( \Delta f = 2.5Hz \)):

It is noticed that grid frequency also changes simultaneously with grid voltage. The response of PLL for a sudden small changes in frequency of 2.5Hz (50 – 47.5 – 50 -52.5 -50 Hz) is examined. In this case Fig. 6(a) shows input voltage with step
changes in frequency. Fig. 6(b) shows extracted positive sequence fundamental voltages. Fig. 6(c) and Fig. 6(d) show measured theta and Va and \(\cos(\theta)\) respectively. At the instant of sudden change clear distortion can be observed in positive sequence voltages and in measured phase as shown in Fig. 6(b) and Fig. 6(c). At time of 1 sec frequency is changed from 50 Hz to 47.5 Hz and at time 1.1 sec. frequency restored back to 50Hz. At time 1.2 sec. frequency again suddenly changes to 52.5 Hz and restores back at 1.28 sec. The PLL tracks the signal within a reasonable time of half cycle about 10 msec when frequency is restoring to 50 Hz in either case. However PLL takes time of one cycle about 20 msec to track signal when frequency suddenly changes to either side. This can be inferred from Fig. 6(c) and Fig. 6(d).

**Fig 5 Behaviour of PLL to sudden change in input voltages**

- a) Input voltages
- b) Positive Sequence Fundamental Voltages
- c) Measured phase of input voltage(\(\theta\))
- d) Va and \(\cos(\theta)\)

**Fig 6 PLL response with sudden change in frequency (47.5 Hz to 52.5 Hz and back to 50 Hz)**

- a) Supply voltages
- b) Positive sequence voltages
- c) Measured phase (\(\theta\))
- d) Va and \(\cos(\theta)\)

**C. Case III Distorted utility voltage:**

The performance of PLL is tested with different levels of distortion contributed by different harmonic components. The test results of PLL for the presence of 15% third and 15% fifth harmonics in utility voltages are illustrated in Fig. 7(a-d). The phase sequence of fifth harmonic is assumed to be same as that of positive sequence. The supply voltages are represented by Eqs. (12-14). Fig 7. (a) shows distorted utility voltages applied to PLL and Fig. 7.(b) indicate positive sequence fundamental voltages. Fig. 7(c) shows output of PLL i.e. \(\theta\).

\[
\begin{align*}
V_a &= V_1 \cos \theta + V_3 \cos 3\theta + V_5 \cos 5\theta \\
V_b &= V_1 \cos(\theta - \frac{2\pi}{3}) + V_3 \cos(3\theta) + V_5 \cos(\theta - \frac{2\pi}{3}) \\
V_c &= V_1 \cos(\theta + \frac{2\pi}{3}) + V_3 \cos(3\theta) + V_5 \cos(\theta + \frac{2\pi}{3})
\end{align*}
\]
The tracking of PLL is good even under this case and synchronization time is about 10msec which can be clearly seen from Fig. 7d. showing $V_{1a}$ and $\cos(\theta)$ waveforms are in phase.

Fig 7 Response of PLL with distorted voltage. a) Input voltages b) Positive Sequence Fundamental Voltages c) Measured phase of input voltage($\theta$) and d) $V_a$ and $\cos(\theta)$.

V. SIMULATION RESULTS AND DISCUSSIONS
The proposed PSDPLL has a good static and dynamic performance which can be inferred from the results of simulation study presented for cases resembling to practical situations frequently occur in a grid. PLL takes around 10 to 12 msec to respond for a sudden change in input voltage or frequency. This indicates that addition of a filter does not add undue time delay.

REFERENCES