Abstract—This paper presents design and development of three-level inverter for five-phase motor drive system. Multi-level multi-phase inverters are more complex due to higher number of switches, hence inverter reliability is at stake. Main objective in developing such circuits is to implement inbuilt protection feature to switch to improve operational reliability. The short circuit protection to inverter switches is implemented using desaturation principle where collector to emitter voltage ($V_{CE}$) is monitored through a reverse connected diode. This scheme along with gate driving circuit, optical isolation and dead-band generation is incorporated in a modular way. False triggering issue pertaining to three-level inverters are discussed and appropriate circuit modifications are suggested. Various efforts in PCB designing to minimize EMI issues are elaborated. Detailed design considerations are followed to develop laboratory prototype and performance is verified by experimental results.

Keywords—short-circuit protection, three-level five-phase inverter, gate driver circuit, optical isolation.

I. INTRODUCTION

Recently multi-phase drives has gained much attention in application areas like ship propulsion, hybrid and electric vehicles, traction owing to advantages viz. higher fault tolerance, reduced amplitude and increased frequency of torque pulsation, reduced DC-link current harmonics, reduced component size due to higher power density and reduced current per phase compared with traditional three phase drives [1], [2]. Further multilevel inverters are proposed alternative for medium/high power industrial application with advantages like low output harmonics in voltage/current, low switching losses and reduced $dv/dt$ [3]. Thus multi-level multi-phase drives are better option in context to above mentioned advantages. Research activities related to five phase drive systems accounts for development of reliable inverter with fault tolerant capabilities.

In paper [4], various techniques for fault diagnostics and protection methods of power inverters are reviewed. Design, development and implementation issues related to DSTATCOM are presented and protection circuit using comparators is proposed [5]. A circuit for protecting power switches by continuous $V_{CE}$ monitoring against hard switched faults and fault under load is presented in [6]. This technique of continuous $V_{CE}$ monitoring for fault detection used for protection of Neutral Point Clamped (NPC) inverter cause spurious trippings [7]. In this paper, modified gate drive circuitry is used with a detailed documentation on design, development and implementation for five-phase three-level NPC-inverter.

This paper is organized in five different sections. In Section II, selection of power semiconductor devices and DC-link capacitor is presented. In Section III, driving and protection circuitry is discussed with fair design considerations. In Section IV, optimum layout and bypassing considerations are listed and used accordingly. In Section V, experimental results pertaining to inverter are presented to validate the design.

II. THREE-LEVEL FIVE-PHASE INVERTER

Voltage Source Inverter (VSI) is required to generate appropriate voltage vectors to drive induction motor satisfactorily. A typical VSI may contain suitably connected power electronic switches (MOSFET, IGBT, Thyristor, GTO etc.) with anti-parallel diodes, clamping diodes, DC voltage source, filter capacitor, and coupling transformers. Fig. 1 shows the power circuit of a three-level five-phase inverter. Considering designing of a NPC-inverter with DC-link of 600 V, Semikron make SKM50GB063D NPT-trench IGBT module is used as part of main switches in each leg and IXYS make fast recovery epitaxial diode DSEI 2x30-06c is used as neutral point clamping diode.

A. DC-Link Capacitor Selection

For a rectifier - inverter drive system, DC-link capacitor is required to carry inverter and rectifier currents. When electrolytic capacitors are used, sizing is done by calculating the current required to be handled. The inverter and rectifier currents can be calculated using equation (1) and (2) [8].

\[
I_{i(rms)} = 1.060 \times M \times \cos(\phi) \times I_{o(rms)} \sqrt{\frac{0.98 \times \cos^2(\phi) + 0.245}{M + \cos^2(\phi) - 1}} \quad (1)
\]
For maximum inverter current, $M = 0.6$ and $\phi = 0$

\[
I_{(rms)} = 1.060 \times 0.6 \times 6 \times \sqrt{\frac{0.98 + 0.245}{0.6}} = 5.4522A
\]

\[
I_{r(rms)} = 1.23 \times I_{dc} \times (F_i - 1.73)^{0.551}
\]

where,

- $I_{dc}$ = required rectifier output dc current
- $F_i$ = current form factor

At the edge between continuous current and intermittent current, $F_i = 2$

\[
I_{r(rms)} = 1.23 \times 8 \times (0.27)^{0.551} = 4.82A
\]

Considering these calculated current values two electrolytic capacitors (ALCON PG-LL9) with rating $415VDC / 2200 \mu F$ [9] connected in series are selected for DC-link.

III. DRIVING AND PROTECTION CIRCUITRY

A. Dead-Band Generation Circuit

The IGBT switches used in inverter have some finite value of rise and fall time. When connected in a leg, fed by complementary switches, the switches tend to short the DC-link capacitor due to these finite rise/fall time. Therefore, it is necessary to introduce dead-band between the two complementary signals. A programmable dead-band generator IC (IXDP 631PI) is used for dead time generation. IXDP 631PI generates complement pulse with programmed Dead-band for every input pulse.

\[
I_t = \frac{V_{F}}{R_{F}} = \frac{3.3}{0.01} = 330V
\]

Where,

- $r_{d(off)}$ = maximum turn off delay time.
- $r_{d(on)}$ = minimum turn on delay time.
- $r_{pd(max)}$ = maximum driver propagation delay.
- $r_{pd(min)}$ = minimum driver propagation delay.

Referring data sheet of IGBT module [11] and gate driver IC [12] and placing them in (3) gives,

\[
t_{dead} = [(400 - 70) + (300 - 80)] \times 1.2 = 825ns
\]

Hence, crystal frequency to generate required dead-band as given in [13] can be stated as,

\[
f_{clk} = \frac{8}{t_{dead}} = 9.7MHz
\]

Taking the nearest value, 8 MHz crystal hence, 1 $\mu s$ dead band is used. The switching frequency of inverter is decided according the type of PWM technique used and its application with minimizing EMI. Selection of switching frequency is dependent on application of inverter.

B. Optical Isolation

The logic control signals from dead-band generator circuit cannot be applied to IGBT which are connected in power circuitry. Therefore high speed optical isolators (6N137) are used to provide optical isolation between control and power circuit. The optical isolator operates in active low configuration which interfaces correctly with active low requirement of gate driver.

1) Calculation of Input Resistance: It is essential to provide emitter current limiting resistor. According to data sheet [14] the optical isolator parameters are given by, as follows:

Input Current ($I_F$) = 10 mA
Input Forward Voltage ($V_F$) = 1.4 V
High level switching pulse ($V_H$) = 3.3 V

Input resistance $R_{sp}$ is calculated as,

\[
R_{sp} = \frac{V_H - V_F}{I_F} = \frac{3.3 - 1.4}{0.01} = 190\Omega
\]

Fig. 2: Dead-band generation circuit
2) Calculation of Output Resistance: Depending on the current capacity of transistor and the supply voltage, output resistance can be calculated. According to data sheet [14] the optical isolator parameters are given by.

Optical isolator biasing voltage ($V_{CC}$) = 5 V
Maximum collector current ($I_C$) = 10 mA

Therefore, minimum output resistance is,

$$R_{op} = \frac{V_{CC}}{I_C} = \frac{5}{0.01} = 500\Omega$$

C. Gate Driver Design

A considerable amount of gate drive power is required to operate IGBT between low and high impedance states. Number of ways exist to drive IGBT using hard wired electronic circuits. But the easy and preferred way is to use gate driver IC as they are convenient, compact and incorporates a wide variety of features. Here gate driver circuit is designed using IC MC33153. It has features viz. high current output stage, bipolar gate drive capability, undervoltage lockout and short circuit protection with programmable fault blanking time [12]. NPC-inverters tend to show spurious tripplings due to false detection of short circuit condition during switching transients and different load power factors in the inner switches [7]. This is avoided by disabling the desaturation fault detection circuitry for inner switches (e.g. $S_{A1}, S_{A2}$ for a-phase) by connecting desaturation pin to ground instead of collector for respective drivers. Such modification causes no compromise on reliability as all inverter short circuit faults involve one of the outer devices (e.g. $S_{A1}, S_{A2}$ for a-phase)

$$P_I = I_{CC,max} \times (V_{CC} - V_{EE}) + \Delta V_{GE} \times Q_G \times f_{sw}$$
$$P_I = 7.9 \times ((15 - (-5)) + 20 \times 500 \times 15 = 308mW$$

This loss is much lower than specified in datasheet (1 W) hence gate driver can be used reliably.

2) Calculation of Blanking Capacitor : Owing to finite value of rise time delay of IGBT, desaturation fault detection circuitry must remain disabled for this time following the turn-on of IGBT to allow the collector voltage to fall below desaturation threshold. Referring the datasheet of driver IC and IGBT module for calculating blanking capacitor value, required parameters are noted as,

Internal desaturation current change ($I_{CHC}$) = 270 $\mu$A
desaturation voltage ($V_{DESAT}$) = 5.8 V

For blanking time of 0.5$\mu$s the blanking capacitor can be calculated using (5) [15] as,

$$C_{BLAK} = \frac{I_{CHC} \times T_{BLANK}}{V_{DESAT}} = \frac{270 \times 10^{-6} \times 0.5 \times 10^{-6}}{5.8} = 25pF$$

Ultrafast diode (UF4007) in series with a current limiting resistor (100 $\Omega$) is used to connect desaturation sense pin to collector terminal.

3) Fault Feedback Resistor: In order to provide fault feedback with isolation, optical isolator (6N137) is used. To limit the emitter current a resistor $R_{FB}$ is used. Referring to optical isolator datasheet the emitter requirements can be given as,

Input current ($I_F$) = 10 mA
Input forward voltage ($V_F$) = 1.4 V
High level switching pulse ($V_H$) = 13.3 V

Fault feedback resistance is calculated as,

$$R_{FB} = \frac{V_H - V_F}{I_F} = \frac{13.3 - 1.4}{0.01} = 1.2k\Omega$$

D. AND Gate Latching Logic

Fault pulses coming from fault feedback isolator of each gate driver are ANDED together locally using AND gate IC (74LS21). Current limiting resistors (1 $k\Omega$) are connected in series with the input channel. Latching is done by connecting a resistor between enable and one of inputs, this ensures continuous enable pulse to enable pin of dead-band generator IC once enabled by DSP/switch. After fault, latch is automatically removed locally. Enable signal can be given to DSP for further required actions.

E. Auxiliary Power Supply

Operation of various circuits require regulated DC power supplies as specified in Table I. A single toroidal ferrite core transformer with single primary (230 V) and multiple secondary (15-0-15 V / 500 mA) is used to build isolated power supplies. Full-bridge diode rectifier configuration with 1000 $\mu$F smoothing capacitor is used to make power supply as shown in fig 6. Midpoint of capacitors is connected to centre tap of secondary windings creating a local ground (GND). The
TABLE I: AUXILIARY POWER SUPPLY REQUIREMENTS

<table>
<thead>
<tr>
<th>Part</th>
<th>Power Supply</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Driver</td>
<td>+15/-5 V</td>
</tr>
<tr>
<td>Feedback Optical Isolator</td>
<td>+5 V</td>
</tr>
<tr>
<td>Dead-band generator</td>
<td>+5 V</td>
</tr>
<tr>
<td>AND Gate</td>
<td>+5 V</td>
</tr>
</tbody>
</table>

unregulated DC is given to voltage regulator ICs 7815 and 7905 to obtain regulated dc output voltages of +15V and -5V, respectively. The +5V can be generated using single secondary coil with 7805 voltage regulator IC.

IV. OPTIMUM LAYOUT AND BYPASSING CONSIDERATIONS

Inverter switching generates EMI which contribute to interference in electronic circuits. Improper layout design and unnecessary track lengths may also create ringing in signals. One such case of noise during development in circuit is shown in fig.7. For reliable operation of designed circuitry various layout and bypassing considerations are taken into account.

1) Copper ground plane introduces capacitive effect hence minimizing line inductance.
2) Double layered PCB ensures more number of signal jumping in less space.
3) Auxiliary power circuit can be placed on same board to ensure reduction of interference path.
4) A FRC cable with alternate signal and ground can used for communication between driver and control board.
5) Bypassing capacitors should be placed near each IC ensuring supply of high frequency currents.
6) For minimum DC-link stray inductance an aluminium strip can be used.

Fig.9 represents an attempt to design optimum layout using the above accounted considerations. 1. shows use of copper grounding plane. 2. represents the use of double copper layers for jumping signals in less space. 3. shows placing of auxiliary power supply layout on the same gate driver board. 4. represents the FRC cable socket layout wherein alternate signal and ground are connected. 5. shows placement of bypassing capacitors near to the IC supply pins. Fig.8 shows signals after optimum layout design. It can be seen that the noise is reduced drastically.

V. EXPERIMENTAL RESULTS

Fig.10 represents picture of developed three-level five-phase inverter. Fig.11 shows gate voltage $V_{GE}$ and gate current $I_G$ for turn-on and turn-off conditions. It is observed that the gate currents for respective timings, 760 mA and -1232 mA are within the specified limits of gate driver.

To verify fault detection circuit operation, a short circuit condition is created by dead short circuiting load terminals. Fig.12 shows short circuit detection phenomena. IGBT gate voltage, collector current and gate pulse enable signal are monitored. Current starts rising once short circuited, once $V_{CE(SAT)}$ reaches 5.8 volts gate pulses are blocked by fall of gate pulse enable signal to zero. Once enable signal goes zero all the gate pulse to switches are disabled.
The designed system is tested on SPWM technique for various modulation indexes and fundamental frequencies for switching frequencies up to 10 kHz. Fig. 13 and Fig. 14 represent voltage and current for three-level five-phase inverter operated at 500 V DC-link feeding five phase induction motor with modulation index $m = 0.9$ and $f = 50$ Hz.

VI. CONCLUSION

This paper has presented design and development of fault tolerant three-level five-phase inverter. Short circuit protection of inverter is successfully tested by dead short circuiting load terminals. Spurious tripping observed in three-level NPC-inverter is addressed by stated modification in gate driver circuit. Optimum design and development of PCB layout is attempted by taking various design considerations into account. Presented design considerations are followed to develop laboratory prototype and performance is verified by experimental results.

REFERENCES

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