Performance Analysis of Hybrid Cascaded Multilevel Converter for HVDC Transmission

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Abstract — HVDC transmission systems deals with bulk amount of power, therefore protection of these systems is highly important. This paper presents newly introduced voltage source converter with DC fault blocking capability, known as hybrid cascaded multilevel converter. This converter has ability to prevent any uncontrolled fault current to flow from AC to DC side during DC faults, without the action of AC circuit breaker. This feature blocks power exchange between AC and DC side and may eliminate need of DC circuit breaker. HCMC provides various features of multilevel converter. Converter is able to operate over an extended modulation index range, independent of load power factor. This paper presents DC fault blocking capability of hybrid cascaded multilevel converter. Converter performance before fault and during fault is examined.

Keywords — HVDC transmission; hybrid cascaded multilevel converter; nearest level control; Capacitor voltage balance control; dc fault blocking capability.

I. INTRODUCTION

HVDC transmission systems play an important role in integration of renewable energy sources from remote location to grid. Development of HVDC technology depends on evolution of converters used for AC to DC and DC to AC conversion. Basically HVDC converters are classified into two distinct classes 1) CSCs (current source converters) and 2) VSCs (voltage source converters). VSCs are more advantageous as they provide additional controllability along with black start capability, independent active and reactive power control and active power reversal without change in DC link voltage polarity [1].

Conventional two level VSC requires large number of semiconductor devices to be connected in series in each valve. For high voltage operation they require high switching frequency which leads to high conversion losses and poor voltage quality. Multilevel converters like 1) Neutral point clamped converter; 2) flying capacitor converter; 3) cascaded H-bridge converter; and 4) Modular multilevel converter (MMC) achieves better performance than conventional VSCs. They eliminate the need of large number of series connected devices. Recently, MMC has been recognized as most suitable multilevel converter for HVDC medium and high voltage applications. This converter reduces switching losses and minimizes grid side filtering requirement. Protection of HVDC transmission systems is key issue for the future development. However, no effective high voltage DC circuit breaker is available in power market. Installation of AC circuit breaker is one of the choices, but due to their slow response they require high rating semiconductor devices to withstand large fault currents. Protection can also be achieved through converter action. Unfortunately all developed VSCs are weak against dc side faults.

Newly introduced a hybrid cascaded multilevel converter (HCMC) with DC fault blocking capability [2]-[7] has a solution on the above mentioned problem. The proposed version consists of two level converter having director switches (DSs) as high voltage stage and stack of H-bridge cells, called as wave-shaping circuit (WSC) as low voltage stage. The features of HCMC are:

- Modularity and scalability;
- Two level converter operates at fundamental frequency, hence reducing switching losses;
- WSC acts as series active harmonic filter attenuating low order harmonics thus eliminating need of filtering;
- Low dv/dt;
- In the event of DC side fault, HCMC prevents any uncontrolled fault current to flow from AC side to DC side and avoids failure risk of switching devices. This feature also blocks power exchange between AC and DC side;
- Converter provides modulation index extension independent of load power factor.

For hvdc power transmission system, generation of multiple isolated dc power supplies is impractical. Therefore H-bridge dc supplies in WSC are replaced by capacitors. Voltage ripples in sub-module capacitors leads to the unequal voltages across the three phases of converter which increases circulating current, consequently converter losses. In order to reduce the circulating current, capacitor voltages are balanced by using sorting technique and triplen harmonic injection method.

In this paper feasibility of modulation and control technique of HCMC under normal mode condition is investigated with MATLAB simulation. In order to examine the performance of HCMC in worse case DC side faults, system is subjected to pole to pole DC faults. Issues such as output voltage and current quality are discussed. Capacitor voltage balancing during fault duration is examined.
II. Converter Configuration

Converter consists of main two level converter and wave-shaping circuits. Director switch is series connection of large number of IGBTs. Two level converter gives desired fundamental voltage component by switching between $+1/2 U_{dc}$ and $-1/2 U_{dc}$. Two level converter operates at fundamental frequency, thereby reducing switching losses. Wave-shaping circuit is having stack of H-bridge sub modules (SMs) which generates multilevel output voltage. Capacitor voltage of each SM should be maintained so that it will not exceed switch device rating. In this paper nearest level control technique is used for generation of switching pulses. Capacitor voltages are balanced by using sorting technique and third harmonic injection method.

HCMC consists of n SMs per phase as shown in Fig. 1. During normal operation each SM will have three operating states i.e., (1) positively inserted, $U_{SM} = U_C$; (2) negatively inserted, $U_{SM} = -U_C$; and (3) bypassed $U_{SM} = 0$. At unity modulation index, converter exploits all n SMs to generate required output voltage waveform between $+1/2 U_{dc}$ and $-1/2 U_{dc}$. Voltage across each SM capacitor must be maintained at $1/2 n U_{dc}$.

III. Modulation Scheme

A. Gate Pulse Generation for DSs

Switching pulses for DSs are generated by comparing phase output voltage reference ($v_p^*$) with zero. If $v_p^*$ is greater than zero, upper DS will be switched on and if $v_p^*$ is less than zero, lower DS will be switched on. Under normal operating conditions switching pulses given to the DSs in one phase are complimentary. Director switches operate almost at fundamental frequency. Under normal operating conditions pulses given to DSs in one phase are complementary.

B. Nearest Level Control with Third Harmonic Injection

Nearest level control (NLC) [8] is low switching frequency technique which is applicable to large number of SMs for high power range. It controls the number of SMs to be inserted for given operating cycle. Nearest voltage level that can be generated by converter is obtained by dividing input reference by SM capacitor voltage as shown in Fig. 1. Then number of SMs to be turned on is calculated by using function Round ($x$), which is integer nearest to $x$ (for example, round (5.2) = 5 or round (5.7) = 6). Therefore, this method is also called as a round method.

Input reference for NLC is obtained by injecting third harmonic into it. Third harmonic injection causes suppression of input reference between $\pm 1$ and thereby reduces required number of series H-bridge cells to minimize conversion losses and converter footprint.

C. Capacitor Voltage Balancing Control

In HCMC, control of AC voltage directly depends on capacitor voltage control. Capacitor voltage can get imbalanced due to several reasons, mainly due to different switching time intervals. For accurate and stable operation SM capacitor voltages must be well balanced [9]. Capacitor voltages vary according to phase current polarity. In this paper, equal voltages across SM capacitors in a phase are obtained by sorting technique. Capacitor voltage balancing is obtained according to following two principles:

- When phase current charges capacitor, SMs with lowest capacitor voltages will be switched on
- When phase current discharges capacitor, SMs with highest capacitor voltages will be switched on

Complete process of capacitor voltage balancing is explained in Fig. 2. Initially, SM capacitor voltages and phase current polarity are sensed.
SMs are sorted in the ascending order of their capacitor voltages. The inserted states (i.e. positively inserted or negatively inserted) of SMs are determined by using sign function,

$$R = n_{on} \text{sgn}(u_w(t))$$  \hspace{1cm} (1)

Where, $u_w$ is voltage of WSC. When $R > 0$, number of positively inserted SMs is $n_{on}$ and when $R < 0$, number of negatively inserted SMs is $n_{on}$. By detecting phase current polarity, switching order of SMs is determined and corresponding SMs are fired. Capacitor voltage balance also takes care of conduction losses.

### IV. DC FAULT BLOCKING CAPABILITY

DC fault protection is a key issue in case of conventional VSC- HVDC transmission system. With conventional VSC, when fault occurs on DC side, IGBTs of converter loses control and converter acts as uncontrolled bridge rectifier, feeding fault current from AC side to DC side. Fortunately, HCMC has ability to block the fault current from AC to DC. This DC fault blocking capability is achieved by preventing gate signals to all IGBTs in converter. Fig. 4 shows the equivalent circuit of HCMC under pole to pole dc fault. Continuous flow of short circuit current through SM capacitors causes its charging and fault current gets reduced to zero.

![Fig. 4. Equivalent circuit diagram of HCMC under pole to pole dc fault](image)

### V. SIMULATION RESULTS

The flexibility of control arithmetic and dc fault blocking capability is verified by using extensive MATLAB simulation. The single line diagram of the test system is given in Fig. 5. The pole to pole dc fault occurs at point ‘F’ on transmission line.
The simulation parameters are given in Table I.

### TABLE I. MAIN CIRCUIT PARAMETERS OF HCMC MODEL

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC bus voltage</td>
<td>200kV</td>
</tr>
<tr>
<td>Grid side AC voltage</td>
<td>400kV</td>
</tr>
<tr>
<td>SM voltage</td>
<td>10kV</td>
</tr>
<tr>
<td>SM capacitor</td>
<td>10mF</td>
</tr>
<tr>
<td>Transformer MVA</td>
<td>250MVA</td>
</tr>
<tr>
<td>Transformer ratio</td>
<td>70kV/400kV</td>
</tr>
<tr>
<td>DC link capacitor</td>
<td>100µF</td>
</tr>
<tr>
<td>Number of SMs per phase</td>
<td>10</td>
</tr>
<tr>
<td>Director switch</td>
<td>5 IGBTs</td>
</tr>
</tbody>
</table>

**A. Verification of Modulation Scheme under Normal Mode**

Under normal mode, DS directs the current either in positive direction or in negative direction. The firing patterns for DS₁ and DS₄ under normal mode are given in Figs. 6 (b) and 6(c). The phase output voltage reference (vₚ) is shown in Fig. 6 (a). When vₚ is greater than zero DS₁ turns on and DS₄ turns off; when vₚ is less than zero DS₄ turns on and DS₁ turns off. The input reference for NLC is given in Fig. 6(d). The reference is obtained after third harmonic injection.

**B. Performance analysis of HCMC under normal mode**

Performance characteristics of HCMC under normal mode of operation are analyzed. Figs. 7 (a) and 7 (b) shows high quality voltage and current waveform at the point of common coupling.
The dynamics of HVDC transmission subjected to step change in active power command are explained. In Fig. 8 shows AC system response to active power step change. Since current control loops are de-coupled, the control of the active and reactive power is independent [10], [11]. Note that during the change in active power command, the converter output voltage is maintained at constant value and the magnitude of current is varied according to the active power supplied by the converter.

![Active and Reactive Power Waveforms](image)

**Fig.8.** Dynamic response of AC system to step change in active power command (a) Three phase output current waveform at PCC (b) Three phase output voltage waveform at PCC

### C. DC Fault Blocking Capability

In order to examine performance of HCMC under dc side fault, system shown in Fig.5 is subjected to pole to pole dc fault. The simulation results are shown in Fig. 9 and 10.

![Fault Blocking Capability](image)

**Fig.9.** Performance characteristics of HCMC (rectifier) under dc to dc fault (a) Three phase output current waveform at PCC (b) Three phase output voltage waveform at PCC (c) Active and reactive power (d) SM capacitor voltages

The dc fault occurs at t=3.5 sec. As soon as the dc fault occurs, gate signals to all IGBTs are prevented. It can be seen from the output current waveforms of Fig 9 (a) and Fig 10 (a), current through WSC reduces to zero very rapidly within few milliseconds after the occurrence of dc fault. There is no effect of blocking of HCMC on three phase output voltage as shown in Fig. 9 (b) and Fig. 10 (b). Under normal mode, P = 500MW and Q = -100 MVAr at rectifier side, and Q = -100 MVAr at inverter side. The blocking feature also prevents power exchange between ac and dc. From Fig. 9 (c) and Fig. 10 (c), it is observed that, the moment fault occurs; active and reactive power gets reduced to zero. SM capacitor voltages remain constant during blocking mode as shown in Fig. 9 (d) and Fig. 10 (d). Therefore, from all the results it can be summarized that by inhibiting gate signals to converter, protection from dc side fault can be achieved. Thus, HCMC is very useful for HVDC transmission where dc faults are prone to occur.
CONCLUSION

This paper examines modulation and control of HCMC along with dc fault blocking capability. Director switches operate almost at fundamental frequency. In order to reduce switching losses, low switching frequency modulation technique, nearest level control is used for switching of WSC. Capacitor voltage balance is maintained by sorting technique and third harmonic injection method. In this approach, first number of SMs to be turn on is calculated by NLC and then SMs are sorted according to their capacitor voltages and phase current polarity. DC fault blocking mechanism is investigated. Effectiveness of modulation and control strategy is verified through extensive MATLAB simulation. It is concluded from the results that in an event of DC side fault, the converter is able to immediately isolate DC and AC side of converter system. Therefore the costly and bulky DC circuit breakers may not be required in an HVDC system.

REFERENCES


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