Abstract—This paper analyses synchronization strategies for cascaded H-Bridge multi level inverter topologies with carrier based sinusoidal phase shifted pulse width modulation technique. In phase shifted pulse width modulation technique, a separate carrier is used for each H-Bridge. The carriers are generally phase shifted from each other by $\pi/n$ Rad ($n=$No. of HBs). Hence, the positions of carriers w.r.t. voltage references play an important role for maintaining 3-$\Phi$, half wave and quarter wave symmetries among multi level inverter pole voltages. This paper analytically shows the conditions for half wave and quarter wave symmetry and experimentally verifies those conditions for phase shifted pulse width modulation technique with a 5 level cascaded H-Bridge multi level inverter laboratory prototype.

Keywords—cascaded H-Bridge multilevel inverter, phase shifted PWM, synchronous carrier, symmetry.

I. INTRODUCTION

With the increasing demand of medium voltage and high power drives, the use of multilevel inverters is gradually becoming more and more important. This is due to reduced voltage stress on semiconductor devices, reduced harmonics in inverter output voltage and lesser electromagnetic interferences. For medium voltage and high power applications the switching frequency and device ratings are limited by the existing semiconductor technology. Increasing the power rating by minimizing switching frequency, while still maintaining reasonable power quality is an important requirement and a persistent challenge. Hence, the use of multilevel inverters become relevant as it suitably distributes the stress among the semi conductor switches. Among the different multilevel inverter (MLI) topologies, the cascaded H-Bridge (CHB) topology is a preferred choice for medium voltage drives for its modularity and this is also the target converter for the proposed PWM technique in this paper.

In high power and medium voltage applications, the power converters are operated at low switching frequency. This is very well defined in the literature as low pulse ratio operation of the converters. The applications consist of traction drives (both VSI and CSI fed drives), grid applications (as bidirectional converters, active power filters) etc. As the pulse ratio is less in these power converters, lower order harmonics including sub-harmonics are introduced in line currents resulting in higher total harmonic distortion (THD). Hence, synchronization among PWM voltages is necessary. Along with synchronization, the PWM voltage should maintain half wave, quarter wave and 3-$\Phi$ symmetries [1]. This is valid for both two and multi level inverters. Reference [2] proposes an optimal PWM scheme for two level inverters to reduce current harmonics with offline calculations of switching pattern. This optimized PWM strategy can also be extended to multi level inverters. Reference [3] shows the application of synchronized optimal PWM technique for a cascaded 9 level inverter. Reference [4] compares the performances of 5 level and 7 level NPC inverters with synchronous optimal PWM technique. But, the synchronized optimal PWM technique is an offline calculation based technique. The switching angles are pre-calculated assuming steady state condition and this requires storage of large data for better accuracy. Reference [5] proposes the model predictive pulse pattern control for a 5 level NPC inverter with optimized PWM technique in order to avoid dynamic problems.

Selective harmonic elimination and selective harmonic mitigation PWM techniques are the other alternatives. Reference [6] shows the application of SHEPWM technique for cascade multi level inverters, whereas [7] shows the use of SHMPWM technique. But they are offline calculation based PWM technique. Hence, along with model predictive control they are used for drive applications.

All the above multi level inverter PWM techniques are offline calculation based technique. The calculation complexity increases with increase in number of voltage levels or increase in the number of commutation angles at lower modulation indexes. Even if the offline calculation complexity is ignored, the real time implementation requires commutation angles to be stored in look-up a table which in turn requires huge memory storage capacity of the controller platform. The carrier based PWM techniques are independent of motor parameters and do not require commutation angles to be stored in look-up tables. Hence, carrier based PWM technique is well suited to multi level inverters although the harmonic content of the inverter output voltage is not optimized. Two carrier based PWM techniques are available in literature for MLIs. They are:- (i) Level shifted PWM technique (LSPWM technique) and (ii) Phase shifted PWM technique (PSPWM technique).
But, the major challenge for carrier based PWM techniques for multi-level inverters is to position the carriers w.r.t. the voltage references so that different symmetries of the pole voltage waveforms can be maintained.

For a two level inverter the carrier should be synchronized with the voltage references i.e. the zero crossings of the carrier should match with the zero crossings of the voltage references and the ratio (p=\(f_c/f_s\)) should be an odd integer (multiple of 3). This condition will maintain 3-\(\Phi\) symmetry, half wave symmetry and quarter wave symmetry of inverter pole voltage waveform. The carrier synchronization with the voltage references is sufficient for the Level Shifted PWM technique for cascaded H-Bridge multilevel inverters (CHBMLIs), as only one synchronous carrier is sufficient for implementation of different voltage levels. Hence, the pole voltage maintains all the basic properties of an ideal synchronous PWM technique. But the power distribution and average device switching frequencies of different HBs are different.

But this scenario is different for Phase Shifted PWM technique, as multiple phase shifted synchronous carriers are used for different H-Bridges. Hence, the positions of the voltage references w.r.t. to the carriers play an important role for maintaining different basic properties of an ideal synchronous PWM, as stated in the previous paragraph. This paper mainly deals with the analytical studies for maintaining symmetry among CHBMLI pole voltage with synchronous sinusoidal PSPWM technique. The carriers used for the analysis in this paper are generated from the instantaneous voltage references, as in [8] and always maintain an odd integer ratio \(p\).

This paper is arranged as follows. Section II deals with the analytical explanation for PSPWM technique to maintain 3-\(\Phi\) symmetry, HWS and QWS among CHBMLI pole voltages. Experimental results are given in section III and the paper is concluded in Section IV.

II. CONDITIONS OF SYMMETRY FOR CHBMLI

A. Verification of 3-\(\Phi\) Symmetry & HWS

![Circuit schematic of a five level cascaded H-Bridge multilevel inverter](image)

Fig. 1. (a) Single H-Bridge (b) Double H-Bridge

Circuit schematic of a five level cascaded H-Bridge multilevel inverter is shown in Fig.1. Unipolar switching strategy is employed for each H-Bridge inverter. With synchronous carriers having 3n times the fundamental frequency (n being an odd integer) being used for the PSPWM technique, 3-\(\Phi\) Symmetry is always maintained among individual HB output pole voltages. Also, from Fig.2 it can be observed that, the region from \(\pi\) rad to \(2\pi\) rad is equivalent to a mirror image of the region from 0 rad to \(\pi\) rad with respect to x-axis. Hence, the intersection points C\(_1\) to C\(_3\) are the mirror images of points from C\(_4\) to C\(_6\) respectively. Hence, the pole voltage pattern in the positive portion of the voltage reference is the exact replica of pole voltage pattern in the negative portion of the voltage reference. Hence, the condition for HWS at points C\(_1\) and C\(_7\) satisfies (1).

\[
\theta_1 = \pi + \theta_k
\]

Similarly, the angle relations at other intersection points can also be stated for HWS. Though, the example is shown for carrier frequency being 3 times the fundamental frequency, the half wave symmetry is satisfied for any carrier having its frequency equal to odd integer multiple of the fundamental frequency. Hence, it can be concluded that the inverter pole voltage maintains 3-\(\Phi\) symmetry for carriers having 3n times the fundamental frequency (n being any integer) and half wave symmetry for carrier having m times the fundamental frequency (m being any odd integer). With carriers having 3n times the fundamental frequency (n being any odd integer), both 3-\(\Phi\) and half wave symmetries are ensured. It is hence only necessary to determine the conditions for QWS in the inverter pole voltage.

B. Determination of conditions for QWS

1) Single H-Bridge

The QWS among pole voltage patterns of an H-Bridge (Fig.1.(a)) can be maintained, if the zero crossings of the voltage references coincide with the zero crossings of the carrier. The carrier can be of two types. They are: - (i) In phase carrier (positive zero crossing of positive voltage reference coincides with the positive zero crossing of the carrier) (ii) Out of phase carrier (positive zero crossing of the positive voltage reference coincides with the negative zero crossing of the carrier). It is also possible to maintain QWS among single HB output pole voltage \(V_{\text{HB1}}\), when the carrier zero crossings do not match with voltage reference zero crossings. The phase relation between the reference and the carrier for QWS of the HB output voltage is analytically derived in the following section.

Fig. 2. shows the zero crossings of carrier C\(_{10}\) having \(p=3\), is \(\Phi\) rad lagging w.r.t. the zero crossings voltage references R\(_1\) and R\(_2\). For maintaining QWS among pole voltage patterns \(V_{\text{HB1}}\), the condition to be satisfied among voltage reference and carrier intersection points C\(_2\) to C\(_6\) is given by (2).

\[
\theta_1 - k = \pi - \theta_k \quad \text{for } k = 1, 2 \text{ and } 3
\]

For \(k=1\), the values of \(\theta_1\) and \(\theta_0\) at points C\(_1\) and C\(_6\) can be found out by equating the equations of voltage references and carrier and can be written as (3) and (4) respectively.

\[
-m \sin \theta_1 = \left( \frac{6}{\pi} \right) (\theta_1 - \phi)
\]
\[ m \sin \theta_b = \left( \frac{6}{\pi} \right) \left( \frac{2\pi}{3} - \phi \right) \]  
(4)

Equation (4) can be modified as (5) by putting the condition of QWS (2).

\[ m \sin \theta_1 = \left( \frac{6}{\pi} \right) \left( \frac{\pi}{3} - \theta_1 - \phi \right) \]  
(5)

By adding (3) and (5), the value of \( \phi \) can be found as (6).

\[ \phi = \frac{\pi}{6} \text{ rad} \]  
(6)

From (6) it can be observed that, the QWS among pole voltage \( V_{HB1} \) can be maintained if the carrier zero crossings are lagging the voltage reference zero crossings by \( \pi/6 \) rad. Equation (6) gives the value of \( \Phi \) in terms of fundamental period of voltage reference. If the value of \( \Phi \) is expressed in terms of carrier period, then \( \Phi \) should be equal to \( \pi/2 \) rad for \( p=3 \). In a similar way the conditions for QWS at other intersection points can also be stated. Similarly, when the carrier zero crossings lead the voltage reference zero crossings by an angle \( \Phi=\pi/2 \) rad, QWS among pole voltage patterns \( V_{HB1} \) in a single HB can be maintained.

Equation (6) shows the condition for QWS among pole voltages \( V_{HB1} \), when \( p=3 \). For carriers having frequency \( p=3n \) (where \( n=1,3,5,7,9,11, \ldots \) etc.) times the fundamental frequency with their zero crossings lagging the fundamental voltage reference zero crossings by \( \Phi \) rad, the condition for QWS among pole voltage patterns \( V_{HB1} \) can be found by using (7)-(11). Here, for QWS, the condition is is given by (7).

\[ \theta_{bn+1-k} = \pi - \theta_k \quad \text{for} \quad k = 1, 2, \ldots, 3n \]  
(7)

For \( k=1 \)

\[ -m \sin \theta_1 = \left( \frac{6n}{\pi} \right) \left( \theta_1 - \phi \right) \]  
(8)

\[ m \sin \theta_{bn} = \left( \frac{6n}{\pi} \right) \left( \theta_{bn} - \phi - \left( \frac{3n-1}{3n} \right) \pi \right) \]  
(9)

By putting the condition of QWS \( \theta_{bn} = \pi - \theta_1 \) in (9), (9) can be simplified as (10).

\[ m \sin \theta_1 = \left( \frac{6n}{\pi} \right) \left( \frac{\pi}{3n} - \theta_1 - \phi \right) \]  
(10)

By adding (8) and (10), the value of \( \phi \) can be found as (11).

\[ \phi = \left( \frac{1}{3n} \right) \left( \frac{\pi}{2} \right) \text{ rad} \]  
(11)

From (11) it can be observed that, QWS among pole voltage patterns \( V_{HB1} \) can be maintained if the zero crossings of \( 3n \) carriers lag the zero crossings of voltage references by \( \Phi=(1/3n)(\pi/2) \) rad. If the value of \( \Phi \) is expressed in terms of carrier period, then \( \Phi \) should be equal to \( \pi/2 \) rad. Similarly, for maintaining QWS among pole voltage patterns \( V_{HB1} \), the value of \( \Phi \) becomes \( \pi/2 \) rad, when the zero crossings of \( 3n \) carriers lead the zero crossings of the voltage references by an angle \( \Phi \) rad.

Hence, the conditions for maintaining QWS among pole voltage patterns \( V_{HB1} \) in a single HB can be summarised as below:-

- The zero crossings of the voltage references should coincide with the zero crossings of the carrier.
- The zero crossings of the carrier should be placed at \( \pm \pi/2 \) rad w.r.t. the zero crossings of the voltage references where \( 2\pi \) rad denotes one carrier period.

2) Double H-Bridge

For two cascaded H-Bridges (Fig.1.(b)), the QWS among individual pole voltages \( V_{HB1} \) and \( V_{HB2} \) can be maintained by using two carriers. They are:-

(i) The zero crossing of the carrier \( C_{HB1} \) in phase with the zero crossings voltage references 
(ii) The zero crossing of carrier \( C_{HB2} \) at \( \pm \pi/2 \) rad w.r.t. the carrier \( C_{HB1} \). The above two conditions maintain QWS among individual pole voltages \( V_{HB1} \) and \( V_{HB2} \) along with resultant pole voltage \( V_{HB} \). It is also possible to maintain QWS of the resultant pole voltage \( V_{HB} \), without maintaining QWS of the individual bridge voltages \( V_{HB1} \) and \( V_{HB2} \). Two possible approaches are possible as shown below. Both the approaches are analytically derived in the coming sections.

- Zero crossings of carriers \( C_{HB1} \) and \( C_{HB2} \) are equidistantly placed on both sides of the carrier \( C_{eff} \) (where \( C_{eff} \) is a fictitious carrier, whose zero crossings are in phase with the zero crossings of the voltage references \( R_1 \) and \( R_2 \)) zero crossings.
Zero crossings of carriers $C_{HB1}$ and $C_{HB2}$ are equidistantly placed on both sides of the carrier $C^{ref}$ (where $C^{ref}$ is a fictitious carrier, whose positive or negative peak are placed at zero crossings of the voltage references $R_1$ and $R_2$) zero crossings.

\[
\theta_{3-k} = \pi - \theta_k \quad \text{for } k=1, 2, 3, 4, 5 \text{ and } 6 
\]

For $k=1$, the values of $\theta_1$ and $\theta_{12}$, at points $C_1$ and $C_{12}$ can be found out by equating the equations of voltage references and carriers and can be written as (13) and (14) respectively.

\[
-m \sin \theta_1 = \left( \frac{6}{\pi} \right) \left( \theta_{1} - \phi_1 \right) \quad (13)
\]

\[
-m \sin \theta_{12} = -\left( \frac{6}{\pi} \right) \left( \theta_{12} - \pi + \phi_2 \right) \quad (14)
\]

Equation (14) can be modified as (15) by putting the condition of QWS (12).

\[
m \sin \theta_1 = \left( \frac{6}{\pi} \right) \left( \phi_2 - \theta_1 \right) 
\]

By adding (13) and (15), the condition for QWS can be found out as (16).

\[
\phi_1 = \phi_2 
\]

From (16) it can be observed that, the QWS among resultant pole voltage patterns $V_{HB}$ can be maintained if $\Phi_1 = -\Phi_2$, i.e. the zero crossings of carriers $C_{HB1}$ and $C_{HB2}$ are placed equidistantly from the zero crossings of carrier $C^{ref}$. In a similar way the conditions for QWS at other intersection points can also be derived and every pair of intersection points will result in the condition of (16). This condition is also valid for carriers having frequency equal to $3n$ times the fundamental frequency.
By adding (18) and (20), the condition for QWS can be found out as (21).

\[ \phi_1 = \phi_2 \]  

(21)

From (21) it can be observed that, the QWS among resultant pole voltage patterns \( V_{HB} \) can be maintained if \( \Phi_1 = \Phi_2 \), i.e. the zero crossing of carriers \( C_{HB1} \) and \( C_{HB2} \) are equidistant from the zero crossings of carrier \( C_{ref} \). The condition of QWS can also be shown as \( \Phi_1 = \Phi_2 \), if the zero crossing of carrier \( C_{ref} \) lead \( \pi/2 \) rad from the zero crossings of the voltage references. This condition is valid for carriers having frequency equal to \( 3n \) times the fundamental frequency.

c) Possible Carrier Positions for Maintaining QWS

For maintaining QWS among resultant pole voltage patterns \( V_{HB} \) in two cascaded H-Bridges, several placements of carrier zero crossings w.r.t. voltage reference zero crossings are possible. For two cascaded H-Bridges, the harmonic profile of resultant pole voltage \( V_{HB} \) is better when the carrier zero crossings are placed at \( \pi/2 \) rad apart from each other. Hence, for maintaining QWS, only those carriers are considered whose zero crossings are placed \( \pi/2 \) rad apart.

<table>
<thead>
<tr>
<th>Case</th>
<th>Position of ( C_{HB1} )</th>
<th>Position of ( C_{HB2} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0 rad</td>
<td>( \pm \pi/2 ) rad</td>
</tr>
<tr>
<td>2</td>
<td>( \pm \pi/4 ) rad</td>
<td>( \pm \pi/4 ) rad</td>
</tr>
<tr>
<td>3</td>
<td>( \pm \pi/4 ) rad</td>
<td>( \pm 3\pi/4 ) rad</td>
</tr>
</tbody>
</table>

Table-I shows the various possible placements of zero crossings of carriers \( C_{HB1} \) and \( C_{HB2} \) w.r.t. the zero crossings of voltage references for maintaining QWS among resultant pole voltage \( V_{HB} \) in two cascaded H-Bridges. Hence, the conditions for maintaining QWS among resultant pole voltage patterns \( V_{HB} \) in two cascaded H-Bridges, where two carriers are placed \( \pi/2 \) rad apart, can be summarised as below:-

- The zero crossings of the voltage references should coincide with the zero crossings of any carrier.
- The zero crossings of the voltage references should be placed exactly at the mid-point of the carriers zero crossings.

<table>
<thead>
<tr>
<th>Case</th>
<th>Position of ( C_{HB1} )</th>
<th>Position of ( C_{HB2} )</th>
<th>Position of ( C_{HB3} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( \pm \pi/3 ) rad</td>
<td>0 rad</td>
<td>( \pm \pi/3 ) rad</td>
</tr>
<tr>
<td>2</td>
<td>( \pm \pi/6 ) rad</td>
<td>( \pm \pi/6 ) rad</td>
<td>( \pm \pi/2 ) rad</td>
</tr>
<tr>
<td>3</td>
<td>( \pm \pi/6 ) rad</td>
<td>( \pm \pi/2 ) rad</td>
<td>( \pm 5\pi/6 ) rad</td>
</tr>
<tr>
<td>4</td>
<td>0 rad</td>
<td>( \pm \pi/3 ) rad</td>
<td>( \pm 2\pi/3 ) rad</td>
</tr>
</tbody>
</table>

Similarly, for three cascaded H-Bridges the conditions for maintaining QWS among pole voltages are tabulated in Table-II. Hence, in general the QWS in three cascaded H-Bridges can be maintained if the following conditions are valid.

- Any of the carriers is synchronized with the voltage references.
- The voltage references are placed at the mid-point between any two adjacent carriers.

d) Generalized Condition for maintaining QWS

Table-III summarizes the conditions to maintain QWS. It is observed that if these conditions are maintained then leaving out the in-phase and \( \pi/2 \)-phase carriers (if they exist), equal number of carriers will be placed on both sides of \( C_{ref} \) (as shown in Fig. 3) or \( C_{ref}^{12} \) (as shown in Fig. 4) or both.

<table>
<thead>
<tr>
<th>CONDITION FOR QWS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
</tr>
<tr>
<td>Voltage references in phase with any carrier</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>Voltage references are placed at the mid-point between any two adjacent carrier pairs</td>
</tr>
</tbody>
</table>

III. EXPERIMENTAL RESULTS

Fig. 5. (a) Ch.1:-\( C_{HB1} \), Ch.2:-\( C_{HB2} \), Ch.3:-\( R_1 \) and Ch.4:-\( R_2 \) (c) Ch.1:-\( V_{HB1} \), Ch.2:-\( V_{HB2} \) and Ch.3:-\( V_{in} \) and (e) Ch.1:-\( V_{HB1} \), Ch.2:-\( V_{HB2} \) and Ch.3:-\( V_{in} \) when the zero crossings of voltage references are placed at \( \pm \pi/4 \) rad w.r.t. the zero crossings of carriers \( C_{HB1} \) & \( C_{HB2} \) and (b) Ch.1:-\( C_{HB1} \), Ch.2:-\( C_{HB2} \), Ch.3:-\( R_1 \) and Ch.4:-\( R_2 \) (d) Ch.1:-\( V_{HB1} \), Ch.2:-\( V_{HB2} \) and Ch.3:-\( V_{in} \) and (f) Ch.1:-\( V_{HB1} \), Ch.2:-\( V_{HB2} \) and Ch.3:-\( V_{in} \) when the zero crossings of voltage references are in phase with the zero crossings of carrier \( C_{HB3} \) for \( p=3 \) with a modulation index of 0.8 and \( f=50Hz \).

The synchronization strategy for the CHBMLIs is verified with a squirrel cage induction motor drive operated in open loop V/f mode, which is supplied from a 5 level 3-phase CHBMLI laboratory prototype. As discussed in Section II, both the conditions for maintaining QWS among resultant pole voltage patterns \( V_{HB} \) are tested experimentally. For experimental
verification the ratio p is kept at 3. Fig.5.(a) shows the zero crossings of carriers C_{HB1} and C_{HB2} are placed at ±π/4 rad w.r.t. the zero crossings of voltage references R_1 and R_2. Fig.5.(c) shows the individual bridge voltages V_{HB1} and V_{HB2} maintain HWS except QWS. But the resultant pole voltage V_{HB} maintains HWS and QWS. Fig.5.(b) shows that the zero crossings of voltage references R_1 and R_2 are in phase with the zero crossings of carrier C_{HB2}. Fig.5.(d) shows the individual bridge voltages V_{HB1} and V_{HB2} and resultant pole voltage V_{HB}. It can be observed that the individual bridge voltages along with resultant pole voltage maintain HWS and QWS. Fig.5.(e) and (f) show the 3-Φ symmetry among 3-Φ pole voltages.

Fig.6 also shows the results for maintaining QWS for a double HB with p=9. Hence, the conditions tabulated in Table-I are valid for any 3n carriers. Fig.7.(a) and (b) show the R & Y-phase pole voltages along with the line (motor phase) currents for a modulation index of 0.9 for a 3-Φ 5 level CHBMLI with (a) p=3, f=45Hz (b) p=9, f=55Hz when the zero crossings of voltage references are placed at ±π/4 rad w.r.t. the zero crossings of the carriers.

Fig.6. (a) Ch.1:C_{HB1},Ch.2:C_{HB2} and Ch.3:-R_1 (c) Ch.2:-V_{HB1}, Ch.3:-V_{HB2} and Ch.4:-V_{HB} when the zero crossings of voltage references are placed at ±π/4 rad w.r.t. the zero crossings of carriers C_{HB1} & C_{HB2} and (b) Ch.1:-C_{HB1},Ch.2:-C_{HB2} and Ch.3:-R_1  (d) Ch.2:-V_{HB1},Ch.3:-V_{HB2} and Ch.4:-V_{HB} when the zero crossings of voltage references are in phase with the zero crossings of carrier C_{HB1} for p=9 with a modulation index of 0.9 and f=45Hz.

IV. Conclusion
This paper analytically shows the possible positions of zero crossings of the carriers with respect to the zero crossings of voltage references for the cascaded H-Bridge multilevel inverters using phase shifted pulse width modulation technique for maintaining 3-Φ symmetry, half wave symmetry and quarter wave symmetry. 3-Φ and half wave symmetries are maintained among H-Bridge pole voltages for any position of zero crossing of carrier w.r.t. the zero crossing of the voltage references, as synchronous carriers having frequency 3n(where n=1,3,5,7,9,11,……etc.) times the fundamental frequency are used for any H-Bridge. But the positions of zero crossings of the carriers w.r.t. to the zero crossings of voltage references are important for maintaining QWS among pole voltages. This is analytically studied in this paper for single and two cascaded H-Bridges and generalized for any number of H-Bridges. The study is experimentally verified with the help of a 3-Φ 5 level cascaded H-Bridge multilevel inverter laboratory prototype and the results are presented.

References