Performance Analysis of a 1200 V SiC MOSFET Based 10 kVA Voltage Source Inverter

Parthasarathy Nayak\textsuperscript{1}, Jose Titus\textsuperscript{2}, Kamalesh Hatua\textsuperscript{3}
Department of Electrical Engineering
Indian Institute of Technology Madras
Chennai - 600036, India
Email: \textsuperscript{1}parthasarathy.nayak.2015@ieee.org, \textsuperscript{2}josenit1787@gmail.com, \textsuperscript{3}kamalesh@ee.iitm.ac.in

\textbf{Abstract}—Silicon carbide (SiC) MOSFET has the potential to replace silicon (Si) IGBT due to its superior switching performance. However due to presence of parasitic inductance in converter layout, device voltage and current experience overshoots and oscillations during device switching. These undesired overshoots increase switching loss. In the context of these parasitic inductances, the performance of an equivalent Si IGBT and SiC MOSFET based 10 kVA converter has been compared in this paper. Variation of switching loss with switching frequency at different parasitic inductances have been reported. A 10 kVA SiC MOSFET based voltage source inverter has been designed and its performance has been analyzed by driving an induction motor.

\textbf{Index Terms}—SiC MOSFET, parasitic inductance, switching characteristics, switching loss.

\textbf{I. INTRODUCTION}

SiC MOSFET has been the center of attraction since it’s commercial availability in 2011. It is mostly due to it’s superior properties like higher breakdown field strength, improved thermal stability, superior switching performance, low on state resistance [1]-[3]. These superior properties allow the device to be switched beyond 20 kHz while maintaining efficiency above 99 \% for a hard switched converter. Also due to high switching frequency of operation, the size of passive filters can be greatly reduced.

Due to the superior switching characteristics, the $di/dt$ and $dv/dt$ of the SiC MOSFET is more than twice that of equivalent IGBTs. With such a high voltage and current slew rate, the device voltage and current experience undesired overshoot and oscillations due to the presence of parasitic inductance in converter layout and device packaging during switching transients [4]-[7]. These overshoots and oscillations increase switching loss, degrades EMI performance of the converter and generates voltage and current stress in the device.

These are the issues pop up while designing a SiC MOSFET based hard switched converter. These issues are not that detrimental for Si IGBT based converters as they switch slower. Two of the solutions to these issues are to either reduce parasitic inductances or to slow down the switching of the devices by increasing the gate resistance. Whereas there is a limitation for first solution, due to mechanical design constraint and the second solution fails to extract maximum benefit from SiC MOSFET. There have been analysis on performance of SiC MOSFET based converter, where authors have slowed down the device by increasing the gate resistance [8]-[10]. Though it still provides better results than Si IGBT based converters but fails to optimize the potential benefit of SiC MOSFET. This paper reports the performance analysis of a 10 kVA converter by keeping minimum gate resistance but the leakage inductances have been restricted by critical design of converter layout. It also emphasizes on the gate driver design for SiC MOSFETs and it’s performance in the context of common mode current injection. The developed converter has been tested by driving an induction motor. The performance of the inverter at various switching frequency has been included in this paper along with the effects of high speed switching on motor terminal voltage.

Section II of this paper draws a comparison between performance of a 10 kVA SiC MOSFET and Si IGBT based converter. The change in performance of SiC MOSFET based inverter under
the influence of parasitic inductance is reported in Section III. All detrimental effects of parasitic inductance are summarized in Section IV. Section V explains the gate driver and converter layout designs. Performance of a 10 kVA SiC MOSFET with an induction motor has been elaborated in Section VI. Section VII concludes the paper.

II. PERFORMANCE COMPARISON BETWEEN SiC MOSFET AND Si IGBT BASED 10 kVA HARD SWITCHED VOLTAGE SOURCE INVERTER

This section carries out a comparison between performance of an equivalent SiC MOSFET and Si IGBT based 10 kVA, hard switched two level voltage source inverter. The SiC MOSFET (SCH2080KE) under study is ROHM make 1200 V, 35 A device and Si IGBT (IXDH20N120D1) is of IXYS make 1200 V, 38 A device. This study has been carried out on a 3-phase inverter, feeding a R-L load at 0.8 power factor at different switching frequencies of operation. The typical turn on and turn off period of selected SiC MOSFET is 70 nsec and 98 nsec respectively. Whereas for IGBT under study has turn on period of 175 nsec and turn off period of 570 nsec. Due to high switching duration, IGBT exhibits more switching loss compared to SiC MOSFET. The on state resistance ($R_{DS(on)}$) of SiC MOSFET under comparison is 80 mΩ. The on state voltage $V_{CE(sat)}$ of IGBT is typically 2.4 V. This high on state voltage for IGBT increases conduction loss, reducing overall efficiency of the system. The switching loss and percentage efficiency of two converters have been plotted in Fig. 1 and Fig. 2 respectively. As depicted in Fig. 1 the switching loss of SiC MOSFET based 10 kVA converter is 10 W at switching frequency of 5 kHz and 20 W at 20 kHz of switching frequency. On the contrary Si IGBT based converter exhibits loss up to 100 W at 5 kHz and 280 W at 20 kHz of switching frequency. Due to this lower switching loss the SiC MOSFET based converter exhibits an efficiency of 99.4 % and 98.6 % at switching frequencies of 5 kHz and 20 kHz respectively. In both the cases conduction loss of the converter is 40 W. Whereas at 20 kHz switching frequency, Si IGBT based converter exhibits efficiency of 88 % (Fig. 2). This lower switching loss is an advantage of SiC MOSFET. But in real practice it is challenging to achieve such a high efficiency. This is primarily due to the presence of parasitic inductances in the converter layout. These parasitic inductances increase voltage overshoot and switching loss.
The above stated switching loss figures are obtained through LTSpice simulation at different parasitic inductances with different load current level. These information have been tabulated in a lookup table in MATLAB. From the lookup table data, the total switching and conduction loss have been calculated for a 10 kVA converter.

III. PERFORMANCE OF SiC MOSFET UNDER THE INFLUENCE OF PARASITIC INDUCTANCES

During switching transients device current and voltage experience overshoot and oscillation due to the presence of parasitic inductance \((L_p)\) in converter layout. The oscillation occurs because of L-C network formed between parasitic inductances and device output capacitance \((C_{oss})\). These overshoots in device voltage and current increase switching loss. It degrades the efficiency of the converter. Fig. 3 shows the increase in switching loss due to increase in parasitic inductances \((L_p)\). Corresponding reduction in percentage of efficiency is depicted in Fig. 4. It can be noticed that for a \(L_p\) of 500 nH, switching loss increases to 1500 W at switching frequency of 50 kHz. It results an efficiency of 84 %. Interestingly for this range of parasitic inductance, IGBT based converter does not show greater reduction in efficiency. It is because of comparatively lower voltage overshoot considering the slow \(di/dt\) of IGBT. Therefore in order to achieve high efficiency for SiC MOSFET based converter, a special attention must be given to the effects of parasitic inductances in the layout.

IV. EFFECTS OF PARASITIC INDUCTANCES ON SWITCHING PERFORMANCES OF SiC MOSFET

The adverse effects of parasitic inductances present in converter layout for SiC MOSFET are manifold. Some of them are described below.

- Parasitic inductance in the layout causes overshoot in device current and gate voltage during turn on transient. It happens due to oscillation between \(L_p\) and the equivalent capacitance formed by the parasitic capacitance of load inductor and the reverse biased capacitance of antiparallel diode. The overshoot in gate voltage can damage the gate terminal of the device if it crosses the maximum gate to source voltage rating of the device. It can be observed in Fig. 6. For an \(L_p\) of 150 nH device current and gate voltage overshoot by 30 % and 20 % respectively. The overshoot in device current generates stress in the device and increases turn on loss.

<table>
<thead>
<tr>
<th>(L_p)</th>
<th>Overshoot of (V_{ds})</th>
<th>(E_{total})</th>
</tr>
</thead>
<tbody>
<tr>
<td>50nH</td>
<td>5 %</td>
<td>0.9 mJ</td>
</tr>
<tr>
<td>100nH</td>
<td>20 %</td>
<td>1.0 mJ</td>
</tr>
<tr>
<td>200nH</td>
<td>50 %</td>
<td>1.2 mJ</td>
</tr>
<tr>
<td>300nH</td>
<td>55 %</td>
<td>1.7 mJ</td>
</tr>
<tr>
<td>500nH</td>
<td>68 %</td>
<td>2.0 mJ</td>
</tr>
<tr>
<td>650nH</td>
<td>76 %</td>
<td>2.5 mJ</td>
</tr>
</tbody>
</table>

Fig. 5. Overshoot in device voltage, \(V_{ds}\) at \(L_p\) of 200 nH. Scale: \(V_{ds}\) = 150 V/div, Time = 290 ns/div.

Fig. 6. Overshoot in gate voltage, \(V_{gs}\) and device current \(I_d\) at \(L_p\) of 150 nH. Scale: \(V_{gs}\) = 10 V/div, \(I_d\) = 10 A/div, Time = 100 ns/div.
• SiC MOSFET injects comparatively more common mode noises into the system due to high \( \frac{di}{dt} \) and \( \frac{dv}{dt} \). It happens because of miller current injection \( (C\frac{dv}{dt}) \) and voltage developed across DC bus return parasitic inductances \( (L_{dcr}\frac{di}{dt}) \) during switching transients. The common mode current flows into the system through different coupling capacitances. For example, the common mode (CM) current injected into the control unit passes through the coupling capacitances of isolated power supply for gate driver. These noises enter into the power unit through parasitic capacitances formed between device surface and heat sink. These injected noises degrade EMI performance of the converter.

V. 10 kVA SiC MOSFET Based Voltage Source Inverter Design

A. Gate Driver Design

An hard switched gate driver has been developed for switching the devices. The top and bottom view of the gate driver is depicted in Fig. 7 and Fig. 8 respectively. The gate driver is designed with a four layer printed circuit board (PCB) to minimize ground noises. It is stated in the Section IV that due to high \( \frac{di}{dt} \) and \( \frac{dv}{dt} \) common mode (CM) noises are injected into the system. These noises are injected into the control circuit through the coupling capacitance of isolated power supply. Therefore in order to arrest these noises, an isolated power supply has been designed with minimum coupling capacitance (< 5 pF). The isolated power supply is shown in Fig. 9. It has one primary winding wound for 15 V supply and two secondary windings for 20 V and -5 V power supply. An additional common mode choke is provided in the non isolated side of the gate driver to restrict the injected common mode current at the gate driver terminal. The gate driver’s response for restriction of injected common mode current can be observed in Fig. 10. It depicts the CM current injected during turn on and turn off instant.

B. Converter Layout Design

Converter layout design plays a critical role for SiC MOSFET. The parasitic inductance should be kept as low as possible to minimize its detrimental effects. In order to reduce leakage inductances,
the developed layout follows sandwiched bus bar configuration to reduce current loop lengths. The DC bus has been sandwiched on a printed circuit board (PCB). As a result the leakage inductance in each leg is reduced to less than 80 nH. The copper thickness is maintained at 8 mil. It has been designed to carry a load current of 20 A. The PCB is made up of FR4 material of 3.2 mm thickness. The top view of the converter layout can be seen from Fig. 11. In order to nullify the effects of leakage inductances, four metalized polypropylene capacitors of 20 \( \mu \)F each have been connected across the DC bus along with two 2200 \( \mu \)F electrolytic capacitors.

VI. PERFORMANCE ANALYSIS OF THE DEVELOPED 10 kVA SiC MOSFET BASED VSI

The developed SiC MOSFET based converter has been tested by driving an induction motor as a load. The machine parameters are given in Appendix A. The induction machine is operated by v/f control. The developed converter is depicted in Fig. 12. The DC bus has been maintained at 500 V. Due to reduction of parasitic inductances the voltage overshoot at the device terminal is reduced to 17 %. As a result the switching loss is 22 W and efficiency of the converter is 98.5 % at 20 kHz switching frequency. Fig. 13 shows the response of the converter at 20 kHz of switching frequency. Even though the voltage overshoot has been restricted largely, motor terminal voltage experiences a very high voltage overshoot and low frequency oscillations as delineated in Fig. 14 and Fig. 15. It can be observed that the phase voltage overshoots twice the DC bus voltage. It occurs due to cable leakage inductances and parasitic capacitances. In this case the length of the copper cable from converter terminal to motor terminal is 2 meter.

VII. CONCLUSION

SiC MOSFET is a viable alternative for Si IGBT due to its attractive switching characteristics. But the converter performance degrades with the presence of parasitic inductances in the layout. In this paper, a comparison study on SiC MOSFET and Si IGBT based converter has been carried out.
under the influence of parasitic inductance. The detrimental effects of parasitic inductance have been summarized. The gate driver and converter layout design has been explained along with its performances. The developed converter is tested with an induction motor. The response of the converter has been elaborated. The efficiency of the developed converter is found to be 98.5% at switching frequency of 20 kHz.

APPENDIX A

TABLE II
KEY PARAMETERS OF THE INDUCTION MOTOR

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power rating ($P_{rated}$)</td>
<td>30 kW</td>
</tr>
<tr>
<td>Voltage rating ($V_{rated}$)</td>
<td>380 V</td>
</tr>
<tr>
<td>Stator resistance ($R_s$)</td>
<td>0.12727 Ω</td>
</tr>
<tr>
<td>Rotor resistance ($R_r$)</td>
<td>0.12727 Ω</td>
</tr>
<tr>
<td>Stator leakage inductance ($L_{ls}$)</td>
<td>0.001341 H</td>
</tr>
<tr>
<td>Rotor leakage inductance ($L_{lr}$)</td>
<td>0.001341 H</td>
</tr>
<tr>
<td>Mutual inductance ($L_{m}$)</td>
<td>0.045219 H</td>
</tr>
<tr>
<td>Rotor inertia ($J$)</td>
<td>0.8 Kg m²</td>
</tr>
<tr>
<td>Number of poles ($P$)</td>
<td>4</td>
</tr>
<tr>
<td>Rotor speed ($N$)</td>
<td>1450 rpm</td>
</tr>
</tbody>
</table>

REFERENCES


