Virtual resistance based control for Ultracapacitor based Bidirectional dc/dc Backup System

K. Saichand and Vinod John
Department of Electrical Engineering
Indian Institute of Science, Bengaluru

Abstract—This paper presents the control of a Ultracapacitor based dc/dc power-supply which provides energy backup to critical loads either during momentary power main failures or during peak power demands. The conventional control techniques such as unified control strategy although ensures seamless mode transition, does not offer complete flexibility in charging and discharging controls, which is required for any ride through power supply. On the other hand, other important controls such as independent switch control though allows great flexibility in control, will not ensure seamless mode transition without appropriate mode-switch logic. This paper proposes a virtual resistance based mode switch logic for independent switch control which not only ensures smooth, seamless transition between charging and discharging control modes but also ensures complete decoupling in closed loop control structures. The proposed mode switch logic is verified using simulation results and the proposed control is found to work well.

Index Terms—Bidirectional converter, Unified control strategy, Switch control strategy, Mode identification, Ultracapacitors, Mode switch logic, Virtual resistance.

I. INTRODUCTION

Ultracapacitor based bidirectional dc/dc converters are widely used in hybrid electric vehicles [1], traction and transport systems [2], power-quality [3] and in micro-grids [4] for ride through provision. The control of such a bidirectional converter considered in Fig. 1 based on seamless transition between charging and discharging dynamics can be broadly classified into 1) Unified control strategy and 2) Independent Switch control method.

The unified control strategy as shown in Fig. 1(b) as the name indicates, utilizes a single controller which controls both charging and discharging dynamics. Unified control strategy utilizes the idea that both charging and discharging controls has similar inductor current to duty ratio transfer functions \( \frac{i_L(s)}{d(s)} \) [5]. Although unified control achieves seamless transition between charging and discharging control modes, an important limitation in using this control is that while discharging control uses two loop control, charging control is restricted to use a single loop control. Unified control strategy is widely used in control of battery based applications such as in [5], [6].

From ultracapacitor (UC) based ride through point of view, charging time of the UC stack is quite critical. Hence, Constant Voltage (CV) and Constant Power (CP) charging control not only ensures lesser charging time but also smoother charging profile as compared to Constant Current (CC) control [7], [8].

Since, CV/CP charging needs different outer voltage loop as compared to discharging sub-system, the control structures of charging and discharging are no longer similar. On the other hand, independent switch control strategy as shown in Fig. 1(c) allows different charging and discharging controllers but needs accurate mode switch logic.

Independent switch control although allows different control loops for both charging and discharging sub-systems need accurate mode identification and seamless mode transition with proper mode switch logic. Although references such as [9] attempts to use independent switch control, due to the use of fixed transition times, seamless transition between two control sub-systems is not achieved. Reference [10] uses PWM blocking as a mode switch logic for seamless mode transition in independent switch control. This paper proposes a alternate mode switch logic based on virtual resistance which not only ensures smooth, seamless mode transition but also allows adjustable control over mode transition time by varying the virtual resistance during control mode transition.

II. POWER CIRCUIT AND CONTROLLER DESIGN

The ultracapacitor based ride through system for the critical load consisting of UC stack interfaced through dc/dc converter to the dc power supply is as shown in Fig. 1. The converter acts as a buck converter during the charging of the UC stack and as a boost converter during the discharging mode. The operating
conditions of the experimental set-up is as shown in Table I. The closed loop controller design of the bidirectional converter can be categorized as control design for charging operation and discharging operation. The overall control structure for the bidirectional operation is as shown in Fig. 2 [10].

![Control block diagram](image)

Fig. 2: Control block diagram for (a) Charging mode, and (b) Discharging mode.

### Table I: Hardware and Control parameters for UC based bidirectional dc/dc converter

<table>
<thead>
<tr>
<th>Hardware details</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filter inductor, (L)</td>
<td>300 (\mu)H</td>
</tr>
<tr>
<td>Filter capacitor, (C_f)</td>
<td>2000 (\mu)F</td>
</tr>
<tr>
<td>UC stack capacitance (C_{uc}), ESR (R_{uc})</td>
<td>12.5 (F), 0.2 (\Omega)</td>
</tr>
<tr>
<td>(P_{rated}) : Supply Voltage (V_g), UC voltage (V_{uc}), (f_{sw})</td>
<td>100(W), 20(V), 19(V), 100(kHz)</td>
</tr>
</tbody>
</table>

### Charging and Discharging modes’ inner current loop parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proportional gain, (K_{ic})</td>
<td>10 (\Omega^{-1})</td>
</tr>
<tr>
<td>Integral gain, (K_{id})</td>
<td>700 (\Omega^{-1}s^{-1})</td>
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\(1\) UC stack consists of 12 Maxwell BCAP0150 ultracapacitors in series

1) Controller for charging mode of operation: The plant and controller transfer function of inner current loop and outer voltage loop is as shown in (1) and (2) respectively. The design bandwidth of the current and voltage loops are 1\(kHz\) and 100\(Hz\) respectively. Neglecting the effect of ESR of the UC stack, the outer voltage loop control \(H_{vc}(s)\) needs only proportional controller since the voltage loop plant transfer function already has a pole at the origin (\(s=0\)). The charging controller design is based on [10].

\[
\frac{i_{L}(s)}{d(s)} = \frac{sV_gC_{uc}}{L C_{uc} s^2 + R_{uc} C_{uc} s + 1}, \quad H_{ic}(s) = K_{ic}(1 + sT_{ic}) \frac{1}{sT_{ic}}
\]

(1)

\[
\frac{V_{uc}(s)}{i_{L}(s)} = \frac{1}{C_{uc} s + R_{uc}} \approx \frac{1}{C_{uc} s}, \quad H_{vc}(s) = K_{vc}
\]

(2)

2) Controller for discharging mode of operation: Since the unified control utilizes the common current control transfer function for both charging and discharging modes, the inner current loop design of discharging mode is similar to charging mode control around gain cross over frequency with the only difference that the boost mode controller design is performed for various UC voltage and load conditions. The corresponding control bandwidth of the inner current loop is chosen to be around 1\(kHz\). The plant and controller transfer functions of inner current loop is derived as shown in (3) and (4) based on [11].

\[
\frac{i_{L}(s)}{d(s)} = \frac{V_{uc}}{R_L(1 - d)^3} \frac{2 + sC_f R_L}{1 + s \frac{L}{R_L (1 - d) \pi} + s^2 \frac{LC_f}{(1 - d)^2}}
\]

(3)

\[
H_{id}(s) = \frac{K_{id}(1 + sT_{id})}{sT_{id}}
\]

(4)

The outer voltage loop control has a different plant structure as compared to that of charging mode control structure. The plant transfer function and controller transfer function of outer voltage loop is as shown in (5) which is obtained based on [11].

\[
\frac{V_{o}(s)}{i_{L}(s)} = \frac{R_L(1 - d)(1 - s \frac{L}{R_L(1 - d) \pi})}{2 + sC_f R_L}
\]

(5)

\[
\frac{1}{H_{vo}(s)} = \frac{K_{vo} + \frac{K_{vo}}{s}}{2V_o}
\]

(6)

The controller design is based on the plant characterization in the charging and discharging modes. However, the transient performance during mode transition is dependent on the mode identification logic based on virtual resistance.

### III. Virtual resistance based mode switch logic using mode identification algorithm

One of the major challenges of the switch control methods is accurate mode identification where reference [10] uses mode identification algorithm based on PWM blocking. This section explains the proposed mode switch logic based on virtual resistance unlike the PWM block method and hence ensures complete control over mode transition times.

A. Mode identification algorithm using virtual resistance

The mode identification algorithm using virtual resistance ensures that the converter operates in charging mode when the \(V_g\) supply is available or in discharging mode when the \(V_g\) supply is unavailable. The boundaries for current and voltages shown in Fig. 3 are for representative purposes and is not drawn to scale. The mode identification parameters chosen are inductor current \(i_L\) and output voltage \(V_o\).
1) During ultracapacitor charging and discharging \((0 < t < t_1)\) and \((t_2 < t < t_3)\): During charging and discharging modes, the corresponding closed loop controls function based on mode identification algorithm. In order to make sensing of \(i_L\) and \(V_o\) more robust, voltage and current hysteresis is utilized which prevents error mode identification which is as shown in Fig. 3. The mode identification algorithm also accommodates starting condition to ensure smooth starting process. The sub-states for charging and discharging in FSM model as shown in Fig. 3(b) are S1' and S2" respectively. The corresponding conditions for charging and discharging modes in the mode identification algorithm is represented as edges \(E_{11}, E_{21}\) and \(E_{22}, E_{12}\) in Fig. 3(b) respectively.

2) During ultracapacitor charging-discharging transition \((t_1 < t < t_2)\): During the charging-discharging transition, the system continues to work in charging mode which can be seen in Fig. 3(b) as sub-state S1", but with reducing voltage loop reference \(V_{uc}\) as shown in Fig. 4. \(V_{uc}([k+1]/T_s)\) for any given discrete time interval, \(kT_s\) can be calculated using (7) and (8) respectively.

\[
V_{uc}([k+1]/T_s) = V_{uc}(kT_s) + i_L(t_1)R_v(kT_s) \quad (7)
\]

\[
R_v([k+1]/T_s) = R_v(kT_s) + \Delta r \quad (8)
\]

The corresponding condition for charging-discharging transition in the mode identification algorithm is represented as edge \(E_{11}\) in Fig. 3(b). Here, \(R_v(kT_s)\) is the virtual resistance which is increased by a factor of \(\Delta r\) with every sampling interval. \(T_s\) is the sampling time of the system. \(i_L(t_1)\) is the inductor current \(i_L\) sampled at the beginning of the charging-discharging transition, i.e. at \(t=t_1\) in the digital controller. It should be noted that during charging and charging-discharging durations, by adopted sign convention \(i_L\) is negative. Since, \(V_{uc}([k+1]/T_s)\) is reducing with each sample and outer voltage loop of charging control only has P-controller \(K_{uc}\), the inner current loop reference \(i_{ref}\) reduces gradually. During this period, the \(V_{uc}\) value is nearly constant, owing to the large value of UC stack capacitance \(C_2\). This causes the inductor current \(i_L\) to reduce accordingly. This continues till \(i_L\) is zero after which discharging closed loop control takes over.

3) During ultracapacitor discharging-charging transition \((t_3 < t < t_4)\): During the discharging-charging transition, the system continues to work in discharging mode but with reducing voltage loop reference \(V_{o}^*\) as shown in Fig. 5. \(V_{o}^*([k+1]/T_s)\) for any given discrete time interval \(kT_s\) is given by (9) and (10) respectively.

\[
V_{o}^*([k+1]/T_s) = V_{o}^*(kT_s) - i_L(t_3)R_v(kT_s) \quad (9)
\]

\[
R_v([k+1]/T_s) = R_v(kT_s) + \Delta r \quad (10)
\]

\(i_L(t_3)\) is sampled in the beginning of discharging-charging period in the similar fashion as \(i_L(t_1)\). During the mode transition periods, \(i_L(t_1)\) and \(i_L(t_3)\) are fixed quantities. Similar to charging-discharging transition, due to reducing value of \(V_{o}^*([k+1]/T_s)\) and with main power supply \(V_g\) restored where \(V_g>V_o\) (from Fig. 3(a)), the inner current loop reference \(i_{ref}\) reduces due to negative voltage loop error. This causes inductor current \(i_L\) to reduce with time. This continues till \(i_L\)
is zero after which charging closed loop control takes over. Since the system continues to function in the discharging control, this duration is represented by S2’ sub-state in the FSM model shown in Fig. 3(b). The corresponding condition for discharging-charging transition in the mode identification algorithm is represented as edge $E_{22}$ in Fig. 3(b). The expected $i_L$ and $V_o$ waveforms using the virtual resistance control for both the mode transitions is as shown in Fig. 3(a).

![Fig. 5: Variable resistance control during discharging-charging transition.](image)

The mode identification algorithm provided here ensures smooth, seamless transition between control modes. Sufficient margin between the mode identification conditions is provided to prevent error mode identification. Table. II summarizes the role of virtual resistance control and $i_L$, $V_o$ conditions for control mode identification. The proposed separate switch control is verified using simulation results.

**TABLE II: Logic conditions for mode identification.**

<table>
<thead>
<tr>
<th>FSM edges</th>
<th>Time durations</th>
<th>$i_L$</th>
<th>$V_o$</th>
<th>Mode</th>
<th>Virtual resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{11}$, $E_{21}$</td>
<td>$0&lt;t&lt;t_1$</td>
<td>$i_L&lt;i_{th}$</td>
<td>$V_o&gt;V_b+\Delta V$</td>
<td>Charging mode</td>
<td>No</td>
</tr>
<tr>
<td>$E_{11}$</td>
<td>$t_1&lt;t&lt;t_2$</td>
<td>$i_L&lt;-i_{th}$</td>
<td>$V_o&lt;V_b-\Delta V$</td>
<td>Charging-Discharging tr.</td>
<td>Yes</td>
</tr>
<tr>
<td>$E_{22}$, $E_{12}$</td>
<td>$t_2&lt;t&lt;t_3$</td>
<td>$i_L&gt;-i_{th}$</td>
<td>$V_o&lt;V_b-\Delta V$</td>
<td>Discharging mode</td>
<td>No</td>
</tr>
<tr>
<td>$E_{22}$</td>
<td>$t_3&lt;t&lt;t_4$</td>
<td>$i_L&gt;i_{th}$</td>
<td>$V_o&gt;V_b+\Delta V$</td>
<td>Discharging-Charging tr.</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**IV. Simulation Studies**

The simulation and experimental results shown in the next two sections are based on Table. I. The inductor current $i_L$ along with the corresponding charging and discharging current references is as shown in Fig. 6(a). It can be seen that the mode transitions are quite smooth without any huge inductor current transients. It can be observed from Fig. 6(b), that the output voltage $V_o$ is tightly regulated at 24V through out the back-up period. Fig. 6(c) shows the UC stack voltage during charging-discharging-charging period where a sharp change in $V_{uc}$ is observed during the transition times which is due to the ESR of the UC stack.

**A. During charging-discharging transition**

The simulation results during charging-discharging transition is as shown in Fig. 7. During charging-discharging transition period which is from $t_1<t<t_2$, the system continues to function in charging mode but with reducing voltage reference $V^{*}_{uc}$ which is as shown in Fig. 7(b). Based on (2), the charging current reference reduces causing the inductor current $i_L$ to reduce which can be observed in Fig. 7(c). This continues until $i_L$ reduces to zero value after which discharging closed loop control takes over. It should be noted that by changing the value of virtual resistance, $R_v(kT_s)$ the mode transition time can be changed accordingly. The enable signals plotted are based on mode identification algorithm summarized in Table. II.

![Fig. 6: Simulation results during charging-discharging-charging period for (a) inductor current $i_L$, (b) output voltage $V_o$, (c) UC stack voltage $V_{uc}$.](image)
B. During discharging-charging transition

The simulation results during discharging-charging transition is as shown in Fig. 8. During discharging-charging transition period which is from $t_3 < t < t_4$, the system continues to function in discharging mode but with reducing voltage reference $V_o^*$ which is as shown in Fig. 8(b). Since $V_o$ value is greater than voltage reference ($V_o^*$) due to restoration of supply voltage $V_g$, the negative voltage loop error results in reduction of discharging loop current reference causing the actual inductor current $i_L$ to reduce which can be seen from Fig. 8(c). This continues until $i_L$ reduces to zero value after which charging closed loop control takes over. The corresponding enable signals for various control modes based on Table II are as shown in Fig. 8(a).
The typical value of $\Delta r$ used for simulation and experimentation is $2 \times 10^{-3}\Omega$. Hence, based on Fig. 7 and Fig. 8, it can be seen that transition from charging to discharging mode is seamless indicating that the switch control strategy based on virtual resistance is quite effective for backup purposes.

V. EXPERIMENTAL RESULTS

This section provides the experimental results for the switch control of bidirectional dc/dc converter using virtual resistance based mode identification algorithm.

A. Performance during charging period

Fig. 9 shows the charging profile of the UC stack for a charging current of $I_{uc}=1A$. The UC stack is charged to 16V in a span of 200s which can be verified using (11). Instant (a) indicates the start of mode identification algorithm which identifies the charging mode accurately. $I_{ucs}$ in Fig. 9 and Fig. 10 is the voltage output of the current sensing card.

\[ C_{uc} \frac{dV_{uc}}{dt} = i_{uc} \quad (11) \]

Fig. 9: Charging of UC stack from 0-16V [Ch.1: $i_{uc}$ 500mA/div., Ch.2: $V_{uc}$ 5V/div., Ch.3: $V_{dc}$ 5V/div., Ch.4: $I_{ucs}$ 1V/div., time scale: 20/s/div.]

In Fig. 9, outer voltage loop is saturated with high $K_{vc}$ of 100 (Table. I) in order to demonstrate current control. During the charging period, the input voltage $V_{dc}$ is at 26V indicating the presence of a voltage source $V_g$. Fig. 10 shows the zoomed in version of the various waveforms for a charging current of $I_{uc}=2A$. The switching ripple corresponding to 100kHz can also be observed.

Fig. 10: Waveforms during charging mode [Ch.1: $V_{dc}$ 5V/div., Ch.2: $V_{uc}$ 5V/div., Ch.3: $i_{uc}$ 1A/div., Ch.4: $I_{ucs}$ 1V/div., time scale: 10\(\mu\)s/div.]

VI. CONCLUSIONS

In this paper, a new switch control strategy based on virtual resistance method is proposed to ensure a smooth, seamless transition between charging and discharging modes. Based on the proposed control, the corresponding control modes are accurately identified which can be observed from the simulation results. By increasing or decreasing the virtual resistance, the corresponding mode transition times can be increased or decreased respectively ensuring complete control over the mode transition times. Smooth and seamless transition between charging and discharging control modes and vice-versa is also ensured. This is verified using simulations results.

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REFERENCES


