GaN: Applications: Optoelectronics
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- The GaN LED industry is >10 billion $ today.
- Other optoelectronic applications of GaN include blue lasers and UV emitters and detectors. UV emitters could potentially be used in water purification while solar blind UV detectors are used for missile plume detection.
GaN: Applications: High Power Electronics
(Source: Yole Development)
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(Source: Yole Development)

- While GaN optoelectronics is very well established, GaN based high power electronics is just emerging. It is predicted, based on current knowhow, that GaN based devices will be dominant in the category up to 600 V. Beyond 1200 V, SiC is expected to dominate. Other compound semiconductors, like gallium oxide, are emerging and could also play a key role.
- While the current discrete power devices market (all materials) is about 30 billion US$, the GaN power devices market in 2020 is expected to be of the order of a few billion US$.
GaN: Applications: High Frequency Electronics 
(Source: Yole Development)

- GaN transistors can enable devices that operate at very high frequencies, up to 400 GHz cut off frequency has been demonstrated. In contrast, the power applications discussed in the previous slide are expected to operate at frequencies of up to 2 MHz as of now. These very high frequencies are used in a number of applications such as radars and wireless and satellite communications.
GaN: The four components of the ecosystem

- In order to enable GaN based system technology four components need to coexist
- They are
  a. Material deposition capability
  b. Device design and fabrication capability
  c. Device packaging capability
  d. System integration.

Testing for a variety of structural and electrical parameters are conducted during every part of the process.

It is important to note that for system development, it is not just the GaN based transistor alone that needs to be developed but also passives such as capacitors and inductors that can operate at the higher frequencies.
5. Gate Deposition
Ni/Au : 20/130nm

6. Surface Passivation
Si₃N₄ : 50nm

7. Contact Pad Opening
RIE
GaN: Science to Systems

- Such an interdisciplinary activity always throws up challenges as different members of the ecosystem speak in different languages. In order to communicate better the experience in IISc has shown that it is best to come up with a device data sheet. Then members from across the spectrum need to relate the outcome of their efforts to it effect of a particular data sheet parameter. For instance, the person involved with material deposition is typically worried about the effect of deposition conditions with material properties such as mobility and sheet carrier concentration. These in turn affect on state resistance a parameter found on that sheet. Once this correlation is established the power electronics engineer will be able to better appreciate the language of the grower, who in turn will better appreciate the requirement of the power electronics engineer.
- An example of such a data sheet can be found on the next slide.
## The interface between the device engineer and the power electronics engineer:

<table>
<thead>
<tr>
<th>Device parameter</th>
<th>EPC2105 (80V, 9.5A)</th>
<th>EPC2103 (80V, 23A)</th>
<th>EPC2029 (80V, 31A)</th>
<th>EPC2021 (80V, 60A)</th>
<th>Proposed device (75V, 5A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum pulsed drain current (A)</td>
<td>75</td>
<td>195</td>
<td>360</td>
<td>420</td>
<td>50</td>
</tr>
<tr>
<td>Drain-source leakage current (I_{DSS}) (μA)</td>
<td>150</td>
<td>325</td>
<td>700</td>
<td>700</td>
<td>92</td>
</tr>
<tr>
<td>Gate-source leakage current (I_{GSS}) (mA)</td>
<td>2.5</td>
<td>6.5</td>
<td>9</td>
<td>9</td>
<td>1.24</td>
</tr>
<tr>
<td>Drain-source on resistance (R_{DS(on)}) (mΩ)</td>
<td>14.5</td>
<td>5.5</td>
<td>32.</td>
<td>2.5</td>
<td>28</td>
</tr>
<tr>
<td>Input capacitance (C_{iss}) (pF)</td>
<td>300</td>
<td>160</td>
<td>1400</td>
<td>1700</td>
<td>190</td>
</tr>
<tr>
<td>Output capacitance (C_{oss}) (pF)</td>
<td>200</td>
<td>630</td>
<td>900</td>
<td>1000</td>
<td>92</td>
</tr>
<tr>
<td>Reverse transfer capacitance (C_{rss}) (pF)</td>
<td>3</td>
<td>8.7</td>
<td>20</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>Total gate charge (Q_{g}) (nC)</td>
<td>2.5</td>
<td>6.5</td>
<td>13</td>
<td>15</td>
<td>2.2</td>
</tr>
<tr>
<td>Gate-source charge (Q_{gs}) (nC)</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>3.8</td>
<td>0.96</td>
</tr>
<tr>
<td>Gate-drain charge (Q_{gd}) (nC)</td>
<td>0.5</td>
<td>1.3</td>
<td>2.5</td>
<td>2.1</td>
<td>0.4</td>
</tr>
<tr>
<td>Output charge (Q_{oss}) (nC)</td>
<td>11</td>
<td>33</td>
<td>57</td>
<td>56</td>
<td>8</td>
</tr>
<tr>
<td>Source-drain reverse recovery charge (Q_{rr}) (nC)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
The device requirements:

“High” Current or low “ON Resistance”:
Density of charge carriers and their mobility

“High” Blocking “OFF State” Voltage or low Leakage:
Low density of charge carriers and their mobility

“High” Frequency of operation:
Mobility or saturation velocity of charge carriers
## Si vs GaN

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>GaN</th>
<th>SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap (eV)</td>
<td>1.2</td>
<td>3.2</td>
<td>3.4</td>
</tr>
<tr>
<td>Breakdown field (MV/cm)</td>
<td>0.3</td>
<td>3.3</td>
<td>3.5</td>
</tr>
<tr>
<td>Channel Mobility (cm²/V·sec)</td>
<td>300</td>
<td>2000</td>
<td>650</td>
</tr>
</tbody>
</table>

![Graph showing specific on resistance vs breakdown field for Si and GaN](image-url)
The GaN Advantage:

- GaN power devices are smaller and more efficient than Si devices.
HEMT: High Electron Mobility Transistor

SiN$_x$ or GaN cap
AlGaN

GaN

Transition Layers

Si (2”-6”)

+ +

-
2D Electron Gas: Unlike in other systems, a 2D gas is formed at the interface shown due to polarization effects and not due to doping. As a result, the charge pool is not formed due to thermal activation and exists at all temperatures even down to temperatures less than 4K. Its typical density is \( \sim 10^{13}/\text{cm}^2 \) with mobilities as high as 1800-2000 cm\(^2\)/V-sec. Such high mobilities are the reason behind the use of the HEMT terminology. Bulk Si mobility is 1500 whereas transistor channel mobilities are 300 cm\(^2\)/V-sec.
**Substrates:** Unlike in Si and GaAs technologies bulk substrates are not available for GaN epitaxial growth. The problem is so challenging, that its solution was rewarded with the 2014 Nobel prize in Physics. The table below summarizes the challenges involved.

<table>
<thead>
<tr>
<th>Material</th>
<th>Lattice Constant (and % mismatch)</th>
<th>CTE (x10^{-6}/K) (%Strain, Stress)</th>
<th>Thermal Conductivity (W/mK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN (0001)</td>
<td>3.189</td>
<td>5.6</td>
<td></td>
</tr>
<tr>
<td>AlN (0001)</td>
<td>3.112 (-2.4%)</td>
<td>4.2 (+0.14%)</td>
<td></td>
</tr>
<tr>
<td>Al₂O₃ (0001)</td>
<td>4.758 (-16%)</td>
<td>7.5 (-0.19%, -1 GPa)</td>
<td>30</td>
</tr>
<tr>
<td>SiC (0001)</td>
<td>3.08 (-3.4%)</td>
<td>3.2 (+0.24%, 0.6 GPa)</td>
<td>490</td>
</tr>
<tr>
<td>Si (111)</td>
<td>3.840 (+20.4)</td>
<td>3.6 (+0.20%, +1 Gpa)</td>
<td>130</td>
</tr>
</tbody>
</table>
**Dislocations in GaN Growth:** Due to the heteroepitaxial nature of growth GaN films have a lot of stress and defects in them. These defects, called dislocations, need to be managed in order to make good devices. Dislocations are seen as bright lines in the image (transmission electron microscope image) below. These defects, as the reader should note intersect the 2D gas channel. They, hence, impede electron transport.
GaN Growth Reactor at CeNSE, IISc
**Strain Generation and Curvature:** Due to stress and strain during growth, the wafer bends. It is essential during growth to manage this curvature for flat wafers are needed for device processing. The plot on the left below shows how the wafer curvature which is zero at the beginning changes during growth. It eventually comes to a value close to zero at the end. This is due to careful design of the stack and growth parameters. These curvature changes can also be correlated to atomic level processes happening on the growth surface that result in the microstructure shown on the right.
Wafer to Device

- SiN$_x$ or GaN cap
- AlGaN
- Transition Layers
- Si (2”-6”)
An example of a typical device fabrication mask:

- Circular TLM
- Current Density
- Layer Metal Resistivity
- Square TLM
- Hall Structure
- Alignment layer 01
- Alignment layer 02
- Alignment layer 03
- Alignment layer 04
- Alignment layer 05
- Alignment layer 06
- Hall Structure
An example of a Device Fabrication

1. Starting substrate

2. Mesa Etching
   RIE : Cl₂ Plasma

3. S-D Deposition

4. Rapid Thermal Annealing

5. Gate Deposition

6. Surface Passivation
   Si₃N₄ : 50nm

7. Contact Pad Opening
   RIE